Applications of Type-I Hybrid-ARQ Error Control

Professor Michael Rice
Department of Electrical and Computer Engineering
Brigham Young University
Provo, Utah 84602
(801) 378 - 4469

abstract

Hybrid-ARQ schemes employ the simultaneous application of error-detection and error-correction to combat transmission errors in a data communications system. In this way automatic repeat request (ARQ) and forward error correction (FEC) schemes are combined to offer effective error control. The key to implementation is the identification of reliability information in the FEC decoding process which is used to alter the FEC decoding algorithm. Under certain channel conditions, the realized efficiency is superior to that of either FEC or ARQ.

1 Introduction

A data communications system is designed to move digital data from a source to an end user. Most channels exhibit various forms of noise which corrupt the data and cause transmission errors. A typical data communications system consists of a data source/destination pair, a channel encoder/decoder pair, a modulator/demodulator pair, and a physical channel. The channel encoder inserts redundant symbols based on an (n, k) linear block code into the information symbol stream to form n-tuples called codewords denoted v. Each codeword is modulated onto a carrier and then transmitted over the channel. For the purposes of this paper, the transmitter/modulator, channel, and receiver/demodulator are grouped together in the coding channel. The channel encoder/decoder pair sees the coding channel as an additive source of noise symbols which adds an error vector e to v resulting in a received n-tuple $r = e + v$. At the receiving end, the decoder uses the redundancy contained in r in an effort to determine if any errors have occurred during transmission. Traditionally there have been two catagories of error control techniques: Automatic-Repeat-Request (ARQ) and Forward-Error-Correction (FEC).

An ARQ error control scheme features error detection in conjunction with a retransmission protocol. If no errors are detected in r, it is assumed to be error free and is delivered to the user. When the presence of errors in r is detected, the decoder discards r and requests a retransmission via a return channel. Retransmissions of a particular word continue until it is accepted by the decoder. A decoding error is committed whenever r is accepted and r contains errors. The throughput is a measure of the efficiency of the scheme and is defined as the average number of information symbols accepted per transmitted symbol [1]. The throughput is a function of the code, the channel, and the retransmission protocol and is usually expressed as the product of the code rate k/n and a factor which decreases as the probability of retransmission increases. Thus a degradation in the channel conditions results in inefficient use of the channel and unwanted delay since a great deal of time must be dedicated to retransmitting words with errors. This is the major drawback of ARQ schemes.

In an FEC scheme, the parity check symbols are used for error-correction. When the decoder detects the presense of errors in r it attempts to determine the error locations and correct them. If the exact locations of errors are determined, r will be correctly decoded. On the other hand, if the decoder fails to determine the exact locations of the errors, r will be decoded incorrectly and erroneous data will be delivered to the user. Since there is no return channel, retransmissions are not an option. For this reason high system reliability is often difficult to achieve. The throughput of an FEC scheme is simply the code rate k/n which remains constant with changing channel conditions. FEC schemes are used in systems where retransmissions are not practical or not possible such as communications with deep space probes and magnetic data storage [2].

The error events in ARQ systems are less likely than those oil FEC systems. For this reason, a given (n, k) code will give better reliability when used in an ARQ scheme than in an FEC scheme. However, the throughput of ARQ systems decreases as the channel degrades whereas in an FEC scheme it remains constant. To compensate for this, combined error-detection and error-correction are incorporated into type-I hybrid-ARQ schemes. Type-I hybrid-ARQ schemes, first proposed by Wozencraft and Horstein in 1960 [3], are implemented by correcting a limited number of frequently occurring error patterns (usually simple, low weight patterns) and requesting a retransmission when a more complicated or less frequent error-pattern is encountered. By performing some error correction, the probability of retransmission is reduced, thereby improving the throughput over that of the pure ARQ. The retransmission of unreliable packets increases the system reliability beyond that of the FEC system alone. In this way the positive features of both FEC and ARQ are combined.

2 Implementation

A linear block code with minimum distance d_{min} is capable of correcting all error patterns of weight $\lfloor \frac{d_{min}-1}{2} \rfloor$ or less contained in the received word. Hybrid-ARQ error control is performed by defining a number t called the allowed error correcting capability of the code. When $t < \lfloor \frac{d_{min}-1}{2} \rfloor$ the code is able to simultaneously correct v errors where $t < v < d_{min} - t$. When the number of errors in r is less than or equal to t, an ACK is returned to the sender and the information content of r is delivered to the user after decoding is completed. If the number of errors in r appears to be greater than t then r is discarded and a NAK is returned to the sender. A decoding error occurs when tile error pattern causes r to be within a distance t of a codeword other than the one sent.

The reliability of block codes is measured by P_u , which is the probability that for a single transmission the received block contains errors. When a block code is used in a retransmission scheme the reliability is measured by $P_u(E)$ which is the probability that an accepted block contains an undetected error:

$$P_u(E) = \frac{P_u}{1 - R}. \tag{1}$$

where R is the probability of retransmission.

The performance of binary block codes used in a type-I hybrid-ARQ scheme over a BSC with crossover probability p are [41

$$P_c = \sum_{i=0}^{t} \binom{n}{i} p^i (1-p)^{n-i} \tag{2}$$

$$P_u \approx \frac{\sum_{i=0}^{t} \binom{n}{i}}{2^{n-k}} \sum_{j=d_{min}-t}^{n} \binom{n}{j} p^i (1-p)^{n-i} \tag{3}$$

$$R = 1 - P_c - P_u. \tag{4}$$

Type-I hybrid-ARQ is implemented by a modification to the FEC decoder. The key to implementation is the identification of a source of reliability information in the decoding process. This reliability information is used to determine if the decoder's estimate of the received word is reliable. If it is deemed that the estimate is reliable, decoding proceeds as usual and the estimate is delivered to the user. An unreliable estimate on the other hand generates a request for a retransmission.

2.1 Modified BCH Decoders

BCH (Bose - Chandhuri - Hocquenghen) codes are of great practical importance for error correction, particularly if the expected number of errors is small compared with the code length [5]. They are, as a class, the best known constructive codes for channels in which errors affect successive bits independently [6]. The use of BCII codes in a type-I hybrid-ARQ scheme has been considered before [7]. The decoding algorithm used in most applications is a bounded distance decoding algorithm that iterivcly generates an "error location polynomial" from the syndrome of the received word. The roots of this polynomial indicate the positions of the errors in the lowest weight error pattern associated with the syndrome. Thus the degree of the error locator polynomial can be used as a source of reliability information since it is a reliable estimate of the number of bit errors that have corrupted the received word. The modification of this decoder is all application of the more general case developed by Wicker [8] and is illustrated in Figure 1. The comparitor tests the degree of the error locator polynomial. If it is greater than the allowed error-correcting capability t of the coding strategy, decoding is halted and a retransmission of the codeword is requested. Otherwise, decoding proceeds as usual. Since BCH codes are binary, the "error magnitude computation" block is not necessary.

2.2 Modified Majority Logic Decoders

Although the codes which are decodable using majority logic techniques are somewhat less powerful than BCH codes for practical values of n, k, and d_{min}, they are an important class of codes due to the ease with which they are decoded. The decoding circuitry is simple to implement and thus offers an attractive alternative for error control where there are severe hardware constraints or where a high data rate precludes the use of another decoding method. This class of codes includes Reed-Muller, Euclidean geometry, and projective geometry codes [5, 9].

The use of J orthogonal check sums in a voting scheme provides a natural source of reliability information in these decoders [10]. The error pattern contained in the received word is determined in a bit by bit fashion; each error bit is assigned the value assumed by the majority of the check sums orthogonal on it. The lack of a clear majority indicates an unreliable condition in the decoding process. To modify the FEC decoder, a retransmission region of width τ centered about $\lfloor \frac{J}{2} \rfloor$ is defined so that if the number of l's (denoted η) among the J check sums is within this region, a retransmission is requested. The modified majority logic rule is defined as follows:

Let $\hat{e}_j$ be the estimate of error bit e_j. Then

$$\hat{e}_j = \begin{cases} 0 & \text{if } \eta \leq \lfloor \frac{J}{2} \rfloor - \lceil \frac{\tau}{2} \rceil \\ 1 & \text{if } \eta \geq \lfloor \frac{J}{2} \rfloor + \lfloor \frac{\tau}{2} \rfloor + 1 \end{cases}$$

else request a retransmission.

This alteration produces a coding strategy which corrects $t = \lfloor \frac{J}{2} \rfloor - \lceil \frac{\tau}{2} \rceil$ errors and detects up to $\nu = \lfloor \frac{J}{2} \rfloor + \lceil \frac{\tau}{2} \rceil$ errors. The general modification to the estimation circuitry is shown in Figure 2 where the J check sums orthogonal on the error bit are denoted $A_0, A_1, \ldots, A_{J-1}$. The modification is made to the majority logic gate in the l -step decoder, to the final stage in the L-step decoder, or to the final majority logic estimation circuit in any of the variations of majority logic decoding.

2.3 Modified Reed-Solomon Decoders

The codes which have been discussed so far have been binary codes. Reed-Solomon codes are a powerful class of maximum distance separable (MDS) nonbinary codes. These codes consist of codewords of a fixed length n whose elements are selected from an alphabet $\{0,1,..,2^m - 1\}$ so that m information bits are mapped into one of the $2^m - 1$ symbols. Kasami and Lin [11] showed that MDS codes are effective for both pure error-detection (ARQ) and simultaneous error-correction and -detection (hybrid-ARQ). Wicker studied the modification of the FEC decoder of these codes in a hybrid-ARQ scheme for high reliability data transfer over a land mobile radio channel [8]. The modification of the FEC decoder is basically the same as that of the BCH code decoder discussed above. The essentials of the modification are shown in Figure 1.

Error Control Strategy	BCH Code	Throughput	Probability of Block Error
HARQ	(128,99,4) t = 3	0.774	1.519×10^{-7}
ARQ	(128,113,2)	0.420	1.296×10^{-7}
FEC	(128,71,9)	0.559	5.707×10^{-9}

Table 1: Performance Comparison for Error Control Strategies

The performance of an (n,k) Reed-Solomon code with symbols from $GF(2^m)$ over a memoryless 2^m-ary symmetric channel is given by exact expressions, since the codeword weight distribution $\{A_i\}_{i=0}^{n}$ is known. Let q be the probability that that a symbol is correctly received and let p represent the probability that a particular symbol error occurs (assume all symbol errors are equally likely) so that $q + (2^m - 1)p = 1$. Then the performance is given by

$$P_u = \sum_{j=d_{min}}^{n} A_j \sum_{k=0}^{t} P_k^j \quad (5)$$

$$P_c = \sum_{i=0}^{t} \binom{n}{i} (1-q)^i q^{n-i} \quad (6)$$

$$R = 1 - P_c - P_u \quad (7)$$

where P_k^j, the probability that a received word is within a distance k of a weight j codeword, is given by

$$P_k^j = \sum_{r=0}^{k} \binom{j}{k-r} \binom{n-j}{r} p^{j-k+r}(1-p)^{k-r} q^{n-j-r}(1-q)^r.$$

3 Results

As an example consider the following problem: It is desired to maintain a block error rate of 10^{-6}, or less over a channel which has a received signal to noise ration of 1 dB and suppose further, that hardware constraints limit the length of the code to 128 bits. The hybrid-ARQ error control strategy, offering the highest throughput[1] is a (128,99,4) BCH code with t = 3. The performance of this strategy compared to the traditional ARQ and FEC strategies is presented in Table 3. It is seen that at this SNR the type-I hybrid-ARQ error control outperforms (in terms of throughput) either the FEC or the ARQ strategies. This translates into a reduction of the required bandwidth expansion or an increase in the effective available information data rate.

It is interesting to observe the throughput curves for these three error control strategies as a function of SNR as illustrated in Figure 3. Of the three error control strategies under consideration in this example, the hybrid-ARQ strategy offers the best throughput when $0 < SNR < 2$ dB.

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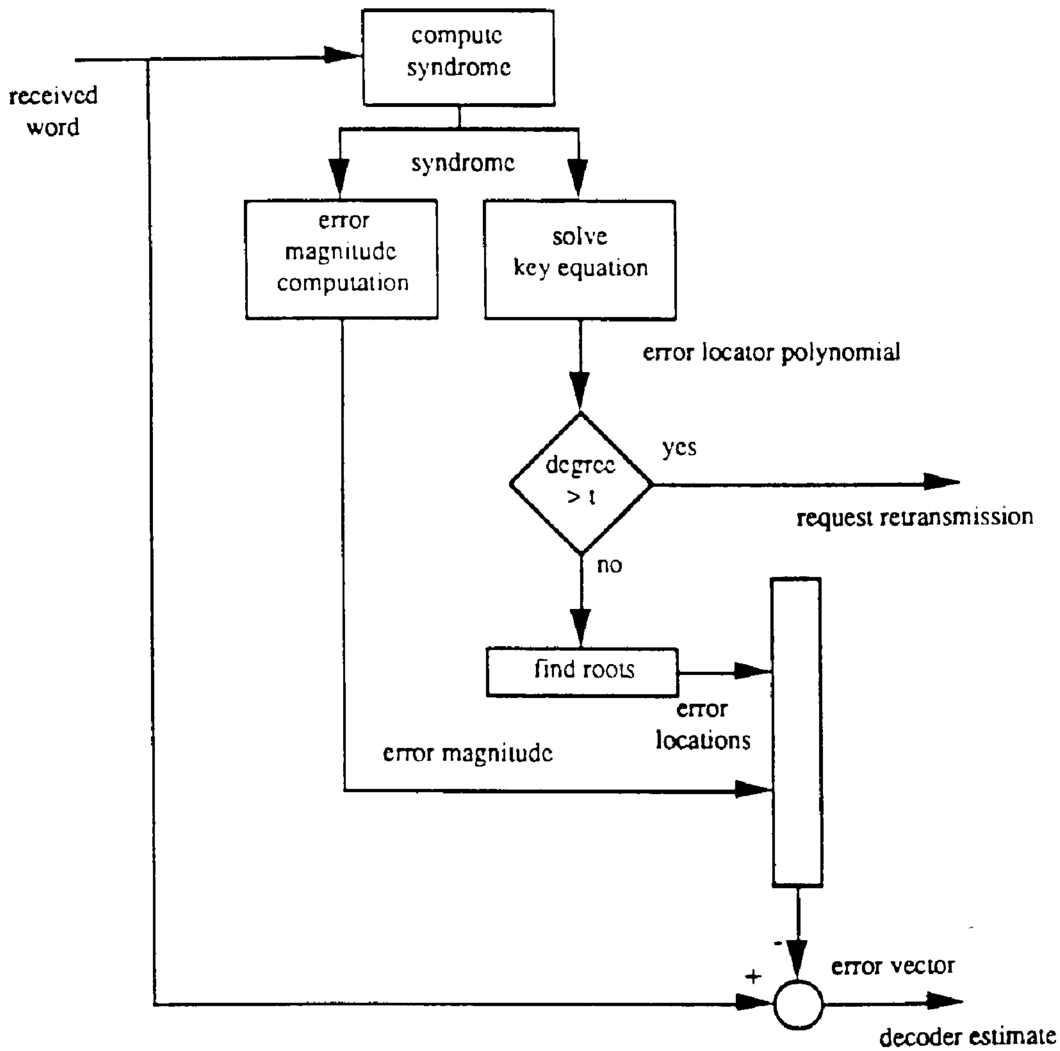

Figure 1: Modification of the Algebraic FEC Decoder

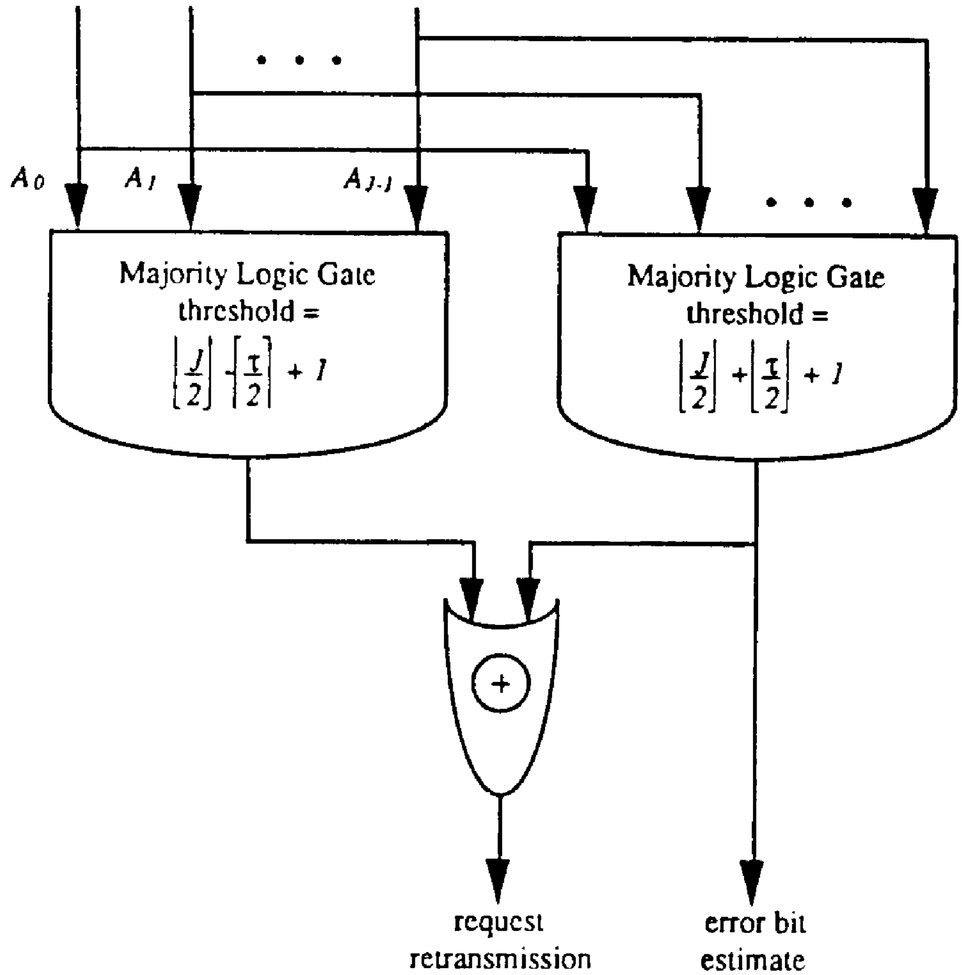

Figure 2: Modification of the Majority Logic Estimation Circuitry

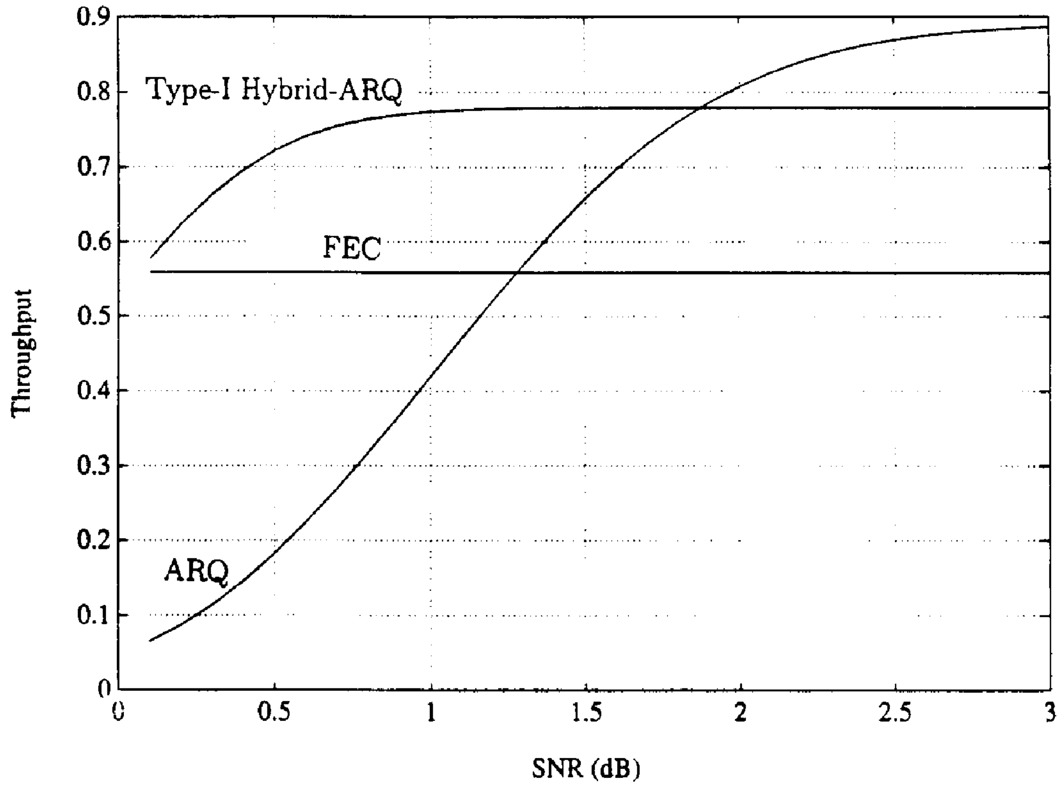

Figure 3: Throughput Comparisons