

SGLS COMMAND DATA ENCODING USING DIRECT DIGITAL SYNTHESIS

Michael Gordon
Computer Engineer
Cincinnati Electronics Corporation
Space Products SBU
Mason, OH 45040

KEYWORDS

Encoding, SGLS Command Data, Direct Digital Synthesis

ABSTRACT

The Space Ground Link Subsystem (SGLS) provides full duplex communications for commanding, tracking, telemetry and ranging between spacecraft and ground stations. The up-link command signal is an S-Band carrier phase modulated with the frequency shift keyed (FSK) command data. The command data format is a ternary (S, 1, 0) signal. Command data rates of 1, 2, and 10 Kbps are used.

The method presented uses direct digital synthesis (DDS) to generate the SGLS command data and clock signals. The ternary command data and clock signals are input to the encoder, and an FSK subcarrier with an amplitude modulated clock is digitally generated. The command data rate determines the frequencies of the S, 1, 0 tones. DDS ensures that phase continuity will be maintained, and frequency stability will be determined by the microprocessor crystal accuracy.

Frequency resolution can be maintained to within a few Hz from DC to over 2 MHz. This allows for the generation of the 1 and 2 Kbps command data formats as well as the newer 10 Kbps format. Additional formats could be accommodated through software modifications. The use of digital technology provides for encoder self-testing and more comprehensive error reporting.

INTRODUCTION

The Space Ground Link Subsystem (SGLS) provides full duplex communications for commanding, tracking, telemetry and ranging between spacecraft and ground stations. The

uplink RF carrier is phase modulated with command data, command sync, and Pseudo Random Noise (PRN) ranging data. The uplink frequencies are in the range of 1750 to 1850 MHz, while the downlink frequencies for tracking and telemetry are within the range of 2200 to 2300 MHz.

The ground encoder converts digital data to a modulation format for transmission over the RF link. This paper describes a microprocessor-based method of signal generation recently developed at Cincinnati Electronics Corporation. This concept is presently used in several models of signal generation equipment.

SGLS SYSTEM AND DATA RATES

The uplink command data and sync signal can be combined with ranging PRN data which phase modulates the uplink RF carrier. The command data consists of ternary (S, 1, 0) frequency shift keyed (FSK) tones which are amplitude modulated at 50% index with a triangular clock signal. Command data rates are 1K, 2K, and 10K bits per second. The S, 1, 0 keyed tone frequencies are described in Table I. Figure 1 displays the typical command data and sync signal format.

Table I. SGLS Command Tone Characteristics

Command Tones (nominal)*				Command Sync	
Data Rate	Logic "1" Frequency	Logic "0" Frequency	Logic "S" Frequency	Mod Freq.	Waveform Type**
1K bps	95 kHz	76 kHz	65 kHz	500 Hz	Triangular
2k bps	95 kHz	76 kHz	65 kHz	1000 Hz	Triangular
10K bps	975 kHz	1024 kHz	1073 kHz	10K Hz	Triangular

*All tolerances $\pm 0.01\%$

**Amplitude modulation of command tones

DIRECT DIGITAL SYNTHESIS

Direct Digital Synthesis (DDS) is a technique to generate complex signals while maintaining fine frequency resolution, continuity of phase, and fast switching speed. DDS is the reverse of Digital Signal Processing (DSP). With DSP, a signal is band-limited, then sampled and digitized. The digitizer provides a number sequence that can be processed to identify characteristic parameters. With DDS, the characteristic parameters are used to generate a number sequence, that is converted to an analog waveform. The alias signals are removed with a band-limiting filter.

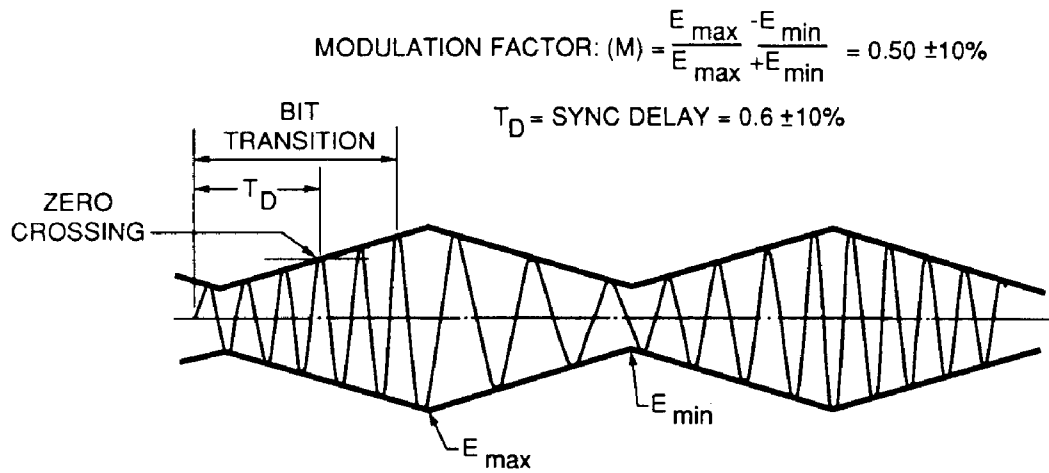


Figure 1. Typical Command Tone Modulation Envelope

DESCRIPTION OF DDS SYSTEM

There are several ways to implement a DDS system. If the ability to generate high frequencies is unnecessary, it is possible to use a general purpose microprocessor. This implementation has been used in many low and medium speed modems, for example. As requirements for synthesizing higher frequencies develop, the computational processing becomes prohibitive for modem high speed processors, and implementation with dedicated hardware becomes necessary.

HARDWARE IMPLEMENTATION OF DDS

The implementation of a DDS or number-controlled oscillator (NCO) in hardware is straightforward. The objective of an NCO is to produce a signal:

$$y(t) = A \sin (2\pi f_{\text{signal}} t) \quad (1)$$

where f_{signal} is the frequency to be synthesized and A is the amplifier gain. The discrete equivalent of equation (1) is:

$$y(kT) = A \sin (\phi kT) \quad (2)$$

where $y(kT)$ is the k th sample generated with T as the sample interval. Equation (3) relates the factor $2\pi f_{\text{signal}}$ in (1) to the phase step ϕ in (2):

$$\phi = \frac{2\pi f_{\text{signal}}}{f_{\text{clock}}} \quad (3)$$

where f_{clock} is the oscillator clock frequency driving the DDS hardware.

The frequency synthesized by the NCO is determined by the phase step ϕ . Since the sine function is periodic in $(0, 2\pi)$, the accumulator needs to represent values between $(0, 2\pi)$. If a 16 bit accumulator were used, there would be 65536 unique values. A change in the least significant bit (LSB) would represent a phase change of $(2\pi / 65536)$ or $9.6E-05$ radians. Changing the phase increment changes the output frequency, while maintaining phase continuity.

The three basic blocks of an NCO as shown in Figure 2 are the digital accumulator, waveform map, and digital to-analog converter.

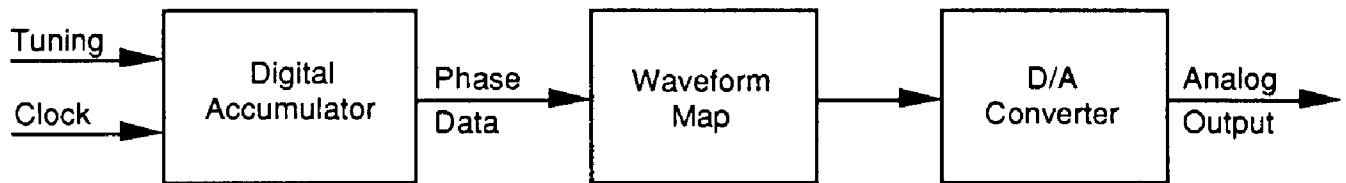


Figure 2. Block Diagram Representation of a NCO

Generating precise, phase continuous SGLS command data and sync signals using an analog scheme is relatively difficult. DDS makes precision generation of the SGLS command data and sync signals relatively easy. The DDS implementation requires two NCOs: one for generating command data and one for generating command sync signals. The low frequency command sync signal is generated in the first NCO and the analog output is used as a reference for a multiplying D/A converter in the command data NCO. The final result is command data tones that are amplitude modulated with the triangular waveform command sync signal. Figure 3 shows the block diagram representation of the SGLS encoder.

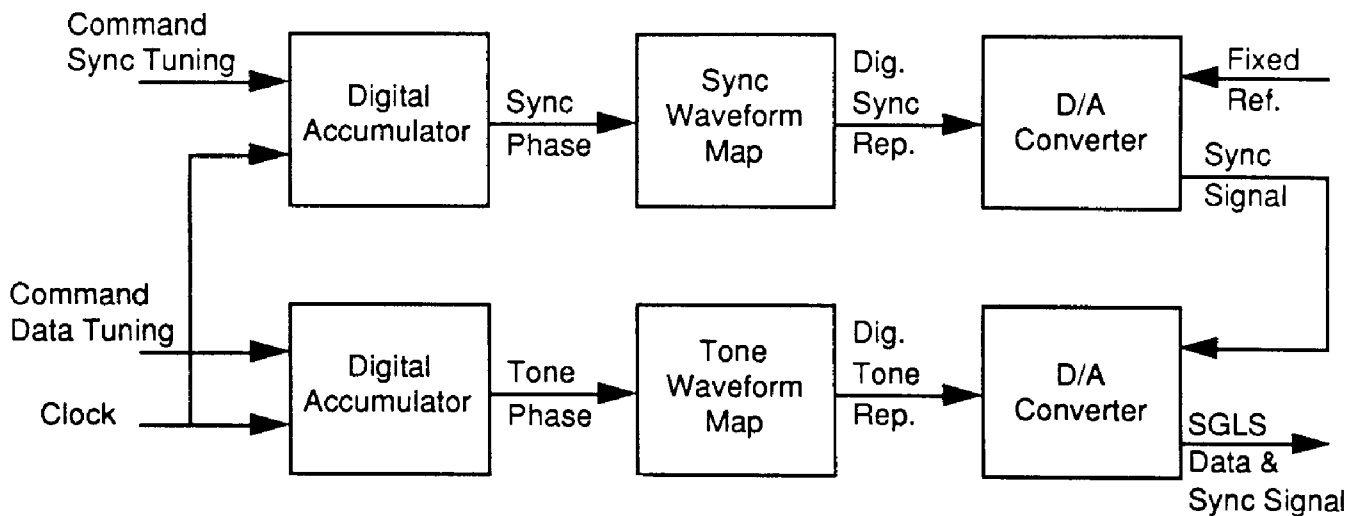


Figure 3. Block Diagram for SGLS Encoder

ALIAS FILTERING

The digitally generated signal is not a perfect representation of the desired waveform. There are alias signals present at frequencies $f_{\text{clk}} - f_{\text{signal}}$, $f_{\text{clk}} \pm f_{\text{signal}}$, $2f_{\text{clk}} \pm f_{\text{signal}}$, $3f_{\text{clk}} \pm f_{\text{signal}}$, etc.,. These signals must be removed using a low-pass filter for a suitable output waveform. The maximum output frequency should not exceed 40% of the clock frequency. Otherwise, it will be very difficult to remove the alias at $f_{\text{clk}} - f_{\text{signal}}$ without affecting the desired signal f_{signal} .

IMPROVEMENTS DDS BRINGS TO SGLS ENCODER

The use of DDS to synthesize a complex SGLS command signal allows for phase jitter-free bit transitions, fast frequency switching, fine frequency resolution over a frequency range large enough to synthesize both the 1K and 2K as well as the 10K data rate formats. The digital-based encoder permits the addition of new signal formats through software changes as well as a comprehensive self-test capability and enhanced error reporting.

REFERENCES

McCune, Earl Jr., "Create Signals Having Optimum Resolution, Response, and Noise," EDN, Vol. 36, Issue 6, March 14, 1991, pp. 95-108.

Klements, H.D., "Air Force Satellite Control Facility Space/Ground Interface", TOR-0059 (6110-01)-3, The Aerospace Corp., El Segundo, CA, June 1987.