AN S-BAND TELEMETRY RECEIVER SYSTEM FOR DEEP SPACE APPLICATIONS

E. LAMPERT
Siemens AG
Munich, Germany.

Summary. To receive the transmitted signals from the HELIOS space probe a S-band telemetry receiver system was built. Of this system the S-band telemetry receivers and the subcarrier demodulators are described. Measured values are presented. The S-band receiver includes a digitally implemented phase-locked-loop. Polarization tracking is possible in a two channel mode as well as in a single channel mode. In the subcarrier demodulator the subcarrier is demodulated before demodulating the RF-carrier. Good noise thresholds and low degradation is reached because remodulation is used in the subcarrier loop. The equipment works in a fully computer controlled station, this includes all aquisition procedures.

Introduction. For the Helios-mission a telemetry receiver system for S-band signals between 2290 ÷ 2300 MHz is needed for the ground segment. The signals transmitted by the space probe are PCM-PSK-PM modulated. For the reception of this signal a RF-carrier as well as a subcarrier demodulation has to be performed. Therefore the S-band receiver is a coherent super-heterodyne receiver which provides the subcarrier demodulator with a wide-band IF-signal together with a phase-coherent reference. After subcarrier demodulation the analogue baseband signal (NRZ-data and additive thermal noise) is transferred to the symbol synchronizer.

During the Helios-Mission the 100 m radiotelescope in Effelsberg (Germany) will be used for telemetry reception. For future Deep Space Missions this will be scarcely possible. According to this the complete receiving station was built into a container with exception to those parts which had to be mounted in the apex cabine of the antenna. Therefore the separate parts of the equipment had to be built in compact blocks.

Apart from mission-specific requirements it was obvious that the equipment should be built to suit all future mission requirements as for as possible. So this equipment is in several points similar to the JPL-Block IV equipment [1]. So it is possible to upgrade the system for X-bandreception and also with instrumentation for Doppler and range measurement. The major demand for the system was fully automatic computer-controlled performance and also the possibility for easy maintenance [2].

Receiver System. The telemetry receiver system, Fig. 1. is used to receive linear or circular polarized waves in the frequency band from 2290 to 2300 MHz and is designed for the demodulation of PCM-PSK-PM modulated signals.

For polarization tracking a two-channel receiver is used, the inputs of which are connected via MASERs with the two outputs of the Ortho-Mode-Transducer (OMT) of the polarizer. The RF-polarizer consists of two “ Quarter-Wave-Plates” of which the one - when receiving linearly polarized waves - is rotated until the signal disappears in one specific arm of the OMT. So one gets the completely received signal power in the second arm of the OMT. The sumchannel of the receiver is connected to this arm and provides the signal for the receiver Phase-Locked-Loop (PLL). The error signal in the other receiver-channel has to be demodulated coherently to provide a tracking error signal for rotating the Quarter-Wave-Plate. This requires a fixed phase relation between both channels, which is made more difficult as in both channels an IF-transmission on separate cables over 200 m is included. So it is necessary that in both channels the same transferoscillator signals will be used. To provide a high degree of redundancy and to make parts of the equipment interchangeable instead of a two channel receiver two complete single channel receivers are used. The built-in frequency supply of each equipment is externally connected to the mixer inputs. When working with polarization tracking both frequency supplies are connected with a distribution box. It supplies the mixers of both receivers with the same signals. AGC voltage and polarization error signals are also distributed from this drawer. Each of both receivers can equally used as polarization sum or error channel. In the case of a failure in one receiver polarization tracking can still be maintained (accuracy then about 5°). The polarization tracking loop then works in a jitter mode. To reach this performance the AGC provides a power level resolution of less than 0,5 dB. The S-band receivers are equipped with Narrow-band PLL and have an AGC usable for power level measurements. This loop can work in a coherent or incoherent mode by choise.

The subcarrier demodulators (SDA) following the telemetry receivers allow either the demodulation of a single subcarrier - the second SDA is then redundant - or the demodulation of a single RF-carrier modulated with two subcarriers. In the latter case one of the two analogue baseband signals has to be recorded on tape. It can be processed “off line” later on.

S-Band Receiver. The S-band receiver is a superheterodyne receiver with a first IF at 74 MHz centerfrequency. In a tuned receiver a telemetry signal at an arbitrary frequency between 2290 and 2300 MHz is downconverted into this IF so that the frequency of the residual carrier has exactly 74 MHz. The 10 MHz wide frequency band is now downconverted to a centerfrequency of 10 MHz. This IF-frequency was strongly requested for compatibility reasons with the NASA Deep Space Network (DSN). In order to have the possibility to process signals with carrier-power to noise density ratio of less than

11 dBHz bandpassfiltering with bandwidths down to about 300 Hz is necessary. This can be achieved by using an IF-frequency of less than 1 MHz. So a third IF at 400 kHz was introduced.

The receiver consists of the following units

Antenna unit
IF-part with frequency supply
DANA-Synthesizer 7010-S179
Digital Control Unit with PLL

In the antenna unit a third order bandpassfilter is used for the necessary selectivity. The local oscillator for the downconversion 2295/74 MHz is generated in a high level frequency multiplier chain (X48). The input of this device is connected via a 200 m cable with the DANA-synthesizer working in the frequency band from 49,25 to 49.458,9 MHz. To keep the phase uncertainties between both receiver channels down to a minimum, both mixers are connected with a common multiplier, Fig. 3. The gain of the antenna unit is 40 dB which is sufficient to provide a noise figure of less than 8 dB for the whole receiver.

The frequency response of the connected IF-transmission cable (0,1 dB/MHz) is equalized in the IF-part of the receiver. Then the residual carrier of the signal is adjusted to a fixed level of -72 dBm by an AGC-amplifier. After downconversion to 10 MHz and amplification to -55 dBm the broadband IF-signal is connected to the outputs which are joint to the further signal processing equipment (SDA, Ranging). As C/N_o - ratios of less than 11 dBHz have to be expected the dynamic range of these outputs must exceed more than 16 dBm.

The PLL is closed over a further IF at 400 kHz with phasedetection. As the phasedetector is preceded by a Hard-Limiter, actual loop noisebandwidths depend on the signal-to-noise ratio at the Limiter input. To achieve the same relative widening of the loop bandwidth dependent on the signal-to-noise ratio, for each loop bandwidth (B_{NLO} = 1,5/6/24/76 Hz) a specific IF-filter is used. The ratio of the 3 dB-IF-bandwidth to the loop designpoint noise bandwidth is fixed for all bandwidths and has a value of 200. So the IF-bandwidths are 0.3/1.2/5/18 kHz. The wideband filters use coils and capacitors whereas the two narrow band filters use a single x-tal. This results in different phase shifts at centerfrequency, so a 10 MHz reference generated by the internal frequency supply will have different phase angles with the pertinent IF-signal when the loop bandwidths are changed.

The 5 MHz station reference frequency is used for the generation of the local oscillator frequencies 64/9.6/0.4 MHz and 10 MHz, Fig. 3, and also for the synchronization of the DANA-synthesizer. (This application requires an excellent short term stability and purity of the spectrum of the 5 MHz reference apart from high long term stability.) The internally generated 10 MHz reference is processed by a phase tracking loop to compensate for the undetermined phase shift in the 400 kHz IF. So the 10 MHz reference output signal is always in quadrature (within 1°) to the residual carrier of the 10 MHz IF-signal. As already mentioned the DANA-synthesizer is used for receiver tuning. This synthesizer uses a phasecomputer so a frequency change is executed without an undetermined phasejump. With the Digital Control Unit the remote programming of the synthesizer can be altered almost continuously in small steps ($\leq 10^{-6}$ Hz), so almost arbitrary frequency sweeps can be performed. The unit has four different built-in programs:

a) triangular sweep: beginning with an initial value the frequency F is swept with the rate $|\dot{F}|$ to a prescribed limit F_1 and from there with the some absolute value of the rate $|\dot{F}|$ to F_2 and back again.

b) polygonial sweep: beginning with an initial value the frequency F is swept with the rate $|\dot{F}_1|$ to the limit F_1 . When reaching this limit F is changed with the rate $|\dot{F}_2|$ until F_2 is reached. During this interval new values for F_1, $|\dot{F}_1|$ can be read into the Data Control Unit, the same applies to F_2, $|\dot{F}_2|$ when the frequency changes via F_1. This program is very useful to diminish loop stress during swing-by manoeuvres.

c) ramp sweep : beginning with an initial value the frequency F is swept via F_1 with the rate $|\dot{F}_1|$ or F_2 with the rate $|\dot{F}_2|$.

d) frequency step via F_1 or F_2.

DANA-synthesizer and Digital Control Unit are parts of the PLL. This loop extends over the first, second and third downconversions to the phasedetector at 400 kHz, followed by a digital loopfilter built into the Data Control Unit cabinet and the synthesizer.

The 400 kHz phasedetector supplies the phase error signal, which is sampled with a frequency of 10 kHz and then converted into a 12 bit binary data word. This data stream feeds the loopfilter which has a proportional-integral characteristic according to a perfect second-order loop with the designpoint characteristic

$$H(p) = \frac{\sqrt{2}\, p_0 \cdot p + p_0^2}{p_0^2 + \sqrt{2}\, p_0 p + p^2}$$

The proportional part of loopfilter output is generated by multiplying the phase error with a fixed factor prescribed by the loop bandwidth. For reasons of less expense the integrator was not realized by using an accumulator shift register but with an up/down counter clocked by a pulse with variable frequency. The counter is read out periodically and these data are added to the proportional part and the output of the Digital Control Unit. The sum controls the synthesizer.

The clock frequency of the loopfilter counter is proportional to the phase error A · sin and the square of the designpoint loop bandwidth B_{NLO} . This is achieved by dividing a 16 MHz fixed frequency pulse by means of rate multipliers. The first chain with 12 stages is programmed by the digital 12 bit phase error signal producing an unequally spaced pulse train, the average repetition rate of which is proportional to the programming input. The frequency is fed into a second 12 stage rate multiplier chain and is divided by $2^{12}/2^{10}/2^{8}/2^{12}$:51 according to the loop bandwidths of 1.5/6/24/76 Hz. Although the DANA-synthesizer has a frequency resolution of 10^{-6} Hz, a resolution of 10^{-4} Hz is sufficient in this loop to guarantee a negligible phase jitter contribution. Driven by a 2.3 GHz generator the receiver loop produces phase jitter values of less than 4° rms under thermal-noise-free condition for all loop bandwidths.

The acquisition of phase synchronism is achieved by sweeping the receiver center-frequency with the Digital Control Unit. The PLL is closed as soon as the frequency error disappears. To indicate this state the phasedetector output signals $A \cdot \cos\Delta\varphi$ and $A \cdot \sin\Delta\varphi$ are lowpass-filtered, squared, added and filtered again. In an adjacent thresholddetector the lock criterion is produced [3].

The AGC loop can work in a coherent or a noncoherent mode by choise. The signal level dynamic control region is 70 dB plus a 20 dB step in this region the control voltage of the AGC amplifier shows a deviation from linearity of less than 1.5 dB when working in the coherent mode. When working in the incoherent mode there will be a residual amplitude modulation of about 1 dB.

The following table I shows that the used design principles lead to a state of the art performance.

Subcarrier Demodulator Assembly (SDA). The subcarrier demodulator assembly is built according to the design: principle of the Multi-Mission Telemetry System SDA [4.5.6.]. Fully computer-controlled operation is possible because of the inclusion of an AGC and an automatic phase-lock acquisition circuitry. As in the equipment the subcarrier is demodulated before the main carrier demodulation a great flexibility in bitrates R and subcarrier frequencies f_{sc} can be achieved, although a relatively small amount of bandpassfilters is used, Fig. 5.

The SDA input is fed by the receiver broadband 10 MHz IF as well as the 10 MHz reference signal. The power level of the modulation sideband is adjusted to a fixed value with the variable gain amplifier A1. The adjustment is done either by MGC, according to modulation index or internally via an incoherent AGC loop. The amplifier output feeds three channels. The first channel provides the data demodulation, where as the second is used merely for producing the phase error signal of the phaselock indication as well as the AGC-error signal. The third channel produces the phase error signal to track the subcarrier phase.

The double-balanced mixers M1, M2, M3 are used as phase-switches controlled by the local subcarrier reference. When the loop is synchronized the whole modulation power is convoluted to the region around the 10 MHz centerfrequency producing a directly phasemodulated PSK signal. After appropriate bandpassfiltering and amplification according to the actual bitrate the analogue data are coherently downconverted to baseband by the amplitude detector CA1. If there is a phaseoffset at M1 between the phase of the received subcarrier and the local reference the baseband signal is reduced. This produces a baseband signal of the form

$$e_1 = m\,(t) \cdot R_{sc}\left(\frac{\Delta\psi}{2\pi}\right) + n_1\,(t)$$

where m (t) are the NRZ Data and R_{sc} (X) is the autocorrelation function of the subcarrier with the argument $X = \tau \cdot f_{sc}$. According to the way the signal is processed in the quadrature channel the baseband signal in it is of the form

$$e_2 = m\,(t) \cdot R_{sc}\left(\frac{\Delta\psi}{2\pi} + \frac{1}{4}\right) + n_2\,(t)$$

The phase-locked-loop of the SDA is closed via the third channel. The phase error signal is produced by the mixer M3 which is driven by the -90° phase shifted local reference already phase modulated by a data estimate m. The data estimate m is generated by video clipping the analogue baseband data. The error amplitude at the output of the coherent amplitude detector CA3 is proportional to $\left(\frac{\Delta\psi}{2\pi} \quad \frac{1}{4}\right)$. For a proper loop operation a limiter circuit has to be inserted between the phase-switch and the amplitude detector. As this limiter - apart from noise - only gets an input signal if there is a phase error it has to be treated as a soft limiter.

The phase error signal is processed in the loopfilter. It is then fed into the analogue frequency search input of a commercial DANA 7020-synthesizer (search region ± 10 Hz). The output of the synthesizer drives the phaseswitches M1, M2, M3 via a 4 : 1 divider.

During acquisition of phase lock the synthesizer frequency is swept linearly around the programmed centerfrequency. As soon as the lockdetector indicates phase coincedence the frequency sweep is switched off, holding the actual frequency offset. Now the loop is closed and phaselock is achieved. As the criterion is derived from the signal

$$e_1^2 - e_2^2 = m^2 \cdot R_{sc}\left(\frac{\Delta\psi}{2\pi}\right) - m^2 \cdot R_{sc}\left(\frac{\Delta\psi}{2\pi} - \frac{1}{4}\right) + n_1^2 - n_2^2$$

it depends on $2 \cdot \Delta\psi$, and the phase error signal is also periodic in π . So the sign of the analogue output data can be inverted. This uncertainty however is inevitable when demodulating fully modulated PSK-signals. As the noise in the lockdetector is only normalized deficiently by the AGC/MGC circuitry considerable margins are necessary in the threshold setting. This results in a diminished search rate. Under worst case conditions (8 Sps, $\frac{E}{N_o}$ = 1 dB) the acquisition time is about 20 min.

A principal drawback of this acquisition circuitry is that when the subcarrier frequency is swept only long periods of phasecoincidence are searched for. It would presumably be better to look for frequency coincidence in a first step and achieve phasecoincidence in a second. But this requires the quadrature components of a signal of which the data modulation has already been removed similar to the procedures in the phase error channel. The hardware expense however would be considerable.

Compared with a Costas-Loop smaller values of degradation can be achieved at low E/N_o -values. This is due to the remodulation procedure in the phase error channel. To reach this improvement in a realized equipment, phaserelations between the three channels must be fixed and stable over long time intervals even though IF-filters are changed.

The difficulties mentioned above were solved during the development phase. It could be avoided to put each bandpassfilters into an oven. The video amplifiers of the coherent amplifiers however had to be put into an oven to get small offset voltages. So the delivered SDAs could be included from the beginning into the computercontrolled operation of the receiving station. Table II shows the values achieved with the equipment. The stated values are pertinent to a square wave subcarrier modulated by a pseudonoise (PN) data stream. Performance degradations occur generally when the data stream is a square wave. In this case the data estimate is worse than in the PN-modulated case from which results a higher loop phase jitter caused by the increased selfnoise.

Conclusion. The synthesizer of the RF-receiver can be used for tuning as well as for phase control. It must then be possible to use the synthesizer as a numerically controlled oscillator (NCO). In this case a digital loopfilter realization is used. Instead of an accumulator an alternative solution is possible for the implementation of the loopfilter integrator. As the Digital Control Unit can be used to remove loop stress, it is possible to work with moderate by small loop bandwidths. - It would also be possible to alter the parameters of the loopfilter continuously according to missionrequirements (not implemented). The IF-interface between receiver and subcarrierdemodulator is at 10 MHz whereas the phasedetection is done at 400 kHz. So the phase of reference has to be controlled in order to get a fixed phaserelation between 10 MHz IF-signal and reference independent of the used RF carrier bandwidth. All phaseadjustments in the subcarrier demodulator are then independent of receiver programming.

In the subcarrier demodulator the RF-carrier is demodulated after the subcarrier has been removed. In the subcarrier loop datamodulation is suppressed by remodulation techniques. By these means it is possible to use the subcarrier demodulator over a very wide range of subcarrier frequencies and symbol rates. Apart from this signals with very high noise levels can be processed.

The complete receiver system can work fully automatic. For carrier and subcarrier acquisition only the following data are necessary: RF-carrier and uncertainty, the expected signal-to-noise ratio or the useful RF-loop bandwidth, subcarrier frequency and symbol rate.

Literature.

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[2] Angebotsaufforderung “Erganzung des 100 m-Teleskops der Max-Planck-Gesellschaft zum Datenempfang wahrend der Helios-Mission”, Deutsche Forschungs- und Versuchsanstalt fur Luft- und Raumfahrt e. V., Zentralabteilung Satellitenbetrieb (GSOC), 25. Febr. 1972 .

[3] R. C. Bunce: Block IV Receiver Automatic Carrier Acquisition, JPL Space Programs Summary 37-65, Vol. 11, pp. 107-116

[4] Multiple Mission Telemetry System, JPL Space Programs Summary 37-46, Vol. III, pp. 175-242

[5] M. H. Brockman: MMTS: Performance of subcarrier demodulator, JPL Space Programs Summary 37-52, Vol. 11, pp. 127

[6] M. H. Brockman: Effect of Variation in Subcarrier Loop Parameters on Telemetry Subcarrier Demodulator Performance, JPL Space Programs Summary 37-54, Vol. 11, pp. 77

Input:	frequency range	2290 - 2300 MHz;
	initial bandwidth	10 MHz;
	noise figure	7 dB
	dynamic range	-143 ÷ -53 dBm
	image suppression	≥ 60 dB
	spurious frequency suppression	60 dB

IF-Output: centerfrequency 10 MHz,
residual carrier level -55 dBm
10 MHz reference +10 dBm

RF-Phase-Locked-Loop (Designpoint 1 rad noise error at PLL)

single side noise bandwidth at design-point	1,5 Hz	6 Hz	24 Hz	76 Hz
400 kHz-IF-bandwidth	0,3 kHz	1,2 kHz	5 kHz	18 kHz
minimum stable operating condition	12	18	24	29
sweeprate for acquisition under above conditions	1,2 Hz/s	14 Hz/s	80 Hz/s	1,2kHz/s

tracking range ± 375 kHz off actual centerfrequency

phase jitter 4° rms for all loop bandwidths

AGC-loop dynamic range 70 dB + a 20 dB step
amplifier control voltage gain 7 dB/V
deviation of AGC voltage

from linearity	1,5 dB
stability	better 0,8 dB/12 h
resolution	0,1 dB
loop time constant	0,03/0,3/3 s

Table I essential receiver data

Subcarrier: frequency range	500 Hz + 1 MHz
wave form	square wave or sine
symbol rate (NRZ)	5 Sps ÷ 100 kSps
Modulation index	11° ÷ 72°
Input-IF-frequency	10 MHz
1 dB-bandwidth	10 MHz
residual carrier power	-55 dBm ± 3 dB +
sideband power	-45 dBm ÷ -72 dBm ± 3 dB
maximum input noise loading	+ 6 dBm

Phase loaked loop bandwidth at designpoint	0,03 Hz	0,37 Hz	1,5 Hz
variation due to limiter noise loading	0,01-0,35 Hz	0,37-1,7 Hz	1,5-2,6 Hz

tracking range	± 2,5 Hz off centerfrequency	
acquisition automatic mode	search region	± 250 mHz
	sweepperiod	100/25/5s
manual mode	search region	± 2,5 Hz

noise characteristics (square wave f_{sc} = 32,768 kHz)

Symbol rate	Loop-bandw.	E/N_0 /db	Frequency uncertainty	Degra-dation	Function
8 Sps	0,03Hz	-1 +1 +3 5,2	0,1 Hz 0 Hz 0,25 Hz	0,7dB 0,2dB	noise threshold limit of stable operation min value for automatic acquisition
100 Sps	0,37Hz	-1 -1 +1	0,5 Hz 0 Hz 0,25 Hz		noise threshold min value for automatic acquisition
400 Sps	1,5Hz	0 0 +2	2 Hz 0 Hz 0,5 Hz		noise threshold min value for automatic acquisition

Table II essential subcarrier demodulator data

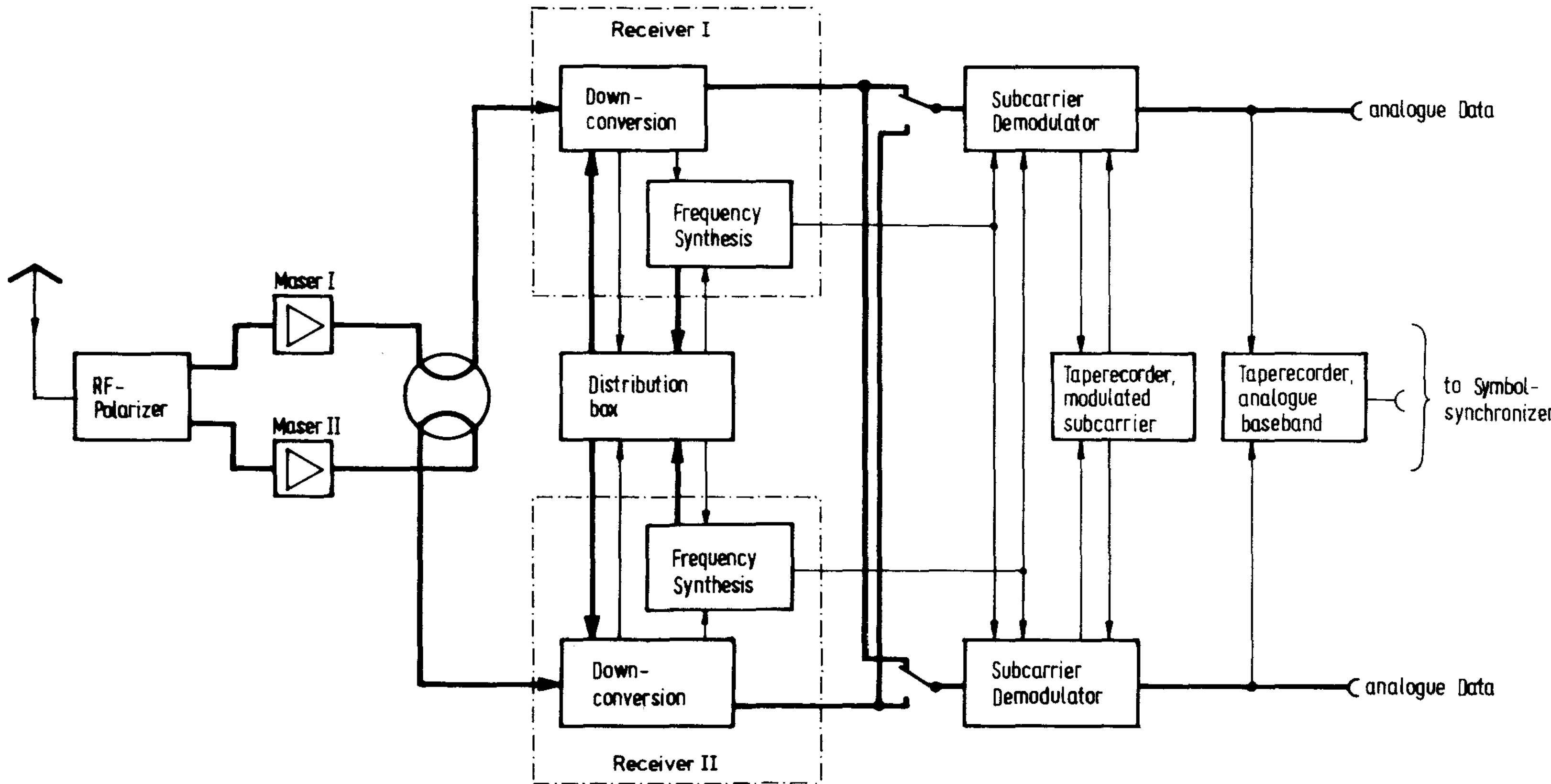

Fig. 1 Telemetry receiving system

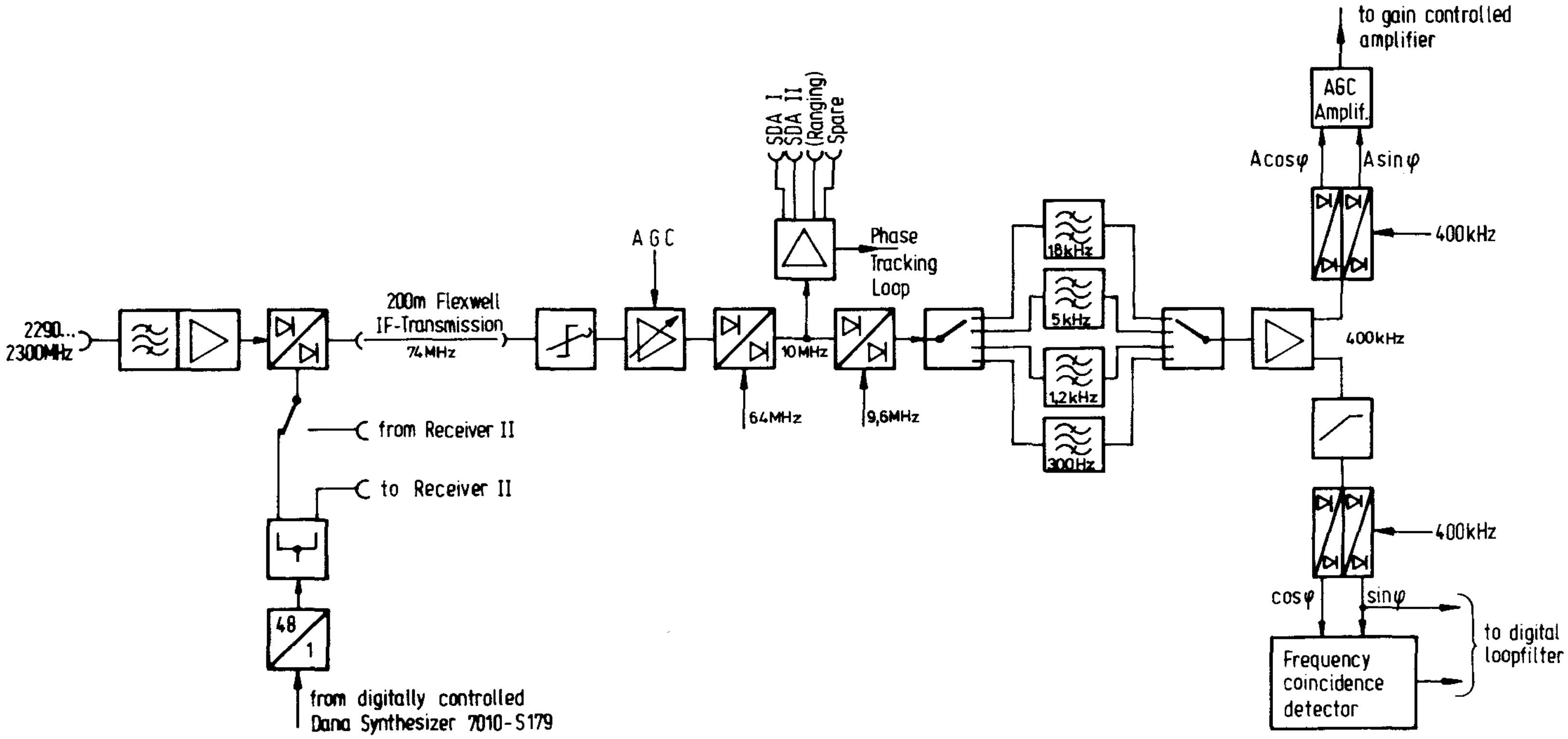

Fig. 2 S-Band telemetry receiver

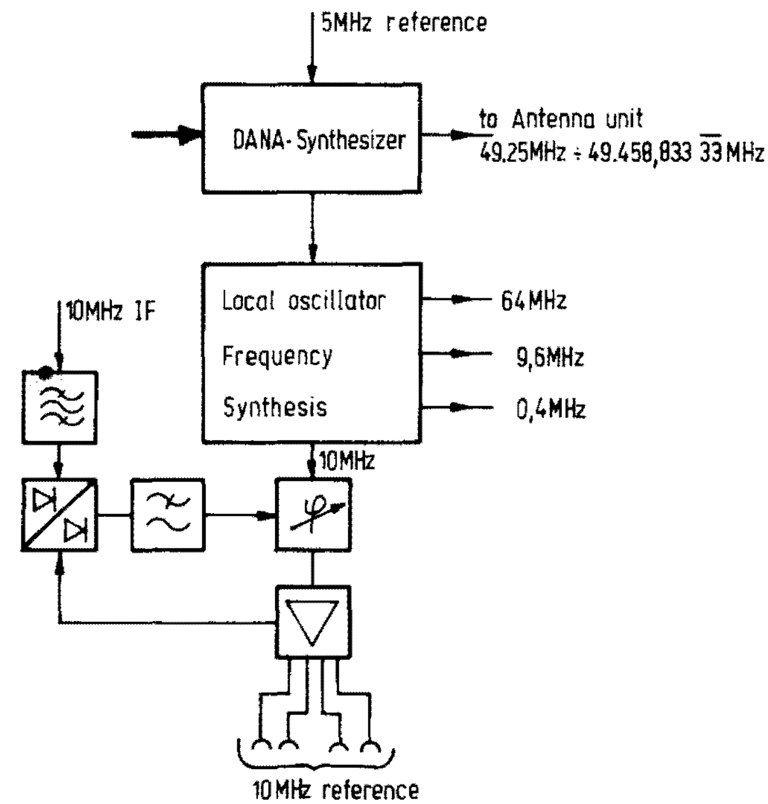

Fig.3 Local frequency generation

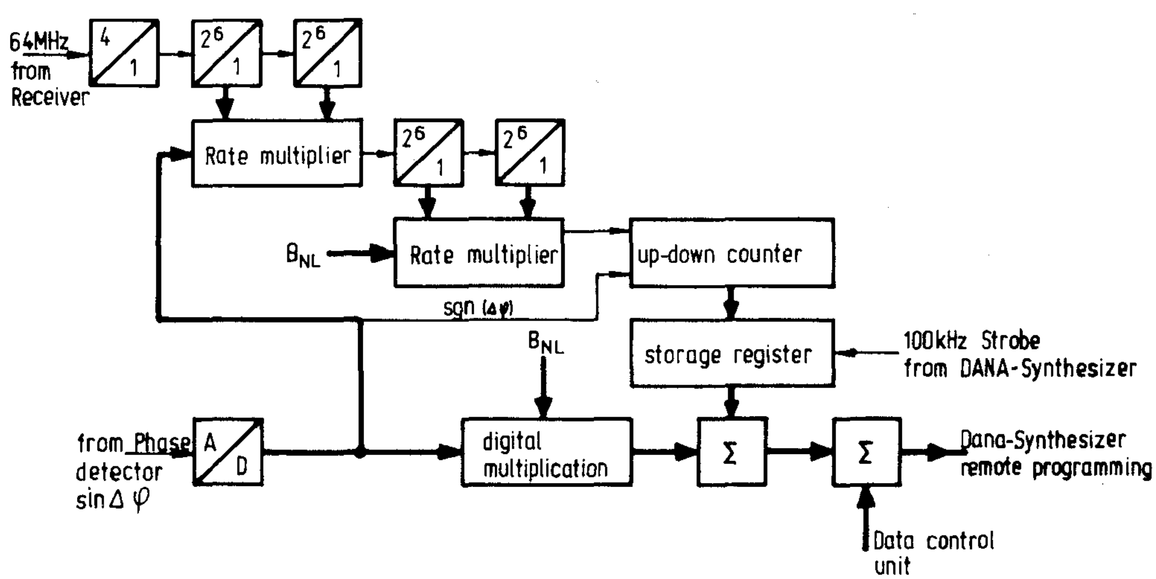

Fig.4 Digital implementation of PLL

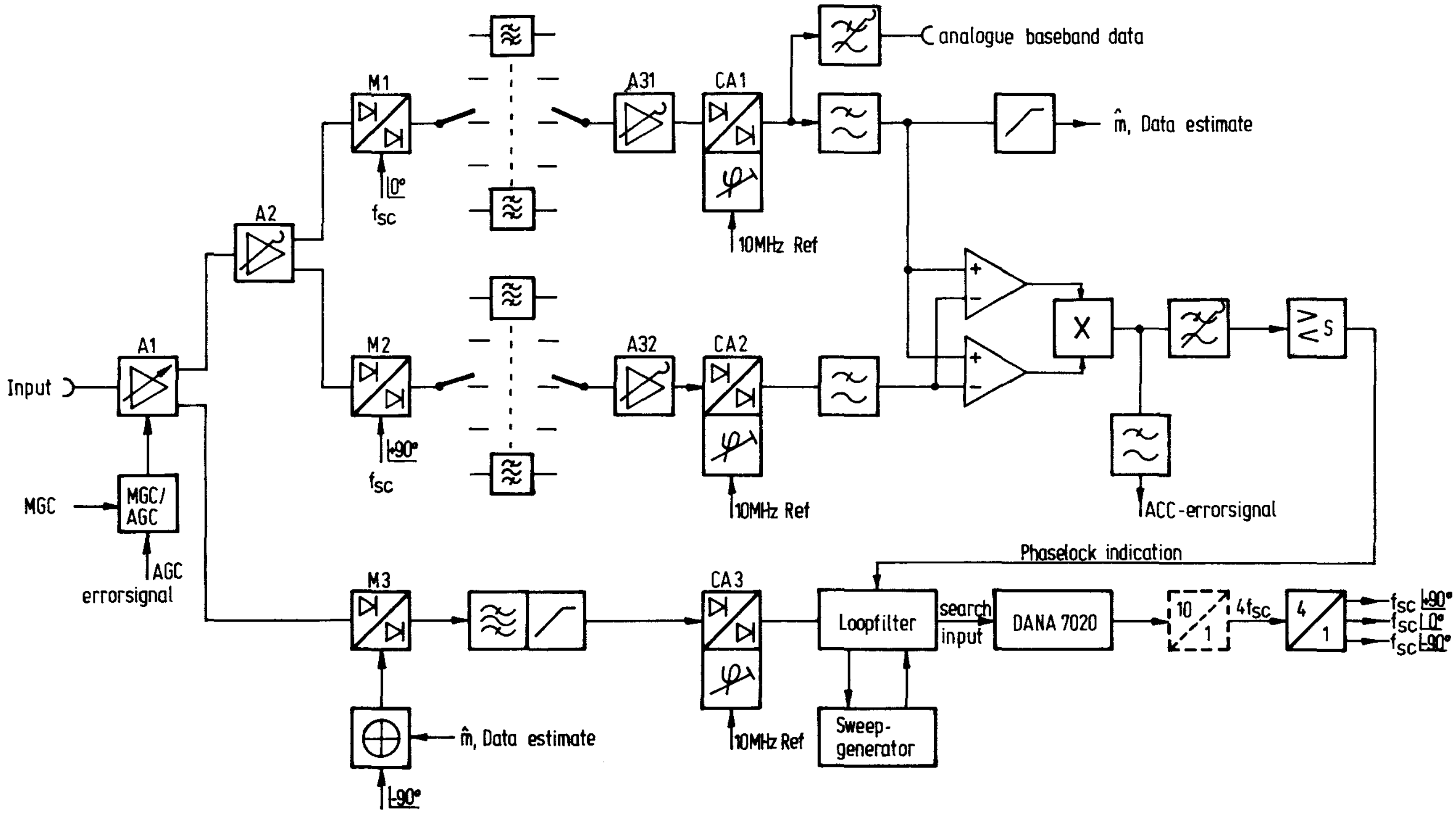

Fig. 5 Subcarrier Demodulator Blockdiagram