A CENTRAL CONTROLLER/DISPLAY SYSTEM WITH REAL TIME PROCESSING FOR REMOTE DATA ACQUISITION UNITS

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Summary A flexible Data Management and Display Unit (DMDU) has been developed as part of the On-Board Data System developed for the 40' x 80' Wind Tunnel at Ames Research Center. The DMDU can be operated as a slave to a Systems Engineering Laboratories Model SEL-840MP computer or as a standalone system receiving instructions from an operator via data terminal/keyboard inputs. It is capable of controlling the acquisition data from four data acquisition units at software selectable word rates of 250 to 125,000 words per second in increments of 50 words per second. The number of remote acquisition units can be expanded to twenty-nine units providing data point capacity in excess of 10,000 channels. Acquired data can be distributed in real time to the host computer (SEL-840MP), a bar graph CRT display (up to 128 data points), a strip chart recorder (up to 3Z data points), to one or both of two analog magnetic tape recorders (BIØ-L or DM-M format) or to a PDP-11/05 minicomputer for data processing in real time. The DMDU can be utilized as a "quick-look" playback facility for the playback and display of data previously recorded on magnetic tapes in any of the standard IRIG PCM formats. It receives initialization information consisting of the remote acquisition units and data point address, amplifier gain, each data points required sampling rate and the data output destination entered locally via punched paper tape or from the SEL-840MP computer. Resident software generates a "master sampling format" with sub-commutation and super-commutation as required. Embedded within the master cycle are the minor cycle sampling formats for the individual recorder outputs, complete with software controllable fram ‘ e synchronization patterns. Conversion from the data acquisition mode to the data playback or data reduction mode can be performed dynamically under interrupt control.

Introduction. NASA's Ames Research Center, in an effort to increase the efficiency of its 40' x 80' wind tunnel, as described by Finger and Cambra (1), contracted with Teledyne Controls under Contract NAS2-7727 to develop a computer controlled wind tunnel data acquisition system. This system, known as the "On-Board System" or OBS, consists of two (2) primary elements. One major element is the Remote Multiplexer/Demultiplexer Unit (RMDU) which performs data point selection, signal conditioning and transducer excitation. The RMDU described by Trover (2) is located in the aircraft in the tunnel. The

second major element of the OBS is the Data Management and Display Unit (DMDU) which is located in the wind tunnel control room and is the subject of this paper.

Due to the wide variety of tests that are performed on a model in the wind tunnel, and the wide spectrum of models tested, the data acquisition system (DMDU) had to be designed with a great amount of built-in flexibility. That is, it must have the ability to readily change data sampling formats (sampling rates), change the display of selected parameter's, gather data from multiple sources and operate as a slave or standalone system. The DMDU will operate either as a slave to the 40 x 8''s main computer, a Systems Engineering Laboratories Model SEL- 840MP in the "On- Line Mode" or as a standalone data system in "Off- Line Mode" whereby all machine functions are controlled locally by an operator. In either mode of operation, the DMDU controls the acquisition of data from the RMDU(s) or other (foreign) PCM Systems in the model and outputs the acquired data to any one of six (6) output devices.

All key system parameters are under software control of the DMDU's PDP-11/05 minicomputer. The storage medium for the data acquisition sampling format is a 4096 word x 18 bit semiconductor random access memory (Format Memory), while the main memory consists of 28K words x 16 bit core RAM. The format memory can accommodate a single data cycle of approximately 2000 data points or multiple data cycles of smaller size. For future expansion, or to satisfy requirements for increased data cycle sizes, the storage capacity of the Format Memory can be incrementally expanded to 16K words by the addition of up to four standard 4K word memory modules. When multiple sampling formats are stored in the Format Memory, the DMDU can switch formats in less than 80 microseconds by software command from the PDP-11/05 minicomputer, thus dynamically changing the system configuration to meet changing test conditions.

Since Ames Research Center has an investment in existing data acquisition equipment, it was necessary for the DMDU to simultaneously accept data from both RMDU's and existing PCM equipment, which may be installed in the models, in any one of the standard IRIG formats and merge the data with the data from the OBS On-Board Units. To satisfy requirements for widely varying data acquisition rates, the DMDU has been designed to provide a master data cycle for data acquisition with the capability of outputting either the master data cycle and/or minor data cycles at semi-asychronous word rates to the destination devices. Master data cycle flexibility is achieved by a software controllable time base generator in the RMDU controller which incorporates a "phase-locked-loop" word rate generator. The RMDU controller can output addresses to the RMDU's and accept data words from the RMDU's at word rates from 250 WPS to 125,000 WPS in increments of 50 WPS, for a total of 2496 different word rates selectable by software command from the DPD-11/05 minicomputer. The master data cycle (RMDU) word rate

or data acquisition rate can be changed dynamically during a test run to increase or decrease data acquisition rates during critical test phases.

Input initialization data for the DMDU may be received from either the SEL-840MP computer or locally entered thru the DMDU paper tape reader/ punch. Initialization data consists of RMDU address, RMDU card select, channel select, amplifier gain, required sampling rate and data destination. From this basic requirements list, the format generation software system assembles a standard PCM sampling format and produces a punched paper tape of the format memory contents as an archivable record. The sampling format is stored in the format memory section of the DMDU and is accessed by the RMDU controller for transmission of data point addresses in serial format to the RMDU's in the model. The DMDU is presently mechanized to control four RMDU's (two will be delivered with the system). The system can be expanded at any time to a maximum of twenty-eight remote units bythe addition of up to six additional RMDU I/O assembly boards, each of which can control four RMDU's. Expanded to its full capacity, it is possible for the DMDU to direct data acquisition from nearly 10,000 different data points or transducers.

Information stored in format memory consists of the previously mentioned data point specifiers, output port destination control information and pointers to the next words to be fetched from format memory. Acquired data are outputted to any or all of up to six destinations. The present destination units include two display devices, (1) a bar graph CRT display where up to 128 data points can be displayed, in unipolar or bipolar PAM format and (2) a digital to analog converter where up to 16 data points can be displayed on a strip chart recorder (expandable to 32 channels with the addition of DAC modules). In addition to the real time displays, data can be routed to two different magnetic tape recorders (or parallel tracks of the same recorder) with individually programmable word rate and word length controls, to the SEL-840MP (block transfer), and/or to the PDP-11/05 for real time computation. Data points outputted to the bar graph and strip chart recorder are displayed in real time and the selection of data points to be displayed can be changed during a test by software command from the PDP-11/05 minicomputer. This change can be initiated by the system operator via the CRT/Keyboard terminal.

Either the master data cycle or minor data cycles (or both) can be outputted to one or both of two analog tape recorder ports for recording in either BI∅-L or DM-M code. Each recorder output port has a unique standard PCM data cycle which may, or may not be related to the major data cycle of the RMDU controller. Each recorder controller's minor data cycle however is synchronized to the RMDU controller data cycle by the "end of cycle" signal from the RMDU controller. Thereby, the common time denominator between the RMDU controller and each analog recorder port is the master cycle rate of the RMDU controller. The word rates of the recorder ports are simply the master "cycle rate"

multiplied by the number of words out of the data cycle that are recorded on that recorder track. Each recorder port has subcommutation and super commutation capability with frame synchronization patterns software programmable and is semi-synchronous in relation to the other recorder port and/or the RMDU controller.

The capability of having an asynchronous (or semi-synchronous) relationship of acquired data to data distributed to an individual output device required some means of data buffering. Original system concepts had the output data buffered in portions of the PDP-11/05 minicomputer memory for each output device. Detailed timing analysis revealed that during worst case conditions, up to 95% of real time would be required for data transfers into and out of the PDP-11/05 memory, leaving little or no time or rea time data processing and system “housekeeping chores”. As a result of this undesirable condition, the concept of a separate output data bus and a “first in - first out” (FIFO) data buffer for each output device evolved. This separation of data acquisition from system control enables the PDP-11/ 05 to be occupied with meaningful tasks during the acquisition of data. The output bus structure of the DMDU permits any type of output device or peripheral to be utilized with the DMDU as long as the peripheral meets the generalized I/O requirements of the output data bus. The significance of the dual bus concept (the output data bus plus the PDP-11/05 Unibus) is that additional analog recorders, or multiple tracks of a single recorder can be used to distribute the acquired data thus reducing recorder bandwidth requirements and/or increasing record time capacity, while leaving over 90% of the PDP-11 Unibus time available for data processing. A block diagram of the DMDU is presented in Figure 1, and Figure 2 is a photograph of the DMDU.

System Operation The DMDU requires a certain amount of operator-machine dialogue whether it is in the On-Line mode as slave to the SEL840MP computer, or in the Off-Line mode as a standalone data acquisition system. The principal device for this operator-machine dialogue is a video display CRT for displaying system status and requesting inputs of the operator and a standard Teletype T type of keyboard for operator commands and responses. When DMDU power is turned on, the system requests a definition of operational mode from the operator, i.e., Off-Line or On-Line mode. If the operator types in On- Line, the DMDU then looks to the SE L840MP computer for further control via the Control Word interface. The SEL-840MP then commands the DMDU to start accepting a table of initialization data that contains the previously mentioned data point specifiers, required sampling rates, data destination points and a definition of “foreign PCM” if any. The SEL-840MP computer then commands the DMDU to echo back this table of initialization data as a verification of valid data transfer. The SEL-840MP then transmits a second list of data point specifiers which are in the opinion of the operator bad channels, i.e., malfunctioning transducers, etc.

For Off-Line operation, the table of initialization data is inputted via the DMDU's punched paper tape reader and the list of bad channels is inputted by the operator via the operator's keyboard. For either mode, the DMDU then asks via the operator for a definition of whether or not there is also foreign model PCM (other data acquisition units than RMDU's). Foreign PCM setup data consists of information required to control the EMR Model 720 Bit Synchronizer and EMR Model 2731 Frame Synchronizer under computer control, i.e., bit rate, frame (word) rate, frame length, word length, PCM code (BIØ-L, DM-M, etc.), frame synchronization pattern, etc. The operator then enters the required data via the operator keyboard. At this juncture a foreign PCM program tape can be created for future setups of the same type of test. The DMDU then requests of the operator information defining which channels are to be outputted to the Bar Graph Display and the Digital to Analog Converter. The operator responds accordingly.

Finally, the DMDU then generates a standard PCM sampling format (Figure 4) for the RMDU controller with super-commutation and subcommutation as required. The software format sampling generation program thus relieves the operator of the tedious trial-and-error method of generating a sampling format. The DMDU is then ready to enter the Data Gathering mode and start acquiring and disseminating data as defined by the sampling format. The SEL-840MP can at this time command the DMDU to enter the static standardization, static calibration, static data collection or dynamic data collection modes of operation as described by Finger and Cambra (1).

DMDU Functional Description The DMDU is divided into four functional elements. These are; (1) the Central Processor Unit (CPU) and it's associated peripheral devices (station control, data processing and data input - output), (2) the RMDU Controller, (3) the Format Memory and, (4) the Output Data Buffers, controllers and display devices (recorders, digital-analog converters and bar graph display) including the "Foreign PCM" loop (bit synchronizer and frame synchronizer).

CPU and Peripherals The central processor unit selected for the DMDU is the Digital Equipment Corporation Model PDP-11/05 minicomputer. The PDP-11/05 is a 16-bit general purpose parallel logic, 2's complement arithmetic computer whose instruction set lends itself to control functions. The PDP-11/05 instruction set consists of 45 basic instructions which when modified by the byte mode and the different addressing modes expand to over 400 instructions. The PDP-11/05 features eight hardware general registers, push-down, pop-off stack processing, automatic priority interrupts, hardware vectored interrupts, direct addressing of up to 32K words of core memory, direct memory access for maximum data transfer rate and automatic power-fail restart. As in the basic DMDU design, the capability for modular expansion was a "must" requirement in the selection of a CPU. Due to the unique "Unibus" T structure of the PDP-11/05 the capability of the CPU can be expanded simply by the addition of peripherals on the Unibus. This expansion

can include hardware arithmetic units which decrease the time required for multiply and divide operations, a disk memory for program storage and "Disk Operating Systems" software, a digital magnetic tape system for mass record storage, and a high speed line printer for data dumps. Available software support for the PDP-11 /0 5 include s a macro assembler, an editor, an on-line debugger program, floating point math routines, and a complete set of hardware diagnostics.

The PDP-11/05 through its software program controls all of the DMDU operation. Then in the On-Line mode, the PDP-11/05 interprets and responds to instructions from the 40 x 80's SEL-840MP computer, and when in the Off-Line mode it interprets and responds to instructions entered by the operator via the CRT/Keyboard.

The DMDU input-output devices are the high speed paper tape reader/ punch and the CRT/Keyboard. The CRT/Keyboard is the Model H-2000 manufactured by Hazeltine Corporation. It has a display area of 27 lines x 74 characters (a total of 1998 characters) with an update rate of up to 960 characters per second. The PDP-11/05 through the system software displays primary system parameters, system error messages, operator prompts and monitors selected data points on the video CRT.

The high speed paper tape reader/punch is the Digital Equipment Corp. Model PC-11. It can read a paper tape at rates up to 300 characters per second and punches a tape at rates up to 50 characters per second under software control. The PC-11 paper tape reader is used for loading the system software program into core memory, and inputting initialization data for the format generation program. The PC-11 paper tape punch is used to output the results of the format generation program when in the Off-Line mode. The information contained on the punched paper tape is a mirror image of the data in the Format Memory and information defining the RMDU Controller bit rate and word rate, and Recorder Controller bit rate and word rate. When the format generation program is used for programming of the EPROM's used on the RMDU Stand Alone Timing Module, the PC-11 paper tape punch outputs four different paper tapes to be used by the DATA I/O Model PROM Programmer.

RMDU Controller and Format Memory. The RMDU controller operates in one of two modes under software control of the PDP-11/0 5. The software system, via the proper commands, can cause the RMDU Controller to; (1) continuously acquire and disseminate data, (2) to acquire and disseminate (or store in mainframe memory) a complete signal scan of data or, (3) to acquire and disseminate (or store in mainframe memory) a single frame of data.

The RMDU Controller, as shown in Figure 4, consists of five functional areas; the format memory read logic, bit rate and word rate generator, RMDU address transmission logic,

RMDU out ut data logic, and the data/ control registers. The Format Memory read logic consists of a mainframe address register, a mainframe address counter, a subfrarne register, subframe address counter, read address multiplexer and control logic. The mainframe address register and subframe address register are loaded via system software command from the PDP-11/05 with the Format Memory address of the first word of the mainframe format memory map and the first word of the subframe memory map respectively. At the start of a typical data acquisition cycle (see Figure 5), the contents of both registers are clocked into the mainframe subframe address counters. The read control logic then initiates a memory cycle from Format Memory and multiplexes either the mainframe address counter or the subframe address counter to the format memory. As Control Word 1 and 2 are transferred from Format Memory to the RMDU Controller logic, the selected address counter (MF next or SF next) is incremented to point to the next word to be read from Format -Memory. Bits 5 and 6 of control word 2 determine section of Format Memory (i.e., subframe or mainframe) is accessed for the next pair of control words. At the end of each mainframe of the “master data cycle”, the mainframe address counter is reloaded with the contents of the mainframe address register which points to the first two control words in the mainframe memory stack. At the end of the last frame of the “master data cycle” both the mainframe and subframe address counters are reinitialized with the address of the beginning word(s) of both the MF and SF memory stacks.

Upon completion of the generation of the sampling format generation program, the PDP-11/05 CPU under software control writes the sampling format into the format memory. A sampling format consists of two words of memory per data point. As shown in Figure 6, Control Word Number 1, bits 2-5 specify 1 of 11 cards and bits 6-9 specify 1 of 8 RMDU amplifier gains, per RMDU to be addressed, while bits 10-15 specify 1 of 32 channels on the selected card. Control Word Number two bits 0-5 specify 1 of 29 RMDU’s to which Control Word #1 is to be transmitted. RMDU addresses 30-32 are special overhead addresses used internal to the RMDU Controller to be described later. Bits 10-15 of Control Word two are used to steer the data acquired from the data point defined by Control Word one to the desired output device. In addition, there are three spare overhead bits on Control Word two for system expansion, i.e. , additional output devices. Figure 5 also provides correlation of bit assignment vs. output device. It should be noted that an acquired data point value can be sent to anyone or all six output devices simultaneously. As previously stated, bits 5, 6 are used as pointers by the RMDU Controller to define the source of the next two control words to be fetched from the Format Memory.

The acquisition of a data word from the RMDU is a five word time cycle, During word time one, Control Words 1 and 2 are fetched from Format Memory. During word time 2, Control Word 1 is transmitted in serial fashion to the selected RMDU. Word times 3 and 4 are consumed by the RMDU for interal processing (data point multiplexing and analog to

digital conversion). The RMDU then transmits the data word to the RMDU Controller during word time 5. In the RMDU Controller the received data word is adjusted for autoranging (if is occurred) and outputs the data to the devices specified by Control Word 2.

The Format Memory is organized as two 4096 words x 9 bits/word sections. Each 9-bit word is composed of eight data bits plus an odd parity bit, thus there are 16 data bits per word. The memory is a dynamic semiconductor memory with an access time of 800 nsec. requiring refreshing of the data in memory at a 500HZ rate. All refresh circuitry is built into the memory and is invisible to the using device, The memory is functionally organized into two sections, Mainframe Format Memory and Subframe Format Memory (see Figure 7). This memory organization is a dynamically changing organization and varies from test to test as the required sampling format changes. In addition, there may be more than one sampling format in the Format Memory during a test and the RMDU Controller can switch from one format to another (within 80 psec) under software command from the PDP-11/ 05 minicompute r.

During the 1st word period the RMDU Controller fetches Control Words one and two from Format Memory, transmits Control Word one (in serial format) to the selected RMDU encoded in control word two's field. Control Word two is then delayed two word periods through a series of parallel shift registers until the data word is returned from the RMDU. The RMDU controller shifts the returned data word to account for GPA autoranging in the RMDU and outputs the CT corrected data word to the destinations designated in Control Word two.

The basic unit of frequency in the RMDU Controller is the RMDU bit rate clock which is divided by twenty to generate the RMDU word rate clock. The word rate clock determines the rate at which data point addresses and data are transferred between the RMDU Controller and the RMDU's (i.e., the data acquisition rate). The clock frequency is synthesized via a digital phase locked loop from a basic frequency of 1 KHZ. This 1 KHZ frequency multiplied by a software programmable frequency multiplier to generate a high frequency internal clock of 5.0 - 10.0 MHZ. This 5.0 - 10.0 MHZ internal clock is divided by 4 to generate the 1.25 - 2.5 MHZ RMDU clock. The 1.25 - 2.5 MHZ clock is further divided by 20 to generate the basic RMDU clock of 62.5 KHZ to 125 KHZ.

The word clock of 62.5 KHZ to 125 KHZ is further divided by a software programmable divider to generate word rates of less than 62.5 KHZ for slower data acquisition rates. An algorithm has been developed for use by the system software in programming of the bit rate and word rate generator. It is WORD RATE = $50xN\ ^{1}/_{M}$, $1250 \leq N \leq 2500$, $1 \leq M \leq 256$. This results in data acquisition rates of 250 WPS 125,000 WPS in software selectable increments of 50 words per second.

When Control Word #1 (the RMDU address word) is read from format memory it is loaded into a parallel shift register. At the beginning of the next word time the RMDU address is transferred to a parallel to serial output register and clocked onto the RMDU address line through the output gating logic. The address and clock information is coupled to the communication cable line drivers through optical isolators thus guaranteeing total DC isolation between the DMDU and the RMDU (which can have a 208V potential differential). The RMDU's can be located up to 250 feet from the DMDU. As previously stated, the DMDU transmits an address to the RMDU and the RMDU returns a data word to the RMDU Controller. Due to the possibility of widely variable distances between the DMDU and any one RMDU, the phase shift (propagation delay) in the transfer of data from the RMDU Controller to the RMDU can vary from I bit time to 4 bit times (depending upon bit rate and cable length). To insure the integrity of the returned data, all received data is resynchronized to the internal RMDU controller clock with a digital resynchronizer. Once the returned data word has been received, the "gain tag" bit is tested. If the "gain tag" is set to a logic "1", indicating that autoranging has occurred in the GPA of the RMDU, the RMDU Controller shifts the data word to compensate for the decrease in amplifier gain. Data is then transferred to the output data register from which it is strobed via the output data bus into the output devices which are enabled by the control word to accept the data word.

To provide a means of testing system operation, exclusive of RMDU's, internal self-test logic has been built-in to the RMDU Controller. When control words are fetched from Format Memory with an RMDU address of $35_{(8)}$, the address is shifted to a special test register and then gated to the input data stream where it can be outputted to any one or all of the output devices including the PDP-11/05 minicomputer for error checking. Additionally, a means has been provided to insert computed data values from the CPU in the data to be recorded on the analog recorders. Any pair of control words fetched from Format Memory with an RMDU address of $36_{(8)}$, is treated as a data word to be inserted in the output data stream and can be routed to any output device on the output data bus.

FIFO Buffer Memory. Data from the RMDU's being transferred to the output devices via the output data bus, more often than not, is outputted asynchronously in data bursts while the using device (bar graph display, digital to analog converter, analog recorder, etc,) must access the data at a fixed synchronous rate. The data being transferred from the RMDU Controller to a destination device is stored in "first in - first out" FIFO buffer memories. These FIFO memories accept the even or uneven data input rates from the RMDU Controller and output the data to the using device at a continuous but slower data rate (assuming only part of the master data cycle is being sent to any given destination device). Each output device connected to the output data bus has its own FIFO buffer memory. The size of the buffer memory varies with each output device from 64 words by 12 bits for the DAC channel to 3088 words x 16 bits for the SEL-840MP FIFO buffer

memory. Each output devices' FIFO buffer memory is an expansion of the basic memory element which is a MOS semiconductor 64 word x 4 bit FIFO memory integrated circuit (Figure 8). The FIFO memory integrated circuits can be connected in series to produce memories of an increased number of words, and can be expanded in parallel to generate memories of any word length. The maximum data transfer rate into or out of the FIFO memories is 500 KHZ.

Bar Chart Display. Any data point computed data value or foreign PCM data point, up to a maximum of 128 data points, can be displayed in histogram form on the Bar Chart display. These data points can be displayed as two's complement numbers with the most negative value at the base line and the zero data value at the mid-point of the display or as positive values only with the zero data value point at the bottom of the display (switch selectable on the display). The Bar Chart Display system consists of a 190 word x 12 bit FIFO buffer memory and control electronics, an EMR Model 2759 Bar Chart Driver and a HP1300A Bar Chart CRT Display Unit.

Data on the output data bus of the RMDU Controller is strobed into the FIFO buffer when the destination bit Z3 of Control Word 2 for that data point is set to a logic one. The EMR Model 2759 Bar Chart Driver then accesses the data stored in the FIFO buffer and converts the 8-bit binary number to an analog value applied to the vertical sweep circuits of the HP1300A Bar Chart Display. Data can be displayed at a maximum rate of .5Hz/ channel in the worst case condition when there are 128 channels displayed and all are at maximum value of 28 of $256_{(10)}$.

Digital to Analog Converter System. Any data point, computed data value, or foreign PCM data point, up to 16 channels (expandable to 32 channels) can be outputted to the digital to analog conversion system for application to a strip chart recorder in real time. The DAC system consists of a 64 word x 12-bit FIFO buffer memory, control electronics and an EMR Model 2750 DAC controller with 16 8-bit DAC's (the 2750 capacity can be expanded to 32 channels by the addition of DAC modules). The 8MSB's of data on the RMDU Controller output data bus is strobed into the FIFO buffer if destination bit (Z2) in Control Word 2 for that data point is set to logic one. These 8MSB's are combined with a 5-bit address counter to form a 13-bit word for outputting to the DAC where bits 0-7 are the data to be displayed in two's complement form and bits 8-12 specify the channel of the DAC Controller on which the data is to be displayed. The maximum update rate for the DAC's is 500 KHZ/channel.

Recorder Controller. In order to produce an archivable record of all events of a test in the 40' x 80' wind tunnel, all data acquired from the RMDU's and "foreign PCM" are recorded on a fourteen track analog tape recorder. The foreign PCM, already in a standard

IRIG format, is recorded directly on the magnetic tape recorder while data acquired via the RMDU's must be coded to a standard IRIG form.

The Recorder Controller (see Figure 9 for block diagram) performs three functions. The FIFO buffer memory (500 words x 16 bits) temporarily stores the data words acquired by the RMDU's to account for time gaps created by differences between the master data cycle contents and that of a minor data cycle going to one of the recorder controllers (assuming that not all data points in a master cycle are programmed to go to one recorder controller). Data words are fetched from the FIFO buffer at a constant word rate (i.e., recording rate) to the PCM Encoder. This constant recording rate is generated by the Recorder Controller Word Rate and the Bit Rate generators. The Word Rate Generator is a phase locked loop frequency synthesizer whose reference or input frequency is the "master cycle rate" pulse from the RMDU controller. In order to guarantee synchronism of the recorder (minor) data cycle rate and the RMDU controller major data cycle rate, (i.e., insure a continuous stream of data to the analog recorder) the relationship of MCR = RCR must be satisified where MCR = RMDU Controller master cycle rate and RCR = recorder data cycle rate. This is insured by multiplying the MCR times the number of words from the master data cycle to be recorded in a digital phase locked loop to generate the recorder word rate (RWR). Or the relationship is then RWR = MCR x N where N = the number of words in a recorder data cycle mainframe. If there is sub-commutation, a subframe ID word must be included and the equation is then RWR = MCR x (N + 1). This word rate is then used as the reference frequency to an additional phase locked loop whose output is the recorder bit rate. The recorder bit rate (RBR) is relates to the word rate by RBR = RWR x M where M = the recorded word length in number of bits. This ultimate relationship for the recorder bit rate is RBR = [MCR x (N + 1)] M. The output of the word rate generator is used to transfer data words from the FIFO buffer output port to a parallel to serial shift register where to clock pulses generated by the recorder controller bit rate generator shift then out to the PCM encoder. The PCM encoder converts the NRZ-L output of the serial shift register to either BIV-Ø or DM-M code (jumper selectable on the recorder controller board). The recorder controller generates bit rates of 2.4 KB/S to 1.5 MB/s and can output data words of from 8-12 bits per word at word rates between 250 WPS and 125,000 WPS all under software selectable control in 50 WPS increments.

Foreign PCM. Non RMDU generated PCM data in any standard IRIG format or RMDU recorded data played back from the magnetic tape recorder (non-real time) can be applied to the DMU for display purposes (i.e., quick look) or for merging with RMDU data for transfer to the SEL840MP computer. This acquisition of foreign PCM is entirely under software control and can be dynamically selected from any one of four input sources. When the foreign PCM loop is used as a playback or quick look facility, selected data channels can be outputted to the Bar Chart Display subsystem or the Digital to Analog Converter subsystem for outputting to a strip chart recorder. When used for data

acquisition in real time the foreign PCM is transferred to the PDP-11/05 mainframe memory by direct memory access (DMA) where it is stored until commanded to transfer it to the SEL-840MP computer.

The foreign PCM subsystem consists of an EMR Model 720 Bit Synchronizer, an EMR Model 2731 Frame Synchronizer and an EMR Model 2763 Unibus Interface. All setup parameters for the Foreign PCM subsystem are under software control of the PDP-11/05 computer. During the initialization phase of system operation, the system operator enters into an interactive dialogue with the DMDU cia the CRT/keyboard. One of the setup tasks is the initialization of the Bit and Frame synchronizers which are controlled by a control format stored in PDP-11 memory. The initialization dialogue is a command/response interaction between the DMDU and the operator is setting up control parameters including: data bit rate (1 BPS - 5.0 MBPS), data input code (NRZ-L, NRZ-M, NRZ-S, BI0-L, BI0-M, BI0-S, RZ, DM-M and DM-S) tracking range (1%, 3%, or 10% of bit rate), frame sync pattern data word length, number of words per frame, etc. These parameters can be different for each of the four foreign PCM sources and can be changed dynamically to sequentially scan the four foreign PCM sources.

Software. Software for the DMDU consists of initialization software, calibration software, on-line operational software, off-line operational software and format generation software. All software has been designed for interactive dialogue between the CRT/ keyboard operator and the DMDU. The format generation program converts an English language parameter list to a PCM sampling format for either the DMDU format memory or for the EPROM memory of the Standalone Timing Module (SAT-M) of the RMDU The format generation program produces a paper tape of the format memory contents (four separate tapes for the SAT-M PROM programmer). If a line printer is added to the DMDU the format generation program can also print out a graphics presentation of the Sampling Format plus a word by word binary printout of format memory contents. Punched paper tapes of all software test programs can be produced to give an archivable record of all test programs.

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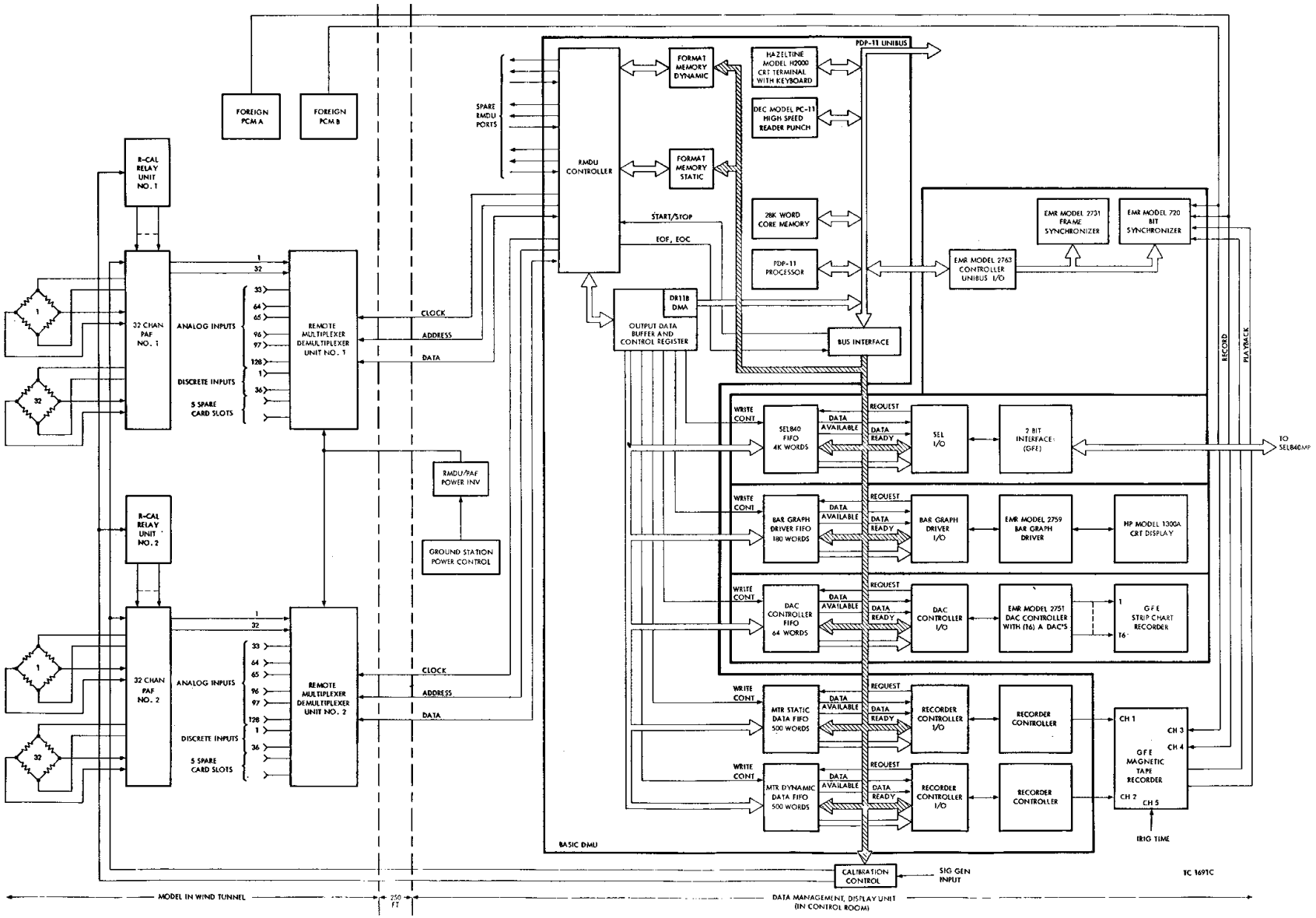

Figure 1. OBS Data Management & Display Unit

Figure 2
40' x 80' OBS Data Management & Display Unit

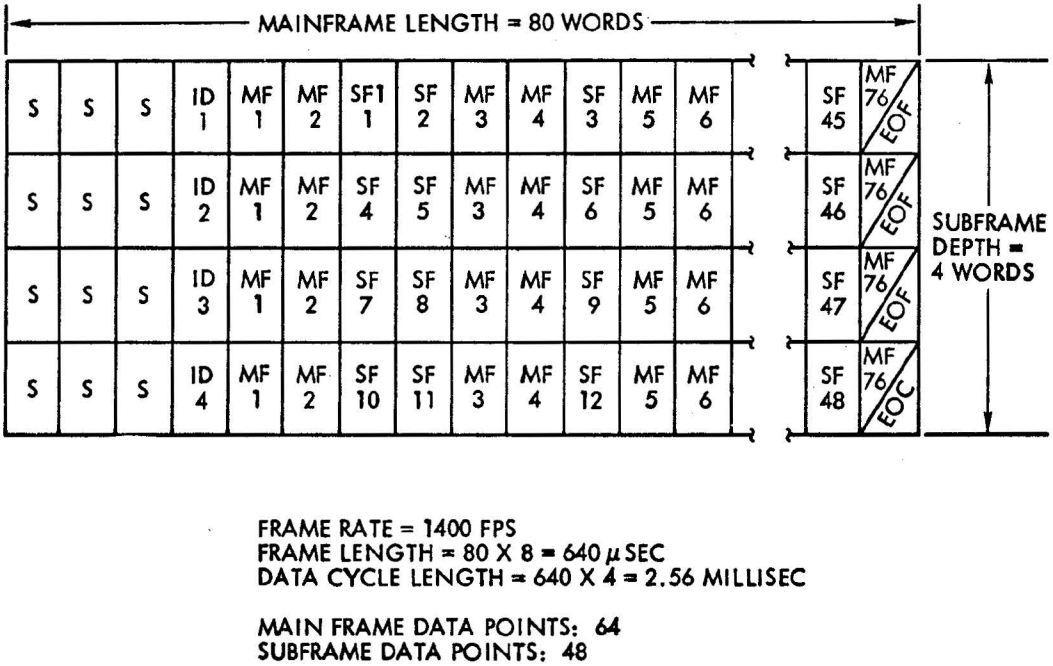

Figure 3. Typical Software Generated PCM Sampling Format

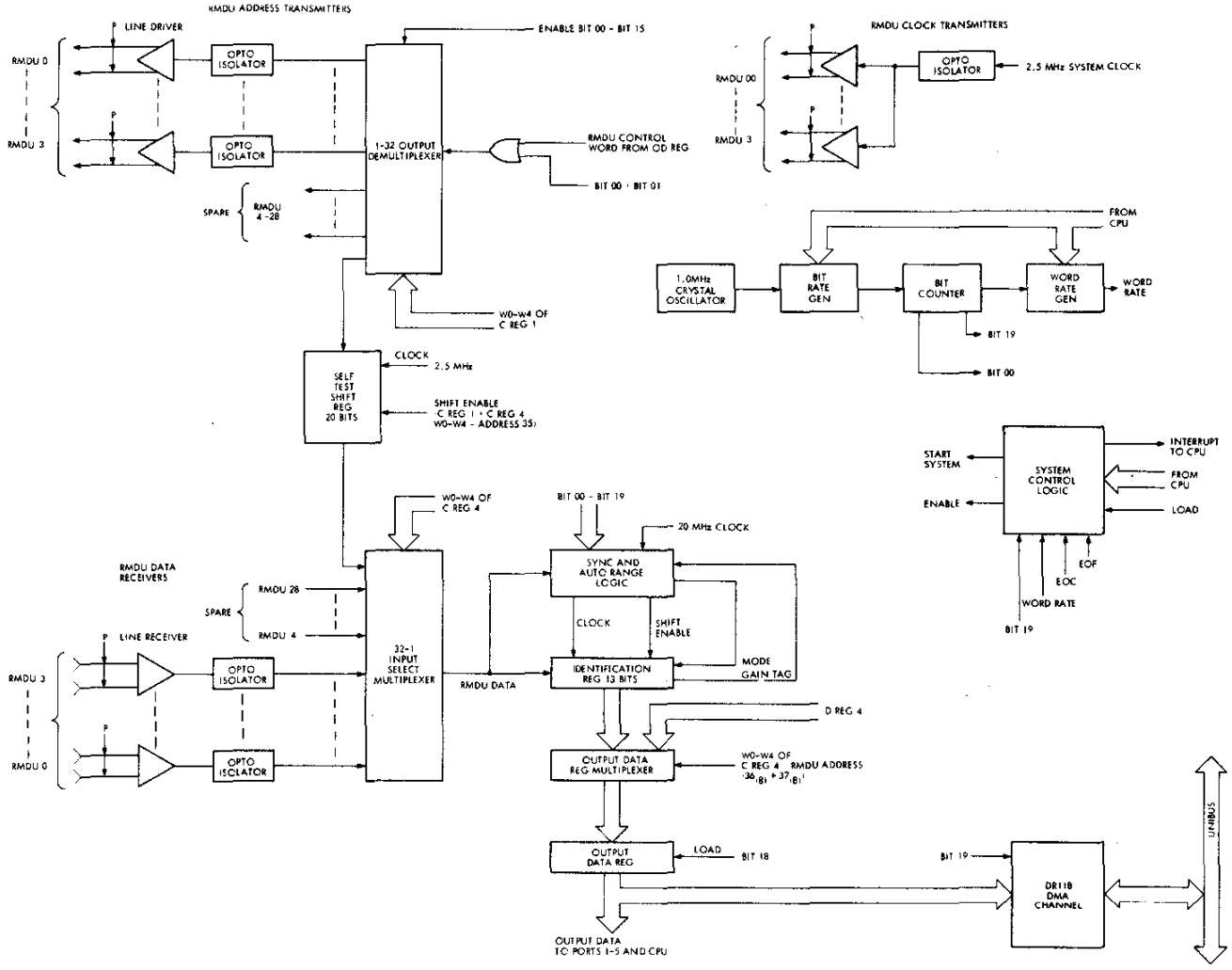

Figure 4. RMDU Controller

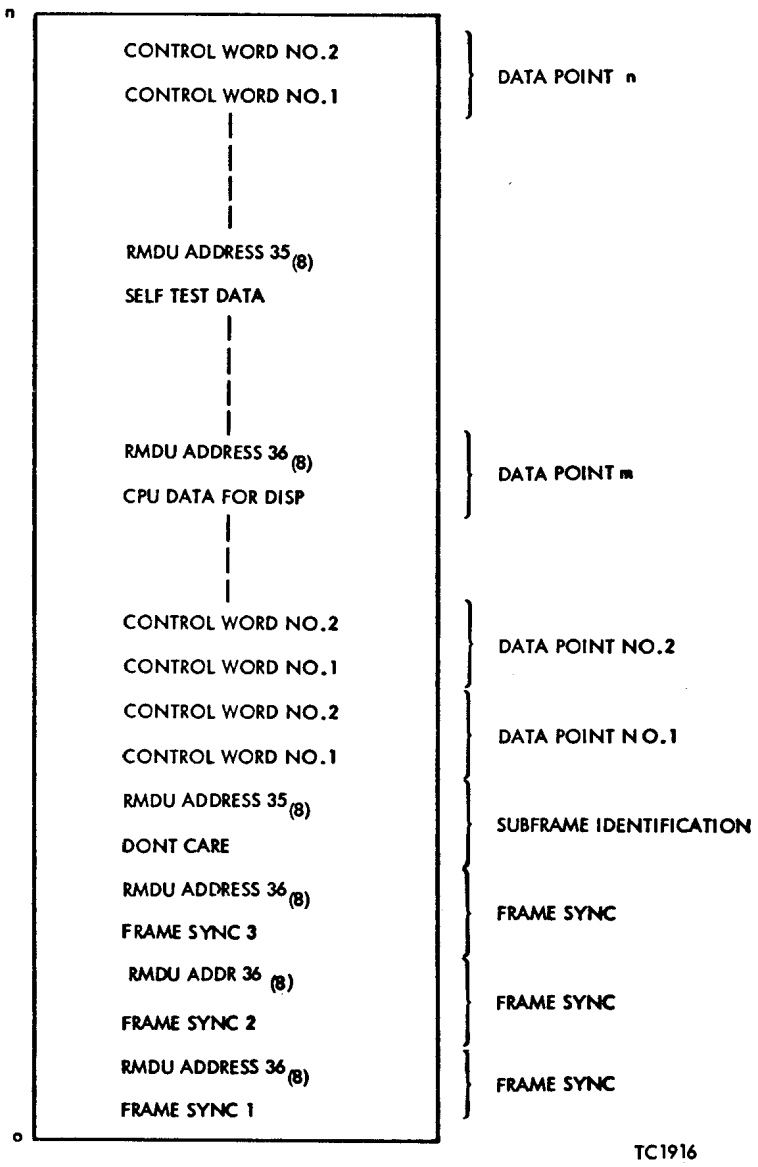

Figure 5. Typical Sampling Program Format Memory Contents

FORMAT MEMORY CONTROL WORD NO.1

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			CARD				GAIN				CHANNEL					

FORMAT MEMORY CONTROL WORD NO.2

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	W0	W1	W2	W3	W4	X0	X1	X2	X3	X4	Z0	Z1	Z2	Z3	Z4	Z5
	RMDU ADDRESS					CONTROL		CONTROL			DESTINATION					

CONTROL

X0	X1	X2	X3	X4	
0	0	D	D	D	MAIN FRAME FORMAT MEMORY
0	1	D	D	D	EØF
1	0	D	D	D	SUBFRAME NEXT
1	1	D	D	D	EØC

DESTINATION

Z0	Z1	Z2	Z3	Z4	Z5	
1	D	D	D	D	D	RECORDER PORT NO.1
D	1	D	D	D	D	RECORDER PORT NO.2
D	D	1	D	D	D	STRIP CHART RECORDER
D	D	D	1	D	D	BAR GRAPH DISPLAY
D	D	D	D	1	D	SEL 840 MP COMPUTER
D	D	D	D	D	1	CPU

NOTES:
1. D = DONT CARE
2. RMDU ADDRESS $35_{(8)}$ = WRAP AROUND SELF TEST
3. RMDU ADDRESS $36_{(8)}$ = CPU DATA FOR DISPLAY OR FRAME SYNC DATA
4. RMDU ADDRESS $00_{(8)}$ - $34_{(8)}$ = VALID RMDU ADDRESS

Figure 6. Format Memory Control Word Organization

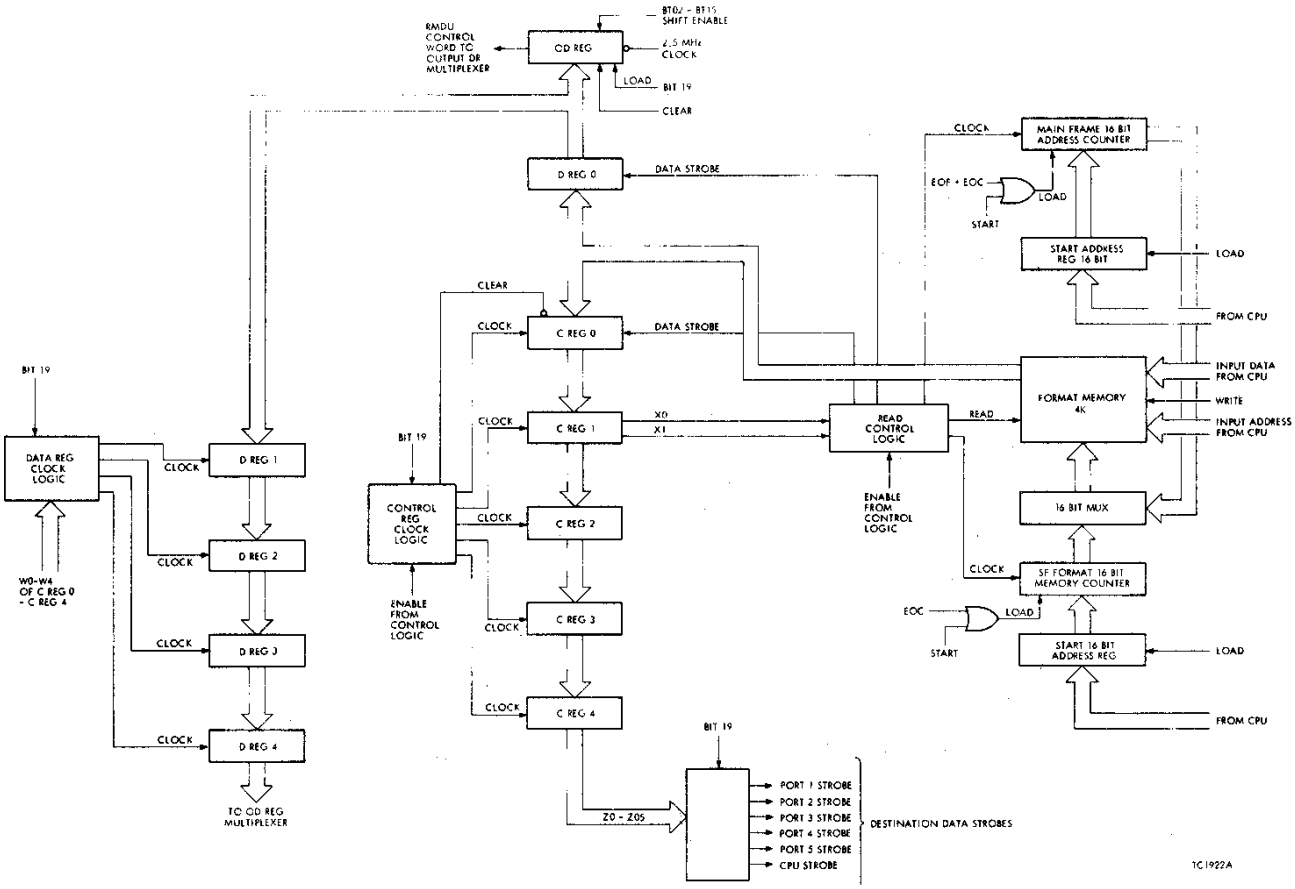

Figure 7. Main Frame/Subframe Format Memory

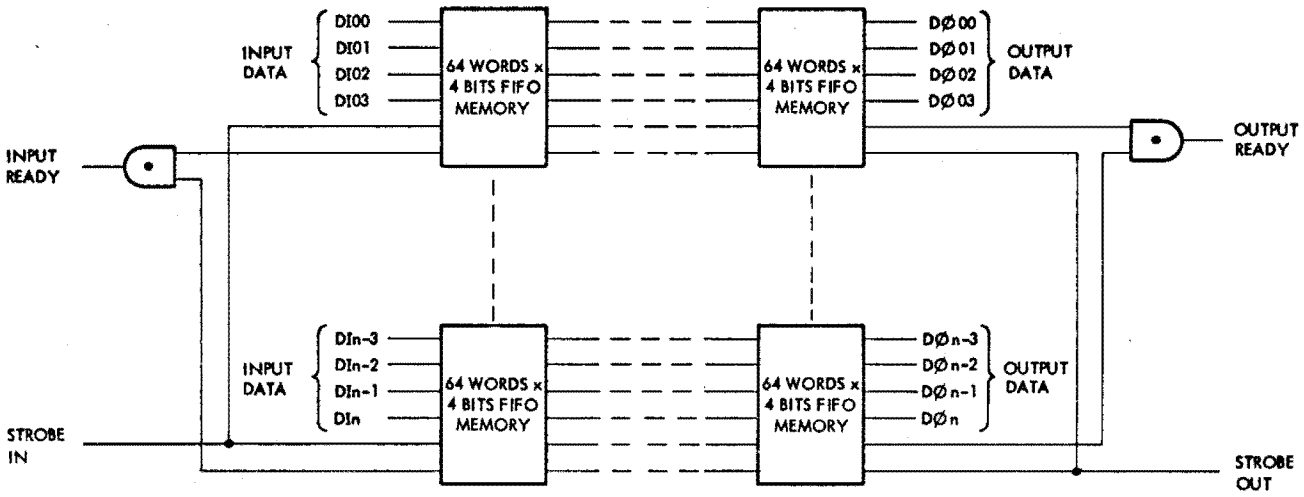

Figure 8. FIFO Buffer Memory

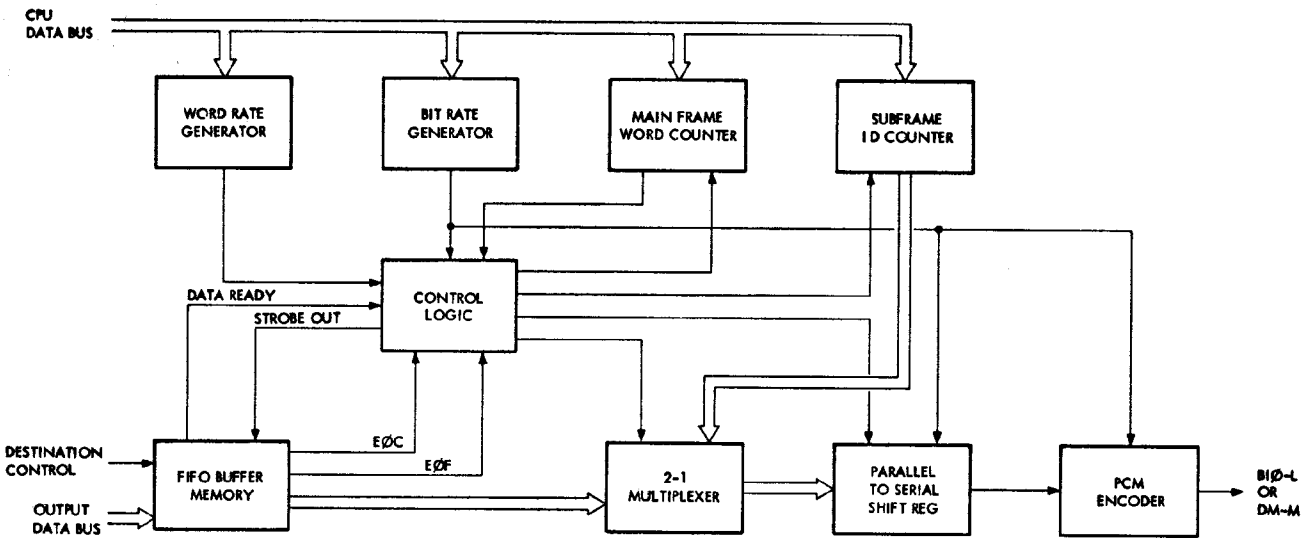

Figure 9. Recorder Controller