CARRIER TRACKING, BIT SYNCHRONIZATION, AND CODING FOR S-BAND COMMUNICATIONS LINKS[1]

J. P. ODENWALDE R
LINKBIT Corporation
San Diego, Calif.

Summary. This paper presents the results of a study of the performance of Viterbi-decoded convolutional codes in the presence of nonideal carrier tracking and bit synchronization. A constraint length 7, rate 1/3 convolutional code and parameters suitable for the Space Shuttle coded communications links are used. Mathematical models are developed and theoretical and simulation results are obtained to determine the tracking and acquisition performance of the system.

It is shown that the combined E_b/N_o degradation due to nonideal carrier tracking and bit synchronization over that required for the ideal tracking case can be held to less than 1.5 dB and that combined carrier tracking and bit timing can be acquired in only a few seconds for the parameters and operating ranges of the Space Shuttle coded communications links.

Introduction. The successful application of convolutional coding depends on the careful design of the carrier and bit timing tracking loops. This is especially true with low rate codes where the channel symbol energy-to-noise ratio, E_s/N_o, may be quite small. Here theoretical and computer simulation results are used to determine the impact of practical bit synchronizer and carrier tracking loops on the coded system performance.

Figure 1 gives a functional block diagram of the coded communications link. This paper, just as the study it represents [1], is organized from the user outward. Since LINKABIT has performed extensive computer simulations and hardware implemented a K=7, R=1/3 Viterbi-decoded convolutional coding system, the ideal demodulation and tracking performance of the system is available for comparison with that of the nonideal cases considered here.

The first section treats the design and impact on decoder performance of a practical bit synchronizer for the BIϕ-L binary PSK modulation used. In addition to tracking

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simulations to determine the degradation in decoded bit error probability, considerable attention and simulations are devoted to synchronizer loop acquisition performance.

The following section incorporates the effects of the carrier tracking loop. Both Costas and decision-directed loops are considered, with considerable performance improvement demonstrated by the latter. Simulation results are obtained for decoder performance degradation due to the combination of bit synchronizer and carrier tracking loops, as well as for the joint acquisition behavior of both loops.

Bit Synchronizer Effect on Coded Performance. The extensive literature available on the subject of bit synchronizers ([2]-[4] among many) deals almost exclusively with the problem of synchronization of a bit stream which employs NRZ-L modulation. Practically none of the references have addressed in any significant detail the problem for BIϕ-L modulation which is used in this application. This form of modulation offers both advantages and disadvantages for acquiring and tracking the bit or symbol timing.

The obvious advantage is that since a transition is provided with certainty during each bit period, a greater effective signal-to-noise ratio is guaranteed in the tracking loop. This is particularly useful during acquisition. It also avoids the problem of maintaining synchronization when a long sequence of zeros or ones occurs in the random data.

There are, however, some potential disadvantages of BIϕ-L modulation. These are, in order of importance:

a) A given fixed timing error will degrade BIϕ-L somewhat more than it degrades NRZ-L modulation; this will be partially or completely offset by the reduction in timing error achieved by the BIϕ-L loop.

b) A bit synchronization loop for BIϕ-L exhibits a two-way ambiguity, with the possibility of locking with a half-bit timing error. This condition can be detected and corrected.

c) The bandwidth occupancy is approximately double that of NRZ-L. Bandwidth occupancy is not likely to be particularly significant in the Space Shuttle application, other than that for a fixed predetection filter, signals with wider bandwidths will be more susceptible to intersymbol interference effects.

Bit synchronizers are members of the class of tracking and synchronization systems whose performance may be evaluated by the classical phase-locked loop analysis ([2], [5]). In addition, bit synchronizer performance is measured by the degradation suffered due to timing errors in the soft decision decoder inputs, whose timing is derived by the

synchronizer. This, in fact, is the most important parameter in the Space Shuttle application.

Numerous types of error detectors are possible. Basically they derive an error signal by integrating over the expected data transitions. With BIϕ-L modulation usually only the guaranteed center transition is used. The transitions between symbols can also be used. However, in this application the added implementation complexity of using the edge transitions is not necessary. The choice of gate width for the integration is governed by the values of the input and desired loop SNR and dynamic range. The narrower the gate, the higher the loop SNR for a given noise level; however a narrow gate produces an error detector characteristic which saturates beyond small timing errors. In this report a gate width of T/4, where T is the channel symbol time, is used.

Figure 2 gives a functional block diagram of the bit synchronizer used. The loop filter can be either digital, employing an accumulator and a scaler for a second order loop, or analog. The VCO can also be either digital, employing an accumulator and a crystal-controlled clock, or analog.

By making enough simplifying assumptions, this system can be analyzed theoretically. A better approach is to use the theoretical results to obtain coarse loop parameters, but to determine the performance by computer simulation. This is the approach used here.

The goal was to design a bit synchronizer capable of tracking frequency uncertainties, i.e., timing ramps, of up to 108 Hz without degrading the coded performance by more than 0.5 dB with respect to that of the ideal tracking performance. Simulations showed that such a synchronizer can be designed. These simulations used second order loops with a damping factor of $1/\sqrt{2}$ and the maximum 108 Hz frequency uncertainty. Figure 3 shows the results for time-loop bandwidth products of 4×10^{-3} and 5×10^{-4}, corresponding to bandwidths of 864 Hz and 108 Hz, respectively, at the 216 kbps channel symbol rate. The larger bandwidth is used in the acquisition mode.

Since there are no theoretical results available for predicting acquisition times a low signal-to-noise ratios, the simulation program was used to estimate this time. It was found that at the threshold value of symbol E/N_o = -5 dB acquisition times became excessively long for offsets equal to or greater than the loop bandwidth. However, it was found that by using a wider loop bandwidth during acquisition the situation was markedly improved. For an acquisition loop bandwidth of 864 Hz, i.e., 8 times the tracking loop bandwidth, the mean time to lock with the 108 Hz offset was about 0.08 seconds. In this case the acquisition time (in symbol times) is defined as the number of symbol times from the start of acquisition until the first of 4096 consecutive symbol times during which the magnitude of

the timing error is less than 1/8 symbol time. In practice a somewhat larger acquisition time would be required to guarantee that with a very high probability the loop is locked.

other acquisition strategies involving stepping or sweeping the VCO over the region of uncertainity were also investigated. one strategy which was simulated stepped the VCO over the region of uncertainty in 8 equal steps, using a 864 Hz bandwidth for each step. Thus the maximum frequency uncertainty per step is 13.5 Hz. The total acquisition time with this strategy is about 8 times the single step acquisition time. This total time was found to be about the same as that of the single step strategy of the preceeding paragraph.

Combined Carrier Tracking and Bit Synchronizer Loop Effects on Coded Performance. Combined carrier tracking and bit synchronizer performance was considered for Costas and decision-directed carrier tracking loops.

Figure 4 shows a block diagram of the two types of carrier tracking loops considered. Without the limiter the diagram represents a Costas loop, with the limiter it is termed a decision-directed loop. m(t) represents the antipodal modulation, S is the signal power and n(t) is the wideband Gaussian noise of one-sided power spectral density of N_o, $n_c(t)$ and $n_s(t)$ represent independent in-phase and quadrature noise components.

The discrete time version of the loop used for the computer simulation is shown in Figure 5. The matched filters are matched to the BIϕ-L modulation and their timing is controlled by the bit synchronizer.

As with the bit synchronizer loop, the phase locked loop theory can be used to obtain coarse estimates of many of the loop parameters. However, computer simulations are needed to determine the coded tracking performance.

Figure 6 shows the simulated performance of the coded system with both carrier tracking and bit synchronization loops implemented. A second-order decision-directed carrier tracking loop and carrier tracking and bit synchronization loop bandwidths of 640 Hz and 160 Hz, respectively, were used. Tracking data was also obtained with a Costas rather than a decision-directed loop. This data showed that the Costas loop was inferior to the decision-directed loop for this application.

The 640 Hz carrier loop bandwidth, B_L, was selected large enough to obtain a small steady state phase error, but small enough to make the probability of loss of lock very small. From linear phase locked loop theory the steady state phase error with a damping coefficient of $1/\sqrt{2}$ and the maximum expected doppler rate of 4.1 KHz/sec can be shown to be $7240/B_L^2$ radians. The 640 Hz bandwidth makes this error insignificant. Also simulations showed

that the probability of loss of lock with this bandwidth is very small. In all of the simulations at this bandwidth the loop never lost lock.

The curves of Figure 6 show that the combined carrier and bit timing tracking degradation from that of the ideal tracking case can be maintained at reasonable values. For the set of loop bandwidths used here, the total degradation varies from 0.6 to 1.3 dB for E_b/N_o ratios from 2.5 to 0.5 dB, respectively.

Acquiring carrier tracking within a reasonable amount of time with the maximum expected doppler offset of 55 KHz requires either a large loop bandwidth or that the loop be stepped or swept through the frequency range of uncertainty. Simulations have shown that the carrier loop bandwidth cannot be increased very much above 640 Hz without occasionally losing lock. So in the acquisition simulations the loop bandwidth was fixed at 640 Hz. Acquisition simulation data for the combined carrier tracking and bit synchronization loops was obtained for bit synchronization and carrier tracking loop bandwidths of 864 Hz and 640 Hz, respectively, the single step bit synchronizer acquisition strategy of the previous section, and carrier tracking acquisition strategies which assume the VCO is swept through 64 or 512 steps. At an E_b/N_o of 2.5 dB both strategies required a total acquisition time of about 0.4 seconds.

Conclusions. This paper presented some of the results of a study of a coded digital transmission system suitable for the Space Shuttle. The tracking loop parameters required to maintain the error probability performance curves within 1.5 dB of the ideal achievable for a K=7, R=1/3 convolutional encoder-Viterbi decoder with perfect bit and carrier tracking have been determined. It has been established, partly theoretically but mostly by simulation, that this performance can be achieved by using a bit synchronizer for BIϕ-L modulation and a decision-directed carrier tracking loop utilizing matched filters, which derive symbol timing from the bit synchronizer. The required loop bandwidths for the bit synchronizer and the carrier loop are, respectively, 160 Hz and 640 Hz.

Acquisition for both loops can be achieved within 0.4 seconds even at E_b/N_o ratios as low as 2.5 dB.

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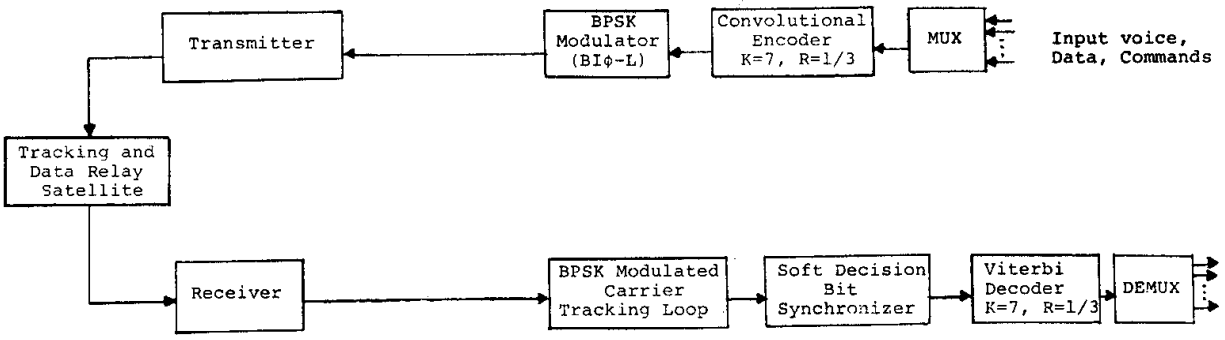

Figure 1. Coded Communications System Block Diagram

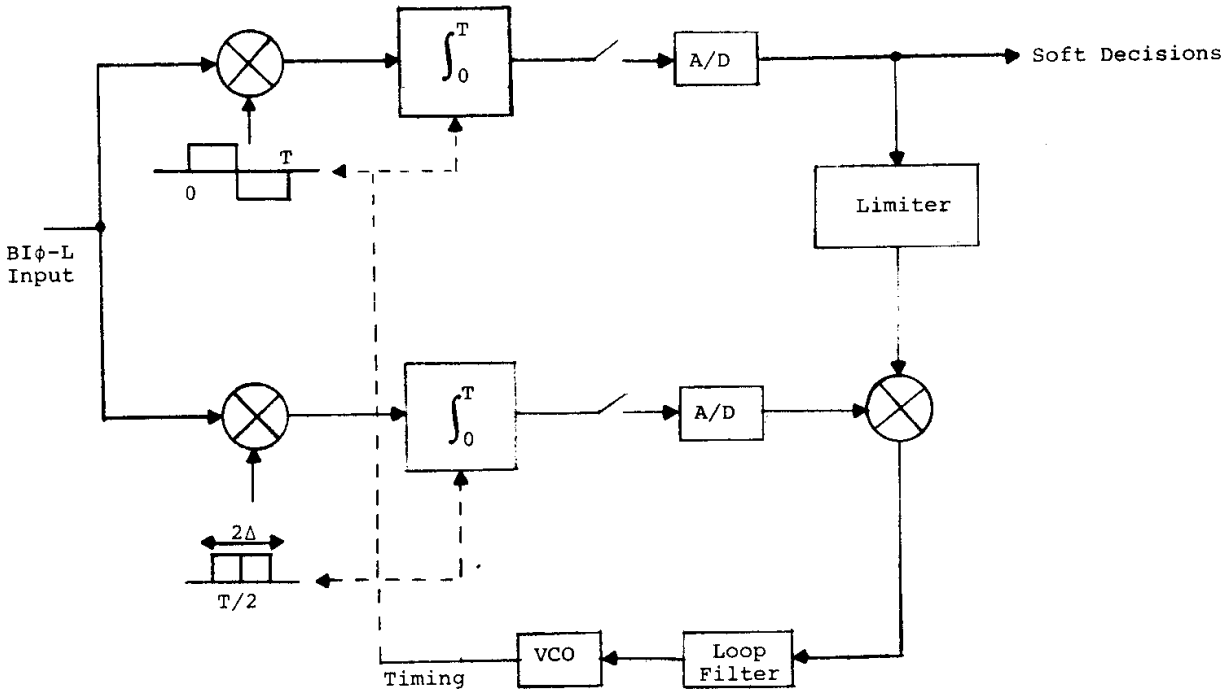

Figure 2. Bit Synchronizer Block Diagram

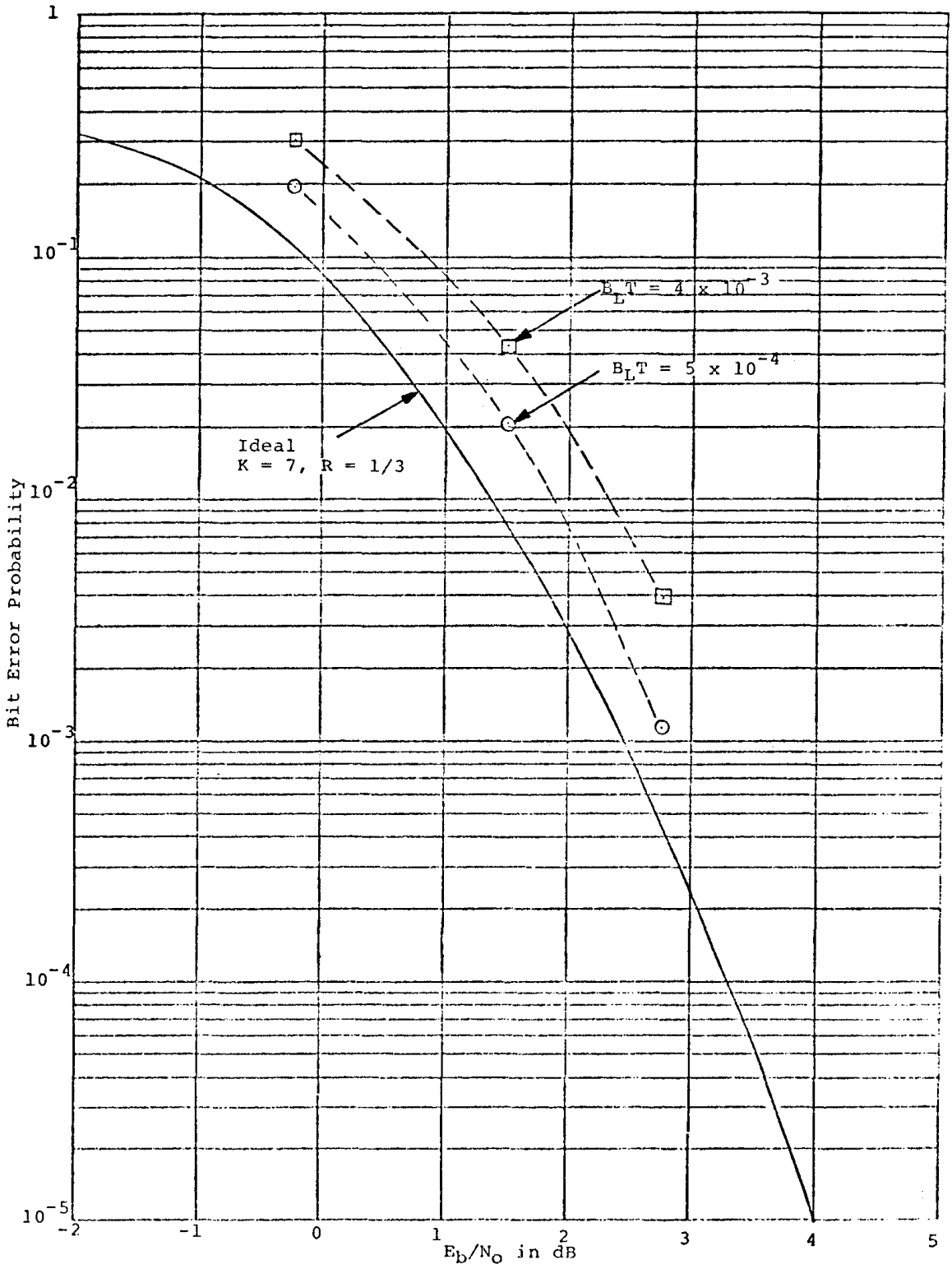

Figure 3. Coded System Performance with Nonideal Bit Timing

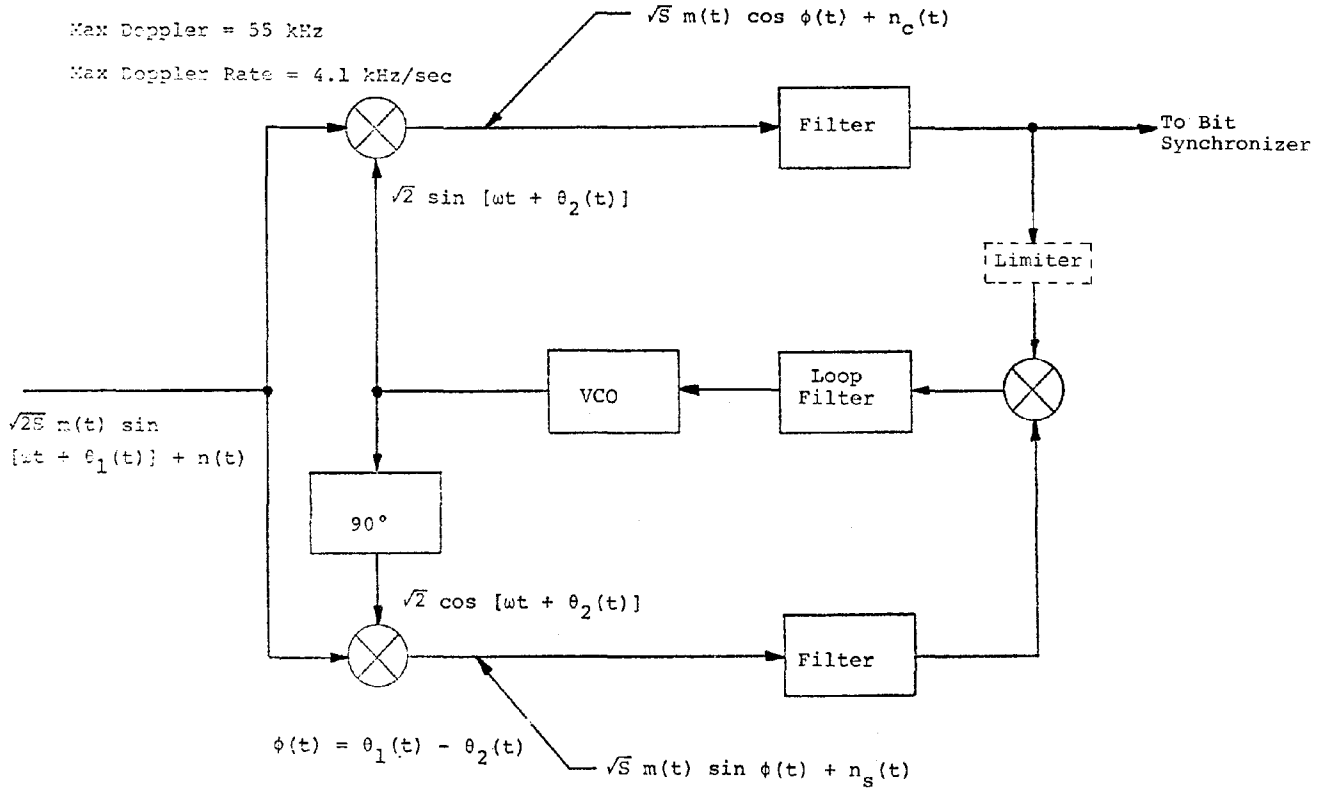

Figure 4. Carrier Tracking Loop Block Diagram

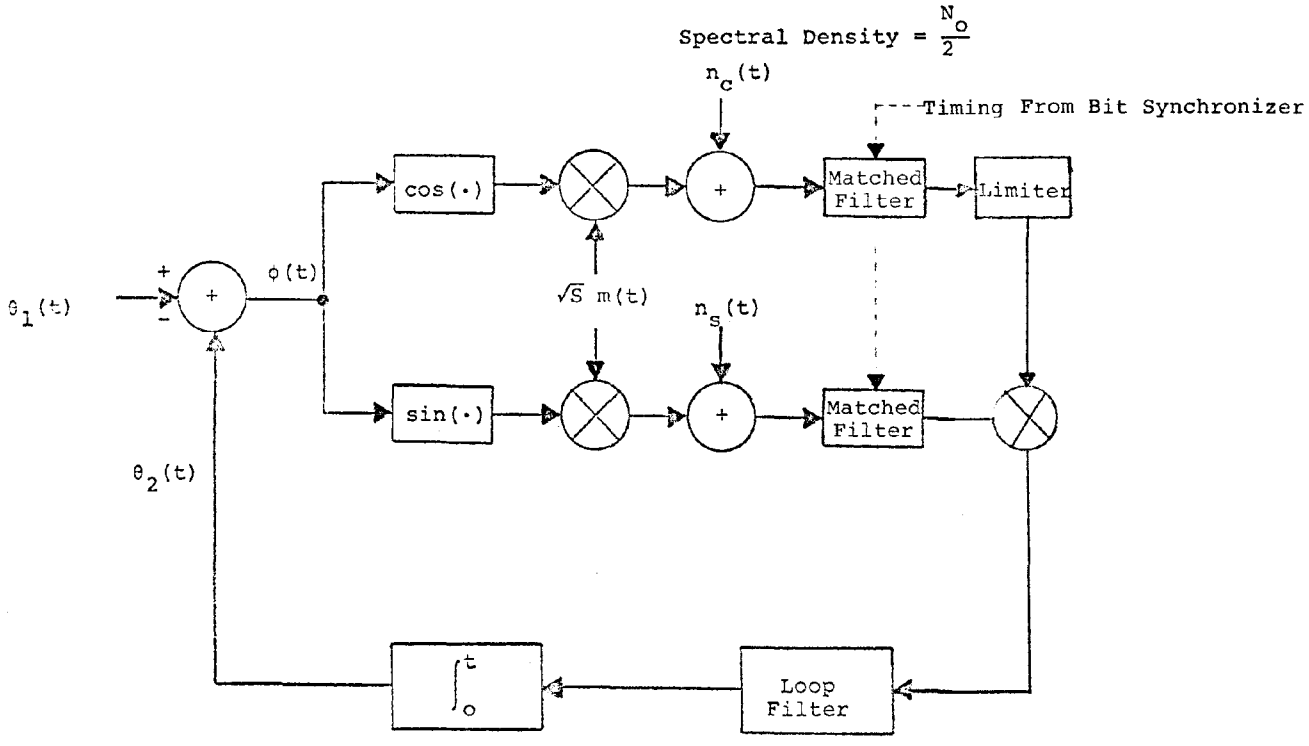

Figure 5. Simulation Carrier Tracking Loop Model

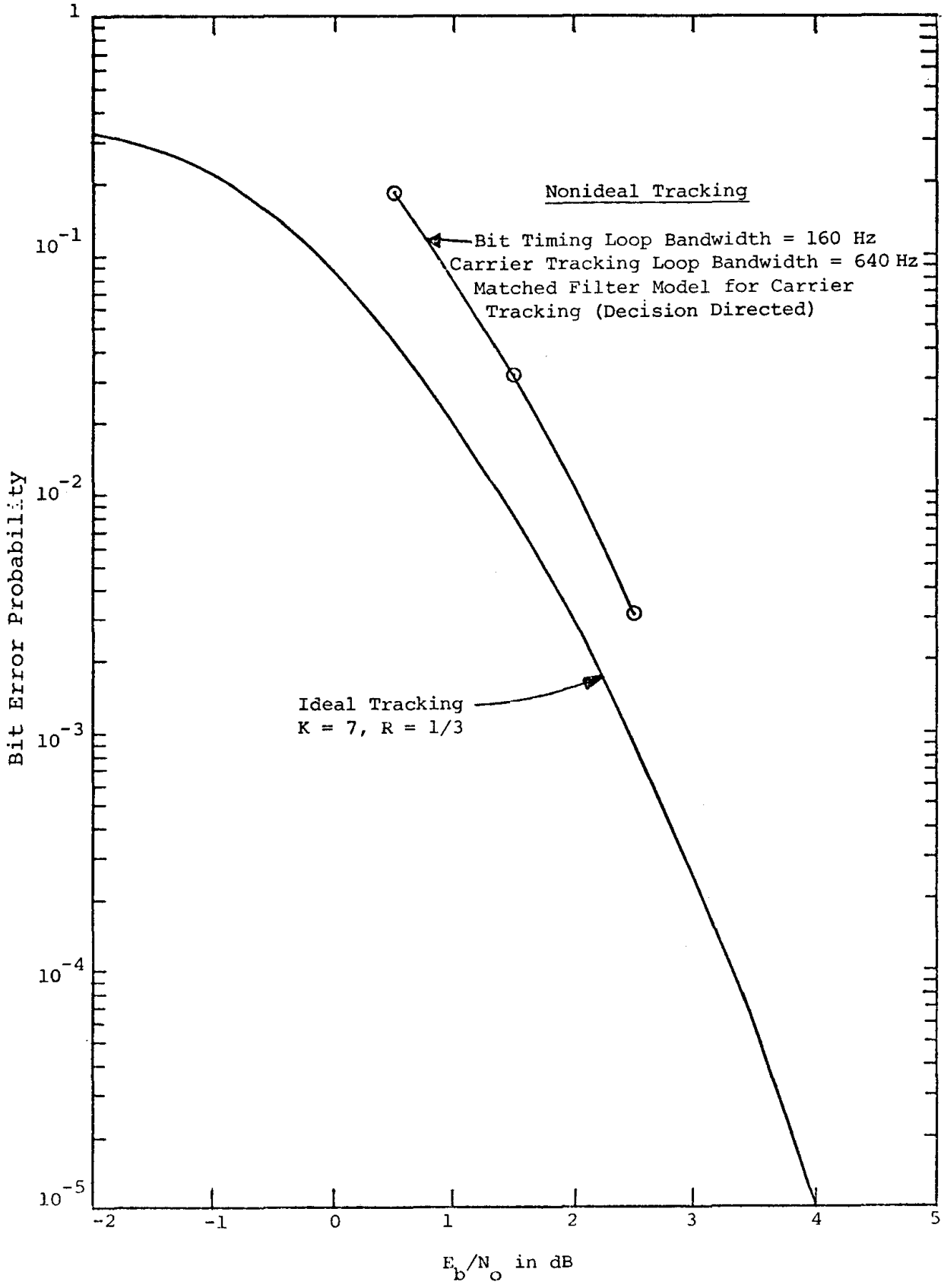

Figure 6. Coded System Performance with Nonideal Carrier