PERFORMANCE TESTING OF PCM BIT SYNCHRONIZERS

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Summary. Performance testing of modern PCM bit synchronizers requires special test equipment above and beyond that available in commercial laboratory instruments. As a result of this need, a standard product Telemetry Bit Error Rate Detector (TBERD) has been designed to fill the requirement for a special-purpose test instrument for use with PCM systems. After examining the primary performance characteristics of bit synchronizers, the TBERD unit was designed to measure both detection and synchronization performance for a wide range of bit rates and for all of the commonly used PCM codes.

Introduction. The widespread use of pulse code modulation (PCM) in telemetry systems has spawned the requirement for specialized test equipment. The measures of performance for PCM differ considerably from those for an analog system and, consequently, standard test equipment such as signal generators and so forth have only limited utility. In many cases, the development of adequate test equipment has lagged behind the development of new products. In the course of developing a high-performance PCM bit synchronizer, the requirement for a special-performance test unit became readily apparent. The utility and flexibility of the engineering test unit subsequently led to the design of a standard product test unit.

In this paper, the test requirements for a bit synchronizer test unit are considered and techniques for the measurement of bit error and synchronization performance are examined. An operational Telemetry Bit Error Rate Detector (TBERD) unit is discussed.

Test Requirements. System testing of PCM telemetry links has been discussed in the literature(1). The performance of the typical PCM telemetry system is primarily determined by the performance of the bit synchronizer. Thus, the emphasis here shall be placed an testing of the typical PCM bit synchronizer. The testing of a bit synchronizer may be classified into two types: (1) operability tests and (2) performance tests. Operability tests are normally performed in an operational environment to determine the operating condition of the bit synchronizer. Some form of test set may be provided to determine whether the synchronizer is operating within some predetermined performance bounds. This type of test is a go/no-go test in that the system user merely wishes to assess whether the unit has a certain prescribed minimum performance. The second type of test is designed to determine the specific performance of the unit. Performance tests may be made by the user to determine specification compliance or by the manufacturer to ensure that a product meets its delivered specifications. Test requirements vary from system to system and any test unit must have sufficient flexibility to cover a variety of test requirements.

The test unit must, as a minimum, have the capability to measure the fundamental performance parameters of the bit synchronizer. The unit must also be capable of measuring the performance under a variety of perturbations which occur in practical system applications. The two primary performance parameters of a bit synchronizer are the detection performance, as measured by bit error probability, and the synchronization performance, as measured by parameters such as acquisition time, tracking jitter, and synchronization threshold. These performance parameters must be tested in the presence of typical system perturbations. Perturbations in most telemetry system applications can be described by additive random noise inputs, periodic additive signals, and input timing variations. Testing a bit synchronizer with additive white gaussian noise provides a means of comparing the synchronizer performance with theoretical bounds. Additive periodic signals, normally specified as a baseline shift, represent perturbations such as unwanted pickup and interference from adjacent signals. Input timing variations simulate effects such as flutter and wow from tape recorders. The test unit must be capable of measuring the synchronizer performance with these perturbations over a range of bit rates encompassed by the majority of the telemetry PCM applications and with a tuning resolution sufficient to measure such parameters as capture and tracking range for a given bit rate. At the present time, the majority of the PCM telemetry systems operate at data rates of less than 5 megabits per second. Standard PCM bit synchronizers typically cover the range of 1 bit per second to 5 megabits per second in both tunable and fixed tuned units. The test units must also be capable of generating the PCM input codes as specified in the IRIG standards(2) and with signal levels compatible with the typical bit synchronizer. With these requirements, techniques for measuring the performance of the bit synchronizer will now be considered.

Detection Performance. The standard PCM telemetry bit synchronizer not only includes clock recovery circuits but also the basic detection circuits for recovering the digital data in the presence of various signal perturbations. Bit error probability has been established as an accepted measure of the detection performance. This performance measure is primarily useful in gaussian random noise environments. When the input perturbations can be characterized as gaussian noise with an arbitrary power spectral density, the bit error probability, as measured by the average number of bit errors in a given number of data bits, represents the most significant detection performance measure. When the input noise is non-gaussian, other performance measures such as the mean time between errors may be more useful. Under these conditions, however, comparing measured data with theoretical performance predictions becomes considerably more complex. One can also argue that the performance of a bit synchronizer under gaussian random noise is indicative of its relative performance in other types of noise environments. Conceptually, the measurement of bit error performance is straightforward. The test unit generates a fixed digital data stream which is summed with an external noise source. The noisy signal is fed to the bit synchronizer which reconstructs the data. The reconstructed data would then be compared with a suitably delayed replica of the generated data bit stream. Errors can then be counted on a bit-by-bit basis. This technique has the advantage that an arbitrary data format can be simulated and every bit error can be detected and counted. The disadvantage of this technique is that the delay between the reconstructed data stream and the input data stream must be known or must be measured. This delay, in turn, must be utilized to delay the reference data stream so that the reference and reconstructed data can be compared an a bit-by-bit basis. In applications such as laboratory bench testing, this technique is entirely suitable if sufficient delay is provided in the test unit. There are a variety of system tests, however, in which the delay between the reference data and the reconstructed data may be excessively long or may be completely unknown. An example of this situation occurs when testing the performance of a bit synchronizer with tape recorded data.

A technique for avoiding the problem of unknown delay between the reference and recovered data utilizes self-synchronizing pseudo-random data sequences. A detailed discussion of self-synchronizing digital sequences is beyond the scope of this paper and the reader wishing to explore the properties of these sequences in greater detail is referred to existing technical literatures[3,4]. The basic principle of self-synchronizing sequence testing is to generate a digital sequence in the test box which forms the basic reference data stream. The recovered digital data from the bit synchronizer is fed to the test unit which contains a sequential logic circuit which synchronizes on the input data sequence and allows errors between the reconstructed sequence and the generated sequence to be measured without a knowledge of the absolute delay between the two data streams. In practice, this is accomplished by using a feedback shift register to generate the reference data stream and a similar sequential circuit to resynchronize on the recovered data and measure bit errors. The use of linear sequential circuits to generate self-synchronizing data sequences is a special case of self-synchronizing data scrambler circuits. A basic data scrambler and self-synchronizing descrambler is shown in Figure 1. The reference digital data stream output is equal to the modulo 2 sum of input data and a sequence of digits from the feedback shift register. If the tap connections in the basic scrambler are determined by a primitive polynomial over the algebraic field GF (p), Savage[4] shows that the digital data stream at the output of the scrambler will respond to an input with a periodic line sequence which either has the period of the input data or a period which is the least common multiple of the input data and 2^m-1. Now suppose that the data input to the scrambler consists of the all-ones condition. In this case, the output digital data stream consists of a data stream which has a period of 2^m-1. Furthermore, Savage shows that the transition density of the output data stream satisfies the following bounds:

$$\frac{1}{2} \quad \frac{(2^m - 2)}{(2^m - 1)} \leq \delta \leq \frac{1}{2} \quad \cdot \quad \frac{2^m}{2^m - 1}$$

Thus, the generator output produces a quasi-random data stream having an average transition density of about 0.5. When this data stream is fed to the descrambler as shown in Figure 1B, the descrambler output will be a replica of the scrambler input data provided no bit errors have occurred. In the noiseless case, we can see from the diagram of the descrambler that the data output satisfies the following equation:

$$\hat{d} = s \oplus g$$

where g = output of the feedback shift register.

For no errors,

$$s = d \oplus g$$

$$\therefore \hat{d} = d \oplus g \oplus g = d$$

When no noise is present, the data output is reconstructed exactly. If all-ones data is inserted into the scrambler in the absence of bit errors, the descrambler output will consist of all ones. Suppose now that a bit error occurs in the reconstructed data. As the bit in error progresses through the descrambler shift register, it will cause erroneous outputs in the feedback sequence and consequently the output of the descrambler will be zero indicating a bit error. If the descrambler has W feedback taps, each input bit error will create an average of W output errors. As long as the average distance between bit errors is greater than the descrambler shift register length, the descrambler will be able to self synchronize and indicate data errors.

This measurement technique is completely automatic and requires no operator adjustment to initiate synchronization. There are several disadvantages to this error measuring technique, however. One disadvantage is the fact that the descrambler is unable to function properly at very high bit error rates. Secondly, the number of errors at the output of the descrambler is a multiple of the number of actual channel errors. Consequently, the test equipment must compensate for this multiplication factor. An alternative technique can remove these objections at the expense of some minor operator intervention. If the descrambler is arranged as shown in Figure 1C with a momentary switch in the feedback shift register, the unit will operate as follows: If the switch is momentarily depressed by an operator, the recovered digital data is fed into the registers of the feedback shift register. If no errors are present in the bits which are loaded into the register, the descrambler will synchronize to the input data and begin producing a replica of the input data stream with the proper synchronization. When the momentary switch is released, the local sequence generator free-runs independently of the input data sequence. The two sequences are, however, in synchronism, and the sequences can be compared bit-by-bit to determine bit errors in much the same manner as with the fixed pattern. Thus, bit errors can be counted directly without requiring any scaling and errors can be measured at very low bit error rates, provided the internal sequence generator is resynchronized with a low error rate data stream.

In comparing the two techniques for measuring bit error probability, there are advantages and disadvantages for both techniques. The primary advantage of the self-synchronizing technique is the ability to measure performance with an unknown or very large time delay between the reference signal and the recovered data. This makes it possible to measure bit error performance in tape recorder systems and over communication links having a large or an unknown propagation delay. The primary disadvantage of the self-synchronizing technique is the specific nature of the test data sequence. The sequence approximates a pseudo-random data stream which has an average transition density of approximately 0.5. While this is a desirable test feature in some applications, in many applications it is desirable to examine the performance of the synchronizer under more realistic data patterns. Thus, a primary advantage of a fixed format test technique is the ability to generate a data sequence which might approximate a practical data format. This permits testing of the synchronizer under conditions with less than 0.5 transition density, and with more realistic data signals. The primary disadvantage of the fixed format technique is the requirement to have an absolute delay compensation between the test unit and the synchronizer under test.

Synchronization Performance. The second major performance parameter of interest in a bit synchronizer is the performance of the clock extraction circuitry. Before bit decisions can be made, the bit synchronizer must extract timing clocks from the input data. There are several parameters of interest associated with synchronization. One parameter is the acquisition time. In many applications, the time required for the synchronizer to achieve phase lock is of paramount importance. The second parameter of considerable interest in practical systems is the signal-to-noise ratio at which the synchronizer begins to lose lock and starts skipping clock cycles. In general, the performance of any synchronizer is measured by the rms clock jitter as a function of input signal-to-noise ratio. The theoretical mean square error performance has been discussed in numerous technical articles(5, 6). The synchronization performance is as vital to system performance as is the basic detection performance. Consequently, the test unit should provide, as a minimum, a means for measuring sync acquisition time and tracking and synchronization threshold performance.

Measuring Acquisition Time. If the data stream from the simulator is blanked for a large number of symbol periods, the bit synchronizer under test will lose lock and the tracking loop will settle to some arbitrary initial condition. Once the loop has settled, the input data stream can be enabled and the phase error between the reconstructed clocks from the bit synchronizer and the reference clock from the test unit can be measured. A pulse can be produced from a comparator circuit each time the two clocks differ by more than some fixed phase error. During the synchronization acquisition period, the phase error between the clocks might be expected to exceed the preset threshold a considerable number of times until the loop achieves phase lock and the average phase error is less than the preset threshold. Thus, by monitoring the instantaneous phase error, an indication can be obtained when the synchronizer has achieved a given level of phase lock. By counting the period between the time at which the data was enabled and the time at which the phase error decreases below the preset threshold, a measure of acquisition time can be made. The typical acquisition performance of the standard PCM bit synchronizer is shown in Figure 2. In order to measure the performance of the typical bit synchronizer, the test unit should have the capability of measuring acquisition times up to about 10,000 bit periods.

Measuring Tracking and Synchronization Threshold. The tracking performance of the bit synchronizer is measured by the rms phase jitter in the reconstructed clock. Although most applications do not require a detailed knowledge of the phase error performance of a given bit synchronizer, occasionally this information is of importance. One method of measuring phase error is to exclusive OR the reconstructed clock with the reference clock. Provided fixed delays are removed in this comparison, the output of the exclusive OR will be a measure of the phase error. Consider, for example, the waveforms as shown in Figure 3. In the absence of a phase error, the output of the exclusive OR is ideally zero, although in actual practice, small spikes are produced at the symbol transition times. As the phase error between the recovered clock and the reference clock increases, the exclusive OR output produces a pulse train with pulses whose widths are proportional to the instantaneous phase error. Furthermore, the pulse train is a function of the absolute value of phase error since negative phase errors produce the same output as a positive phase error. The pulse widths vary periodically as a function of phase error. When the phase error is 180 degrees relative to the reference clock, the exclusive OR is at a high output. As the phase error becomes greater than 180 degrees, the average output decreases. If this pulse train is fed into a very narrow low-pass filter effectively integrating the pulse train, the DC level of the output of the filter will be approximately proportional to the expected value of the absolute phase error. If we consider the instantaneous phase error to be a random variable with approximately a gaussian probability density, it can be shown(7) that the expected value of the absolute phase error is proportional to the rms phase error. This relationship holds only for a gaussianly distributed phase error. It has been shown theoretically(5) that the phase error does in fact approach a gaussian distribution for small errors and is reasonably gaussian for phase errors as high as perhaps

30 to 50 degrees rms. For these conditions, the DC level of the averaged pulse train is a direct measure of the rms phase jitter. For large phase errors, or equivalently low signal-to-noise ratios, phase error measures made in this manner begin to depart from the actual rms phase error. Figure 4 shows some typical phase error measurements taken in this manner showing the departure from the theoretical values at very low signal-to-noise ratios. In many cases, however, this measurement technique is adequate for engineering evaluation. Closely associated with the phase error measurement is the measurement of clock cycle slips. This measurement can be made by monitoring the instantaneous phase error using logic circuits and counting each time the phase error exceeds a preset threshold. Each time this threshold is exceeded, the clock is assumed to have slipped a cycle. By measuring clock cycle slippages, the synchronization threshold, as a function of input signal-to-noise ratio, can be determined. By providing techniques for measuring acquisition time, tracking and synchronization threshold performance, in addition to bit error performance, a reasonably complete test of a bit synchronizer can be conducted.

Test Equipment Design. Based upon the typical test requirements and the performance measures for bit synchronizer, a special-purpose TBERD has been designed which provides test signals and error detection capability to measure the performance of PCM bit synchronizers, tape machines, RF links and other PCM systems. The TBERD generates PCM signals in all of the commonly used codes. Internal bit rates are selectable from 1 bit per second to 5 megabits per second with ± 0.5% resolution. This data rate range permits the testing not only of typical telemetry PCM systems, but includes the rates which are commonly used in many telecommunication applications. The resolution of tuning permits data rates to be set up to examine frequency offset conditions and to measure capture range.

Under “Detection Performance,” it was shown that both fixed data patterns and pseudo-random patterns have application in testing PCM systems. As a result, the TBERD unit is provided with both capabilities. A unique 16-bit word with each bit front-panel selectable can be incorporated into a fixed data pattern with up to 512 words per frame. The choice of pseudo-random sequence was based on a compromise between sequence length and the probability of sequence resynchronization at low bit error rates. A 2047-bit sequence was selected which is generated by an 11-bit shift register with feedback taps on stages 9 and 11. The TBERD provides inputs for adding gaussian noise with bandwidths up to 20 MHz, baseline variation and offset, and bit rate jitter to the PCM output signal. An external data filter can be used to simulate pre-modulation filtering. An internal counter with a front-panel display counts bit errors, clock slippages and synchronization acquisition bit periods, depending upon the display and count mode selected. The counting period can be selected from 10 bits to 10^7 bits in powers of 10 and a totalized mode is provided. An interesting addition to the counting mode permits the counting of errors in both ones or zeros or in only ones or only zeros. In a like manner, all clock slippages can be counted or only positive or negative slips counted. This feature has use when adjustments must be made to the bit synchronizer. A predominance of errors in either one state or the other can be indicative of an improperly set decision circuit. A simplified block diagram of a PCM generator portion of the TBERD is shown in Figure 5. The digital data is generated as NRZ-L data which is then converted to the appropriate output data code. The PCM data is summed in a wideband amplifier with externally-provided perturbation sources. White random noise can be summed with the PCM through a switch-selectable step attenuator. The step attenuator allows the operator to set up a reference signal-to-noise ratio. By merely pressing the appropriate switch an the front panel, the signal-to-noise ratio can be varied in 3 dB steps. If a reference signal-to-noise ratio of 0 dB is set up, the operator can, from the front panel, selectively attenuate the noise so as to provide signal-to-noise ratios up to 21 dB in 3 dB increments. A shift register delay is provided in the PCM generator to delay the fixed pattern data up to 7-1/4 bit periods in increments of 1/4 bit period. Figure 6 shows the basic error detection circuitry. The recovered data and clocks are fed to a pseudo-random data reference generator and to the bit error detector. The reconstructed clocks are fed to the acquisition error detector and the clock slip detector. The outputs of the bit error, acquisition error and clock slip detectors are switch-selectable into the error counter. The contents of the error counter are displayed on the front panel. The basic reference data rate clock is generated from a stable VCO which can be externally frequency modulated to simulate jitter. In the sync acquisition mode, the acquisition time in bit periods is determined directly by presetting the display counter to a count of 10,000. Each time an acquisition error is detected between the recovered clock and the reference clock, the counter is again preset to 10,000. After 10,000 bit periods following the enable signal, the counter contents are displayed in acquisition bit periods directly since the number left in the counter at this time is 10,000 minus N where N is the number of bit periods elapsed since the last acquisition error.

Measurement Error. Measurement errors, when using the TBERD unit, are largely dependent upon the capability and accuracy of external test equipment since the majority of the measurements in the TBERD are digital. The precision attenuator errors combined with errors in the summing amplifier contribute to a maximum error in setting up the signal-to-noise ratio of approximately 0.25 dB. Overall measurement accuracy depends primarily upon the accuracy to which true rms measurements of the noise source can be made and the apparent stability of noise sources themselves. For frequencies up to approximately 20 MHz, true rms measurements over typical input noise levels can be measured to an accuracy of approximately ± 0.2 dB. The stability of the typical noise source is of the same magnitude. Under production test conditions, the TBERD unit combined with high-quality noise sources and true rms meters can be used to routinely measure error performance with an accuracy of ± 0.5 dB. Under closely controlled laboratory bench conditions, measurement errors can perhaps be reduced to something in the order of 0.3 dB.

References

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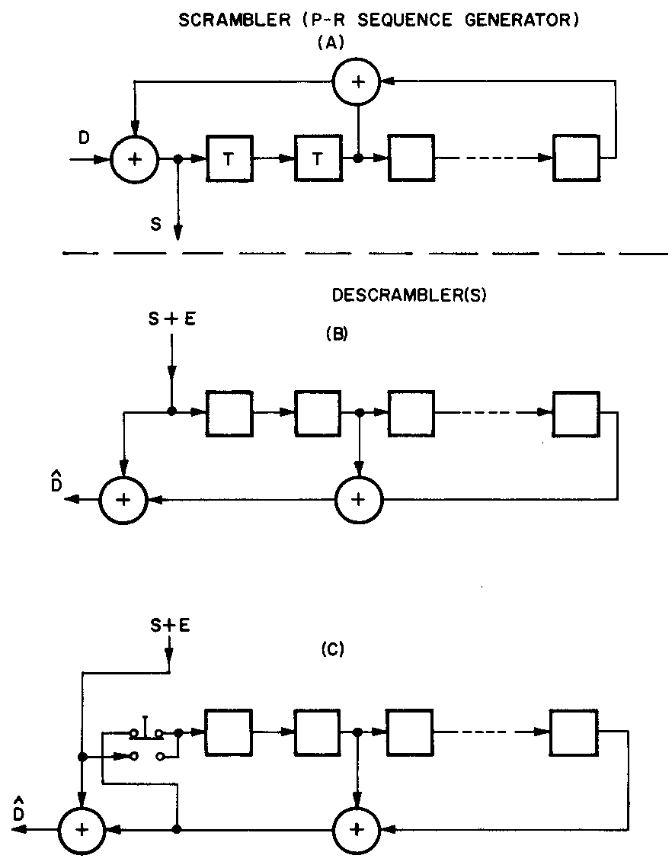

Fig. 1 - Self-Synchronizing P-R Sequences

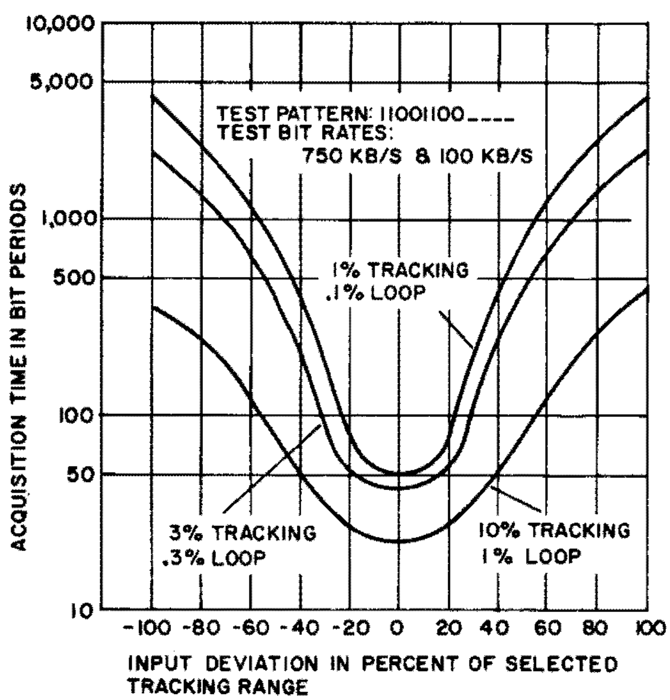

Fig. 2 - Typical Acquisition Performance

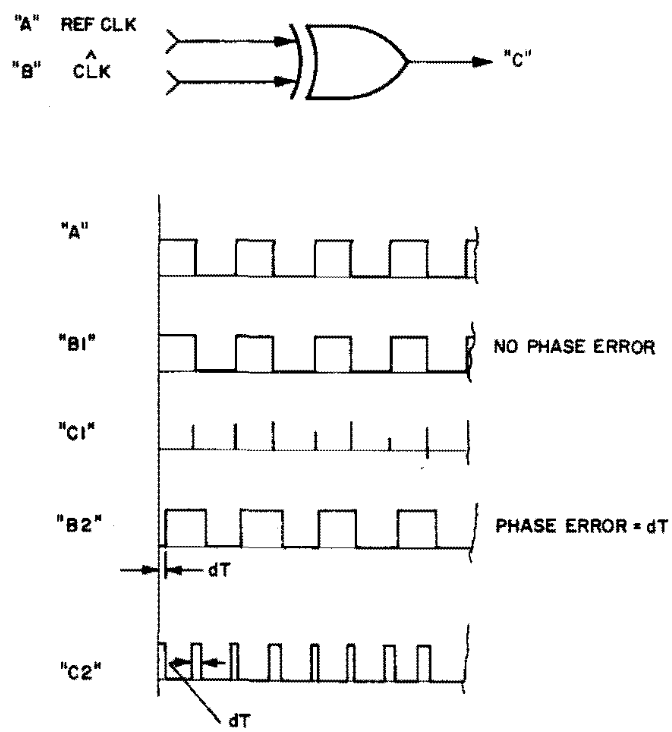

Fig. 3 - Phase Error Measuring Circuit

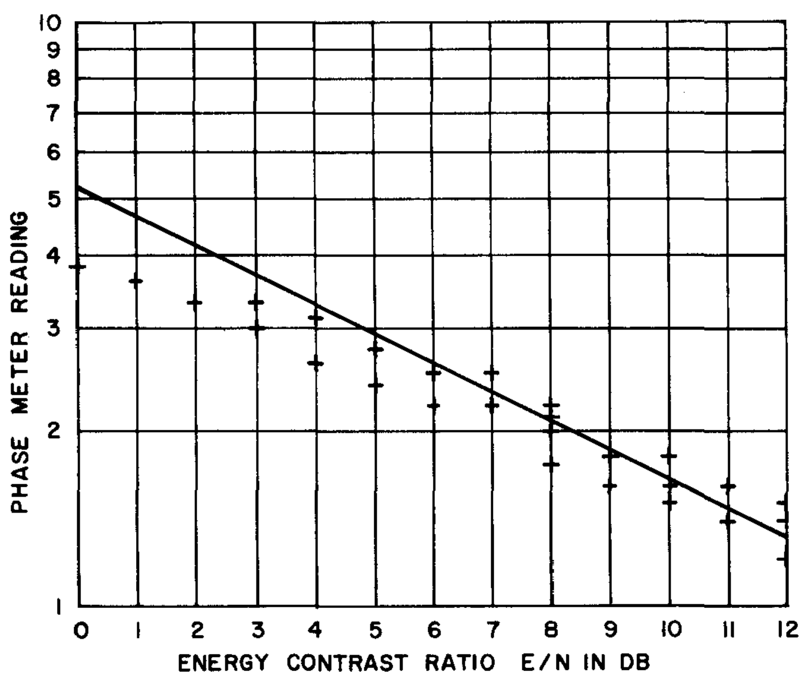

Fig. 4 - Experimental Phase Error Measurements

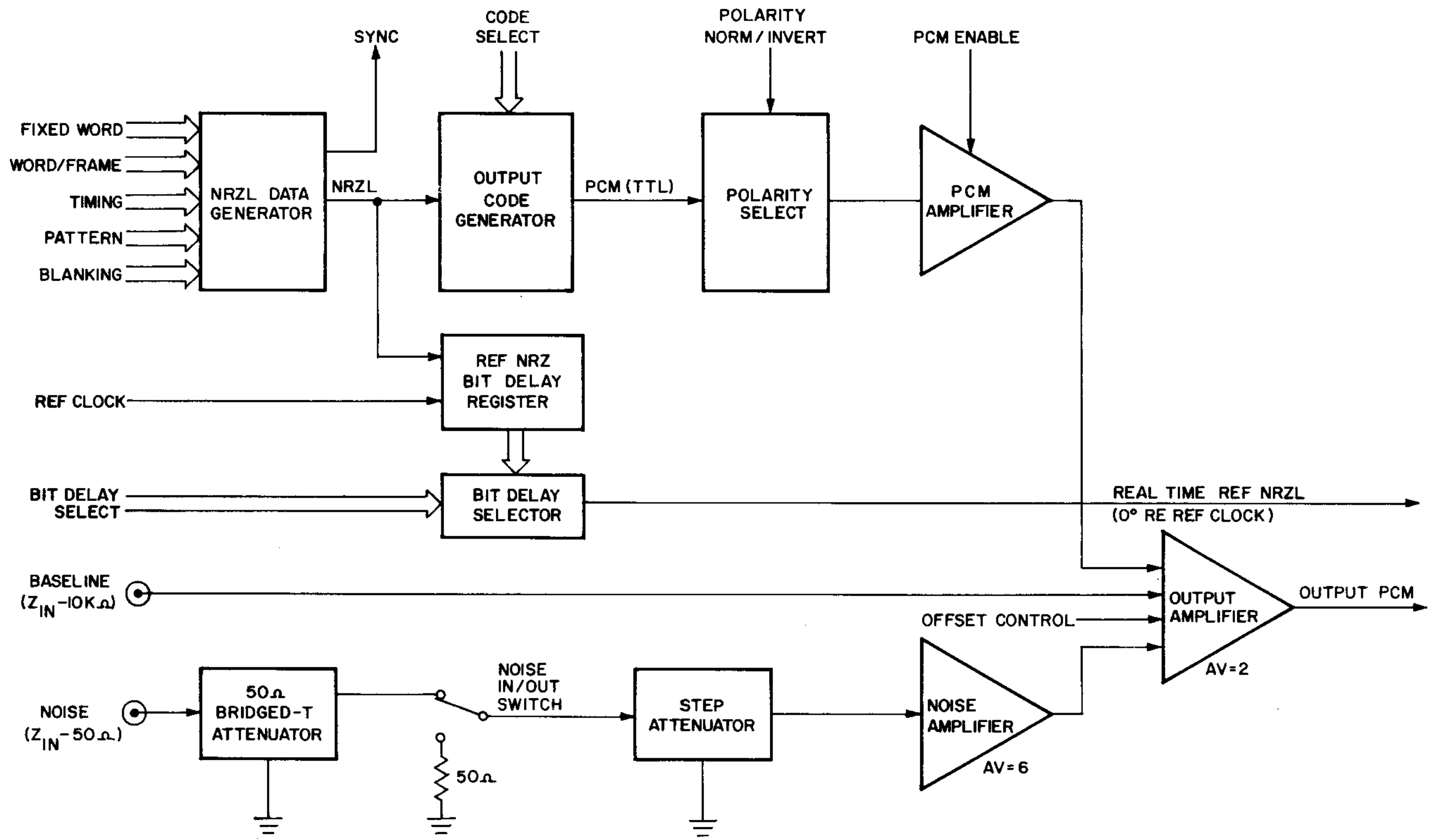

Fig. 5 - PCM Generator Circuit

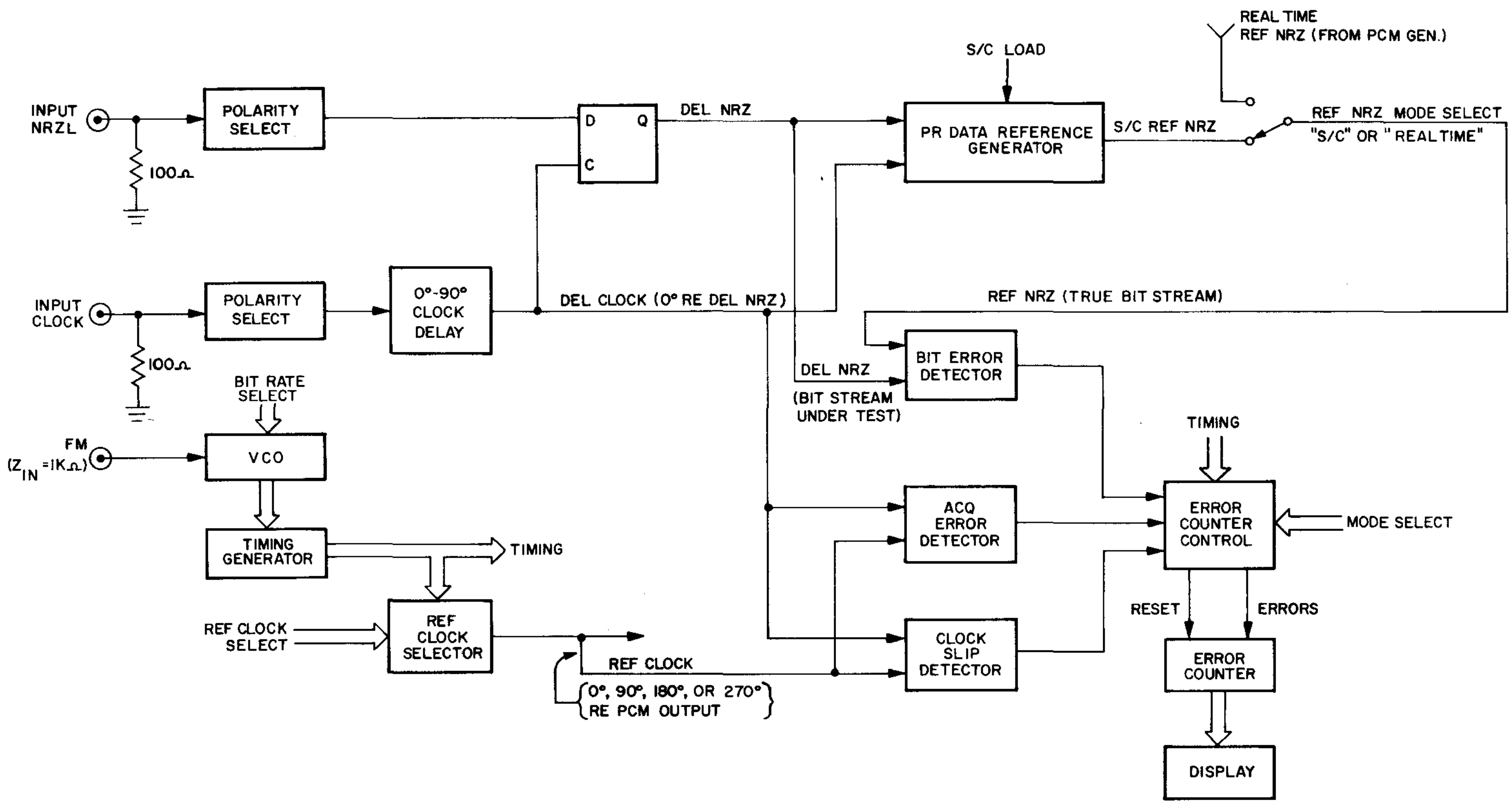

Fig. 6 - Error Detector Circuits