A 200 MEGABIT PER SECOND DATA HANDLING/DATA LINK SIMULATOR

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Summary A multimegabit serial data channel, or slower parallel channels may be needed to monitor multiple input data (including video) from sources such as Earth Resources Experiments, Communication Satellites, and surveillance systems. It is desirable to operate space equipment at low power, which is contrary to the use of fast circuits. Low powered circuits are compatible with the speeds of parallel systems, but multiple channel RF systems are usually costly in both size and weight. A parallel series compromise appears to minimize these problems. A laboratory breadboard of a parallel-series data handling simulator consisting of a data acquisition unit (DAU), a 200 Mb/s serial data link (SDL), and a data recovery unit (DRU) was built and tested to operate satisfactorily up to 230 Mb/s in a typical noisy environment.

Introduction There is a continuing need for data systems to handle large amount of data, which implies large data bandwidths. While the requirements for large data handling systems on such projects as Skylab and Space Shuttle may phase out with culmination of these projects, there is an ever-increasing demand for large data capacities in communication satellites. The term communications is used in the broadest sense as it pertains to commercial, military and NASA applications. All data such as video, voice, instrumentation, navigation, meterological, and survillance continue to “eat up” bandwidth, creating an ever-increasing need for communications at higher frequencies.

Although most of the data sources can be expected to operate at relatively low rates, about 10 Mb/s and lower, the total serial data rates may easily be several hundred Mb/s. Multiple lower rate data links can obviously be used for transmission of this data from Space to Earth, but probably not without a rather large and complicated rf-system. Most recent trends are to develop the data system with two serial outputs that operate at data rates up to 500 Mb/s each for driving a two quadrant modulator. With this approach, serial systems operating to 1 Gb/s have been implemented; however, if a person is restricted to using readily available components, the limit is probably less than 500 Mb/s.

This paper describes the design, fabrication, and operation of a data handling simulator that operates at rates up to 230 Mb/s. Two channels of this system could drive a two

quadrant modulator to provide a 460 Mb/s system. The circuitry utilized is “off-the-shelf” emitter coupled logic for functions operating from about 60 MHz to the 230 MHz. Motorola MECL 10,000 logic is used at about 60 to 100 MHz, and MECL III is used for circuits operating above 100 MHz. Standard and low powered versions of TTL and Schottky TTL are used wherever possible, with emphasis on low power. These state of the art devices are well known by most of us, but too much emphasis cannot be placed upon the application technology above 100 MHz. There is no distinct dividing line at this frequency but the needs for proper line terminations, correct attachment of multiple loads, and devices’ delays seem to be suddenly very apparent. Although the application and design handbooks prepared by Motorola and others are excellent for addressing the problems, the user need almost experience the pitfalls to appreciate criteria for their avoidance. In addition to discussing general design techniques, data synchronization, sync detection, and the clocking of received data, including phase locked loops are considered herein.

Digital Design for Operation Above 100 Mb/s. A large amount of the design of the 200 Mb/s simulator is best presented in a general form. This approach provides some specific discussions of the system, but also provides fundamentals for those not familiar with emitter coupled logic (ECL) circuits.

While there may be no exact operating frequencies where digital circuit designs change, it is assumed that the design concept does change for handling data at rates above 100 Mb/s. There are several reasons for this, with component limitations a primary factor. Essentially all TTL devices are unusable above 100 MHz, and even most of the MECL 10,000 ECLs are too slow for practical use at that frequency. In addition, circuit designs can no longer be limited to logic only, i.e., serious consideration must also be given to RF design techniques. Printed circuit boards should have ground and voltage planes; lines must be short and/or terminated in their characteristic impedances; line lengths must be considered in event-time relationships; and because of high frequencies, the suppression of cross-talk must be considered. A work knowledge of these factors must be attained before a 200 Mb/s design capability is possible. The remaining paragraphs in this section describe the high speed circuit designs that were developed during the performance of this task.

One of the major considerations in component selection, at least for airborne applications, is to design using the lowest power consuming components possible. This requirement is not particularly compatible with high speed circuit performance, i.e., for most state-of-the-art circuits. ECL circuits are the only readily available components that are operable in digital circuitry at 200 Mb/s or higher. There are also custom integrated current steering logic circuits and discrete component circuits, but their use is limited and they also consume relatively large amounts of power. Consequently, component trade-offs at multimegabit frequencies are limited, except for minimizing the number of devices used. A

method of accomplishing this is to divide the basic frequency down (to the greatest extent possible) for parallel operations at lower frequencies. The importance of this technique cannot be overly stressed and it will be emphasized throughout this report. In fact, the discussions concerning the breadboard design shows how it was first implemented improperly by neglecting this technique. A final design improvement is then described to show that most processing was accomplished at 100 Mb/s, or less. Not only is lower power consumption possible, but circuit performance is also enhanced when operating at the lower bit rate. However, further discussion regarding component selection is warranted.

Numerous vendors manufacture several types of ECL circuits that can be used at the high bit rates. The operating frequencies quoted for these circuits vary from approximately 100 MHz to 1 GHz for flip-flops; however, readily available devices are restricted to a few types. Motorola provides a line of MECL devices that are typical of most available components. MECL 10,000 is designated as one of the easiest types of ECL to use up to 100 Mb/s. General design notes stipulate that the circuitry is easily handled using standard component boards with printed circuit lead, or back plane wiring interconnects. Solder, wire wrap, or Termipoint* connections are all considered acceptable. Although some transmission line terminations are required, they are not identified as being critical. Experience gained during the course of this task, however, shows that these circuits are in fact difficult to use at 100 Mb/s. Interconnections must be short, lines must be matched, or both. The number and configuration of multiple loads must be closely monitored, and propagation delays must be considered carefully. There are few MECL 10,000 devices that can be used practically at operating frequencies above 100 Mb/s. Gates available in this Motorola line, e.g., the 10105, have typical propagation delays of 2 nanoseconds, and rise/fall times of 3.5 nanoseconds. A few of the gates classified as transmission line drivers, e,g., the 10210, have propagation delays and rise/fall times of 1.5 nanoseconds. The flip-flops developed initially, e,g., the 10131, are guaranteed to toggle at 125 MHz (minimum) with a typical toggling frequency of 160 MHz. A flip-flop developed more recently, i.e., the 10231, toggles at 225 MHz.

It is evident that the MECL 10,000 is not particularly suitable for operation at 200 Mb/s. The Motorola product that is acceptable for operation at 200 Mb/s is the MECL III family. Gates such as the 1660 have typical propagation delays of 1.0 nanoseconds, and typical rise/fall times of 2.1 nanoseconds. Flip-flops such as the 1670 will nominally toggle at 350 MHz.

The use of standard TTL, low power TTL, Schottky TTL, and low power Schottky devices is encouraged where designs can be implemented at lower speeds. There are known problems with the reliability and yield of standard Schottky devices; however, the

* Trade name registered by AMP Corporation

simplicity in using them offers an attractive advantage up to 80 MHz. The use of high powered TTL offers no advantages in most instances because the power consumption is high, and flip-flop toggle frequencies are limited to approximately 40 MHz.

If data rates are low enough, CMOS logic (which is rapidly becoming more available) could become a serious contender in logic designs. CMOS offers attractive power savings and noise immunity for circuits operating under 1 MHz.

In summary, general rules to be followed in component selection might be stipulated as follows:

- use the least amount of high speed ECL logic possible, i.e., minimum MECL III:
- divide all signals to the lowest practical frequencies using MECL 10,000 circuits in the division chain as required; and
- implement as much circuitry as possible using TTL or CMOS logic.

Earlier objectives of this task resulted in the design of hardware operating at 100 Mb/s. It was demonstrated that circuits could be built on standard PC boards using wire wrap or Termipoint backplane wiring. MECL 10,000 components were installed in conventional DIP sockets. As implied above, the performance of these circuits was not entirely satisfactory at 100 Mb/s. Since problems with line terminations, cross talk, and loading were apparent, it was decided to use different construction techniques for the new ECL circuits. Our approach was to use doublesided PC boards, without sockets. Backplane wiring was still used, but all lines were terminated in their characteristic impedances. Motorola's application notes list multilayer boards as the first preference for high frequency work; however, the high cost and length of time necessary to develop and manufacture such boards could not be justified for a onetime breadboard. The double-sided board approach is a secondary solution, i.e., it is satisfactory if the boards are kept small and contain only a few (about 10) IC components.

When designing with a 2-sided PC board the two sides are used for a ground plane and a voltage plane. The voltage plane can be positive or negative, depending on how the ECL is used. Recommended practice is to use the MECL operating from ground to -5.2 volts (when only one voltage is used). A 5.2 volt differential between V_{CC} and V_{EE} provides the optimum in speed performance. Minus voltages give the beat noise immunity. Since terminating resistors must be returned to a -2 volt bias point, a recommended practice for single voltage operation is to use two resistors connected in series between ground and V_{EE}. (See Figure 1).

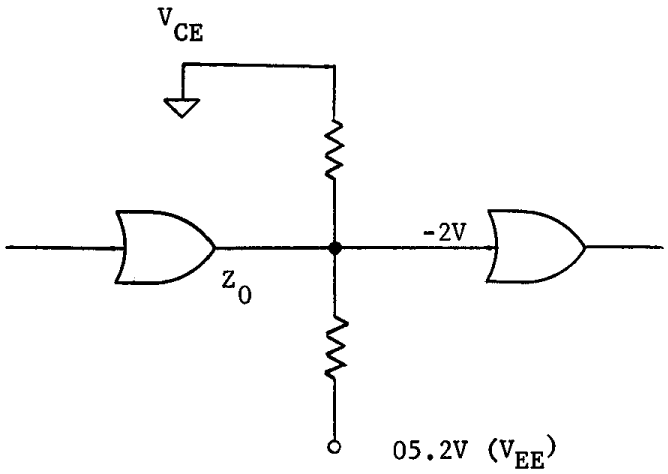

Figure 1. Parallel Termination with One Power Supply

The resistor ratio is selected to provide -2 volts (as indicated), and the parallel Thevenin equivalent value of the resistors should equal Z_0, the characteristic impedance of the interconnecting line.

Initial laboratory evaluation of the double-sided board design approach gave very good results. A divide by N counter was designed and built using MECL III 1670, D-type flip-flops. Most backplane wiring was configured as single conductor, teflon insulated stripline, with a characteristic impedance of approximately 68 ohms. Some twisted pair lines were used over long lengths, i.e., more than 3 inches. The clock was a Hewlett-Packard 608 rf-sinewave generator, capacitively coupled into an input biasing network similar to that shown in Figure 1. The counter divided correctly with input frequencies up to 300 MHz.

During evaluation of the counter, the parallel termination shown in Figure 1, and a series termination suggested by Motorola were examined. The parallel termination is used only at the most remote load on a line. If there are intermediate loads they are tapped with minimum length stubs to preclude reflections. It is not always convenient to tap multiple loads, as the series configuration shown in Figure 2 may have application in some designs.

In Figure 2, R_S plus the output impedance of the driving gate must equal Z_0. This configuration could not be made to perform well at 200 Mb/s.

The results of breadboard evaluation of the counter were encouraging and the data link simulator was designed using the 2-sided PC board. This approach ultimately proved to be somewhat less than optimum, as is discussed later. The major difficulty was in the selection and use of two bias resistors for line termination. Application notes show that the characteristic impedance of backplane wiring is consistent with wire type, length, and spacing from the PC board. The notes also show criteria for modifying the impedances,

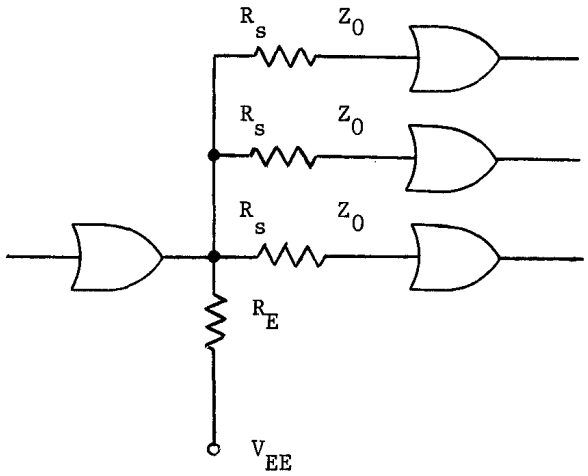

Figure 2. Series Termination

which change due to different distributed loads. In practice, however, specifying wire lengths and wire spacing on the board, and adhering to these requirements can become a tedious and difficult task. As a result, the selection of two bias resistors, and the pull-down resistor (if required) is time consuming and also requires a large resistor stock. In addition, the -2 volt bias point derived from the resistors is not stable enough under load variation at the higher frequencies. Therefore, a minimum of three layers are recommended for ECL at data rates of 100 Mb/s or greater. The third layer is used for a -2 volt fixed bias supply. The three layer board allows for a much simpler selection of terminating resistors, and since the bias is obtained from a fixed supply, circuit performance is greatly enhanced.

The subject of backplane wiring is extensively covered by others, e.g., Motorola's MECL System Design Handbook; therefore, comments are limited to the experience gained as a result of this task.

Since PC boards with backplane wiring were used, we experimented with, and traded off some of Motorola's techniques. An equation presented by Motorola for determining the characteristic impedance of a wire over a ground plane is

$$Z_0 = \frac{60}{e_r} \ln \frac{4h}{d}$$

where e_r is the effective dielectric constant around the wire,

h is the height to the center of the conductor from the ground plane, and

d is the diameter of the conductor.

This characteristic impedance is stated by Motorola to be approximately 120 ohms ±40%.; however, our experience on this task (using the same type materials) gave results more typically equal to 80 ohms ±40%.

The above equation is applicable to a line between two terminals; however, practical circuits will usually have multiple loads on a line. An equation used to modify the characteristic impedance due to loads is

$$Z_0 = \frac{Z_0}{1 + C_d/C_0}$$

where C_0 is the line capacity, and

C_d is the effective distributed capacity due to the loads.

The effective input capacity of MECL loads is about 3 pf per gate input, with variations depending upon the type of MECL.

Unfortunately, all of the line characteristics are dependent upon the total geometry of the wiring and PC board layout. If lines are more than 2 inches long (approximately), and the number of leads is greater than three (approximately), then the matching and termination of lines becomes difficult, and the resultant reflections of mismatches will cause problems when operating at frequencies of 100 MHz or higher.

The data handling/data link simulator

Figure 3 is a block diagram of the 200-Mb/s data handling system simulator built in 1974. The hardware consists of three major blocks, as indicated. The data acquisition unit (DAU) simulates multiple slowspeed data sources being sampled, multiplexed, and formatted, together with sync bits, into a 200-Mb/s serial data stream. The data link (DL) is a hardwired link into which noise was inserted to evaluate performance of the data recovery in the presence of noise. In the initial design there were both data and clock lines in the link, but design refinements were made to eliminate the clock by adding a VCO to the data recovery unit (DRU). This provides a closer simulation of an RF link on which there probably would be no bandwidth available for clock. The DRU detects sync and synchronizes itself to the received data. Data are demultiplexed and then compared with reference data from the DRU. The recovered analog data are compared visually with the source data on an oscilloscope, and all data bits in the recovered stream are compared with transmitted data. Error rates are determined from the comparison and displayed to show the effects of noise on the recovery accuracy. Frame sync dropouts and frames to sync are also displayed.

The DAU consists of simulated data sources, data multiplexing circuits, a sync generator, formatting and control logic, a data serializer, and line driver circuits. Data are sampled and formatted in one of two selectable formats. The major frame format patterns consist of fifty-six 42-bit minor frames. A minor frame consists of a 7-bit analog equivalent word, thirty-four discrete or digital bits, and a sync bit in the forty-second position. In one

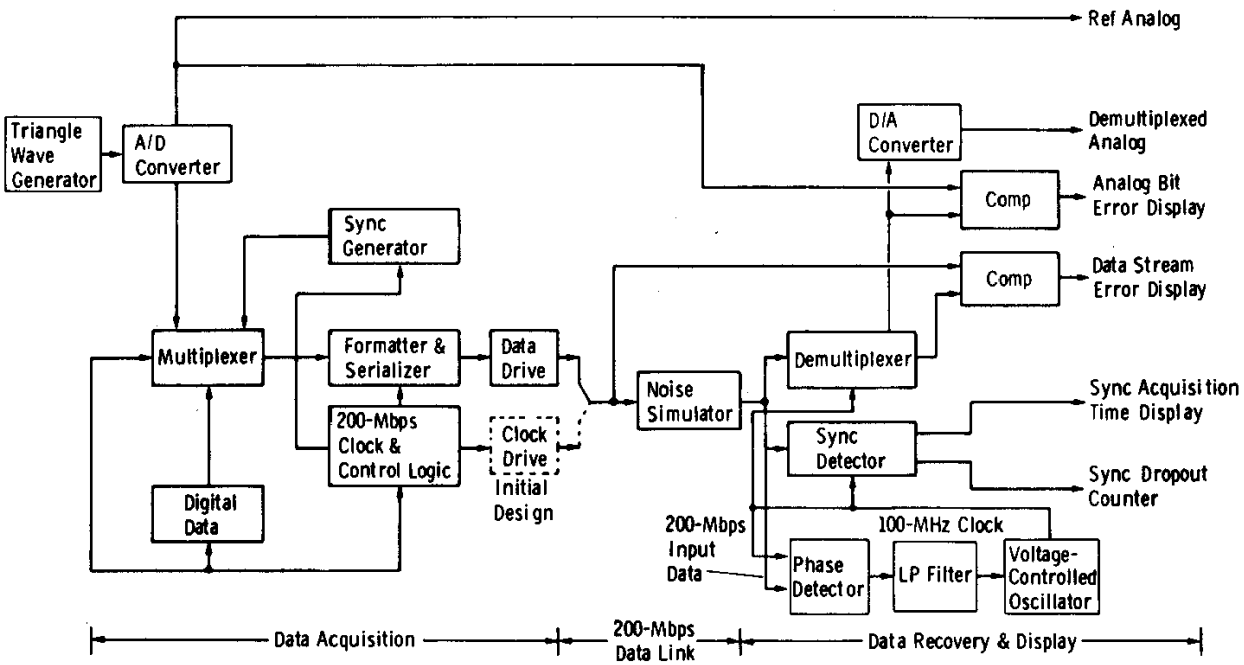

Figure 3. Block Diagram 200 Mb/s Data Handling/Link Simulator

format, the 7 bits representing the analog channel occur at bit positions 1 through 7. The other format distributes these bits at every sixth bit position beginning with 1, i.e., 1, 7, 13, 19, 25, 31, and 37. The analog signal source is a 100 KHz to 300 KHz sawtooth generator operating asynchronously to the system. The sawtooth is sampled, and the sample is digitized by a two step successive approximation A/D converter into 7-bits once every minor frame (about once every 200 nanoseconds.) The thirty-four digital sources are simulated by multiplexing the outputs of a pseudo-random sequence generator. The sync bit is multiplexed from a fixed format sequence generator, which is incremented once each minor frame so that the sync word is the sequence of the sync bits in the 42 minor frames.

A 7-state shift register with feedback generates the multiplexer gate addresses in the proper format for sampling and serializing the data. The outputs of the multiplexers are combined into two groups which are alternately loaded into a two 3 bit serial shift register which operate at 100 Mb/s. Serial outputs of the two registers are “OR’d” together into the 200 Mb/s data stream. The two serializer registers are alternately used to allow enough time for the Schottky TTL multiplexers to operate. The use of two registers also keeps the operating frequencies of most circuits at 100 MHz or less; except for the basic clock and the data link drivers, which operate at 200 MHz rate.

The serial data link consists of a twisted shielded pair of lines for data. Clock noise generators are also a part of this link, even though they are physically located in the DRU.

The DRU receives the data in NRZ form and an internal voltage controlled oscillator (VCO) is synchronized to the data. The nominal operating frequency of the VCO is 100 MHz. Since there are no spectral lines in a 200 Mb/s data stream, the VCO cannot be locked directly to it. The data, however, can be “AND' d” with itself delayed by about 1/2 bit and there will be spectral lines to which the VCO can be synchronized. Although there are a number of phase detectors to use in the loop, an exclusive or circuit worked about as well as any in the VCO.

Data is received in the presence of noise and is arbitraily divided into two 100-Mb/s bit streams (i.e., bits 1, 3, 5, etc for one stream and bits 2, 4, 6, etc for the other, forming “odd” and “even” streams). A bit of each stream is compared with a sync bit in the sync word generator at what is believed to be the bit 42 time of each minor frame. When a major frame is completed and one of the bit streams compared with sync has less than four errors, the system is considered in sync. That stream containing bit 42 is known to be even, thus identifying the sequence of all bits. If there is no sync in a major frame, the minor frame bit counter (42-count) is retarded two counts and a new major frame is examined. The count is retarded until there are less than four errors, at which point bit 42 is identifiable. Once sync is established, demultiplexing is easy, i.e., as the time of all bits is known. Recovered data can be compared with reference and error rates determined by digital counters monitoring for a known total bit time.

Performance MECL circuits were initially fabricated on double sided PC boards. The DAU (which uses the least MECL components) could be made to operate fairly well by carefully tailoring the two resistor networks; however, the DRU operation was very poor. Not only were the lines difficult to terminate, but in addition, too many circuits were operated at 200 MHz. Two significant design criteria already mentioned emerge from the solution of the problems:

- Build MECL circuits using PC boards with at least three layers for V_{CC} V_{EE} and V_{ref}; use a single resistor returned to V_{ref} for each backplane wiring termination, and

- Divide high bit rate data streams and clocks by two or more to provide parallel bit streams at lower frequencies. The logic operations can then be performed with a minimum of circuitry running at high rates.

The second DRU (designed and built in accordance with the above criteria) was much easier to test and make operational.

The success of the redesign was so significant, in fact, that the performance of the DAU suffered by comparison. Thus, the DAU was also reworked to have a -2V reference for terminating all 200 Mb/s circuits. Performance was then satisfactory up to 230 Mb/s.

Figure 4 shows photographs of the total 200 Mb/s data stream, both formats the analog data bits with the digital sources enabled, and a comparison of the generated sawtooth with the sawtooth recovered from the demultiplexed data stream (same for both formats).

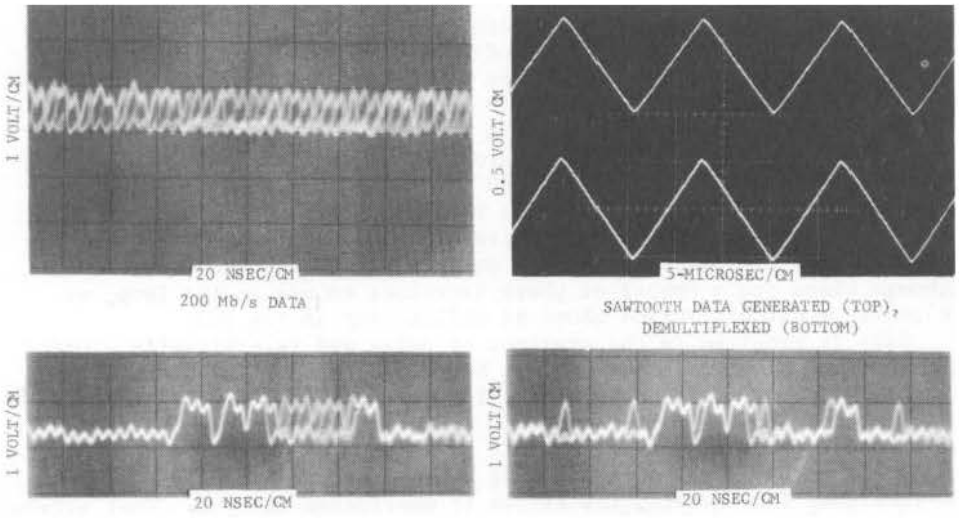

Figure 4. Typical Data Waveforms

All discussion to this point described the system operating without induced noise in the data link. One objective of the task was to demonstrate acceptable synchronization and data decommutation in the presence of 10^{-8} bit errors. Therefore, the noise generation circuitry built into the DRU was made adjustable to permit random bit error rates from 10^{-9} to approximately 4×10^{-7} . None of these random error rates had any appreciable effect on system performance. There were no sync dropouts during a typical run; the worst error rate occurred in the analog channel words. The latter was measured at apprxoimately 5×10^{-6} , with a random bit error rate of 4×10^{-7}.

In addition to random error noise, it was also desirable to simulate noise to produce burst or block errors. Although no limit criteria was defined, test results showed that sync dropouts do not occur with noise bits of 5.5 (10^{-7}). The analog word error rate, however, increases to about 24 (10^{-4}), which is still acceptable. If the burst error rate exceeds 10^{-5}, the sync dropouts increase significantly (to nine or more in a five second interval), and analog word errors increase to over 10^{-3}, which is excessive. The ability to regain sync after a sync loss, however, was successfully demonstrated. Resynchronization was always acquired in 588 major frames. This can be identified as the minimum number required to cycle through a missed sync comparison (with the type of noise simulation used).

Figure 5 shows photographs of the 19" rack mounting breadboard.

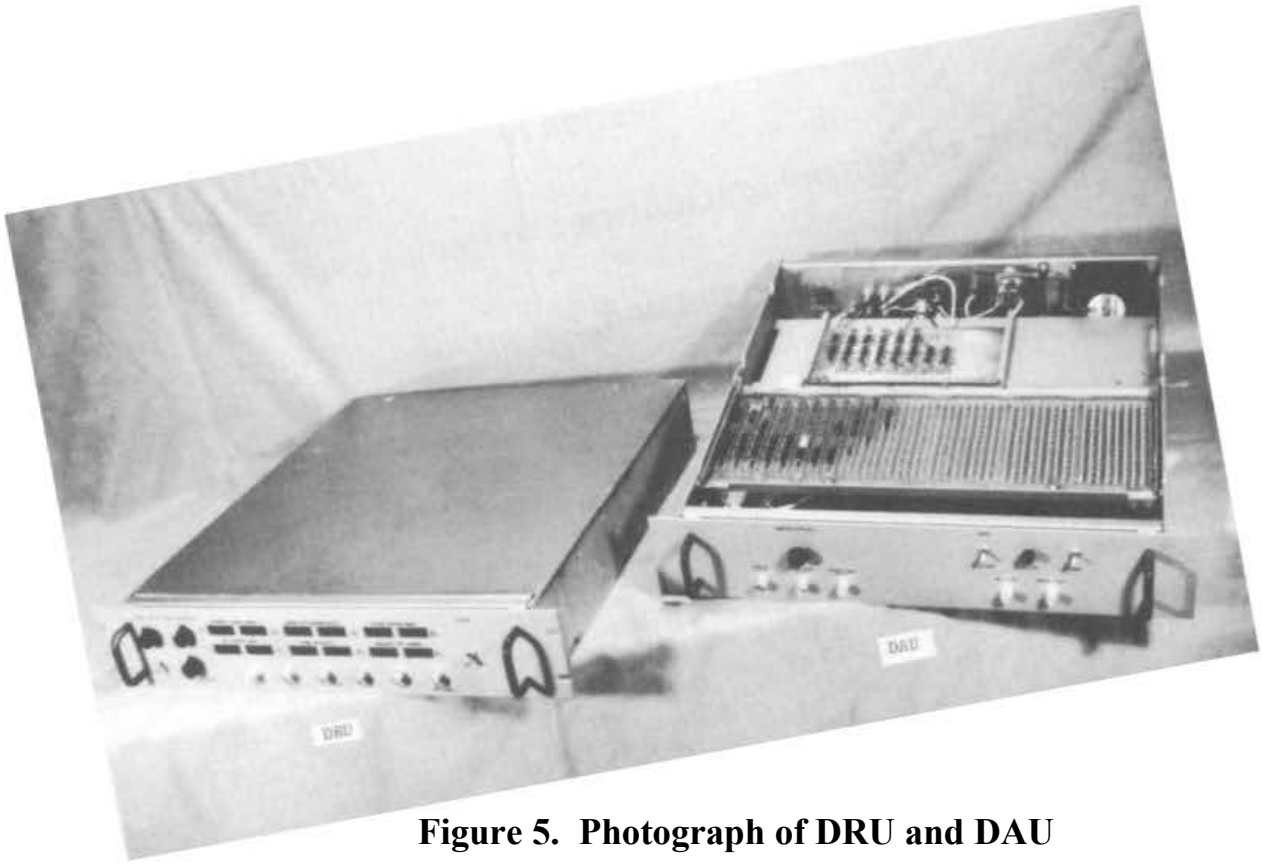

Figure 5. Photograph of DRU and DAU

Conclusions It is realistic to state that all objectives of the task to develop the 200 Mb/s data handling simulator were realized. It was shown that available IC's can be utilized to implement such high rate data systems (at least in laboratory environments), although some components must operate close to their limits. The best was to implement high data rate systems appears to be "do only those operations at the highest frequency that are necessary to get there". Use at least 3-layered pc boards layed out to rf-criteria. for ECL circuits when operating above 100 MHz, unless only a very few components are involved.

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