DIGITAL CLOCK RECOVERY SCHEME MASKS TAPE ERRORS

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1. Summary. The bit error rate (BER) of the tape recorder is a primary factor in determining the overall accuracy of a space to ground PCM data link. The ultimate goal is to obtain a recorder BER signature that is dependent solely on tape quality; however, in practice, the BER may be several orders of magnitude worse than the goal. Usually this occurs when the data transfer rate is not preserved during dropout intervals – intervals where the net signal-to-noise ratio is insufficient to guarantee valid data cell boundary detection.

This paper investigates tape dropout signatures and addresses the problem of maintaining time coherency between reproduced data and clock assurance throughout the dropout interval. A digital approach is presented that utilizes a dual threshold detector in conjunction with a clock recovery generator. The generator is synchronized to the tape signal by a clock, N-times the data transfer rate, coherent with the transport servo reference.

Implementation of the approach is discussed for two popular PCM formats. The effectiveness of the approach as a function of cell boundary detection, system signal-to-noise ratio, and transport time base error (TBE) is considered.

2. Introduction. Digital data retrieved from magnetic tape are inherently low level analog signals that exhibit a zero axis crossing for each flux reversal recorded on tape. The signature of this signal is characterized by finite amplitude modulation attributed to temporary loss of intimate head-to-tape contact. When this effect reduces the signal-to-noise ratio below the threshold of reliable detection, an error is generated. Failure of the recorder electronics to preserve the data transfer rate over such intervals implies that the frame rate of the PCM data train has been disturbed. That is, the ground based equipment will lose frame synchronization (bit slippage). Consequently, the invalid data interval begins with the original error and lasts until frame synchronization is regained.

In past PCM data links involving spaceborne tape recorders, the problem of bit slippage was avoided by eliminating the source of the error. Stringent tape selection and tape

conditioning combined with moderate tape transition densities allowed for virtually errorless performance of the tape recorders.

The PCM data links of the present and immediate future however, have generated total data storage requirements an order of magnitude greater than was previously available. To satisfy this need and still fall within the boundaries of size and weight constraints, multitrack parallel recording techniques, operating at high tape transition densities and yielding finite error rates, must be used. These requirements, coupled with the trend to further reduce recorder induced errors via error detection and correction systems, have led to the use of clock assurance techniques in the reconstruction electronics of the recorder.

The common denominator in all past research relating to clock assurance is the phase lock loop (PLL). Although implementation techniques vary, the basic concept remains the same. In essence, the PLL consists of a voltage controlled oscillator (VCO) that is phase locked to the signal generated from the tape zero axis crossings. In the presence of normal data, the VCO output will generate a strobe having a rate equal to the data transfer rate and phased to fall at the mean position dictated by the data decoder limits. In the presence of a data dropout, the VCO strobe will continue to supply decoder clocks at the mean data transfer rate and (hopefully) rapidly reacquire lock without introducing additional post-dropout TBE.

For a given application, a figure of merit may be assigned to a PLL design based on its ability to have sufficient:

- Bandwidth to track the TBE (integral of flutter) of the tape transport
- Frequency stability of the strobe during a dropout versus temperature and life
- Slew rate during transition from dropout to normal data

The PLL is inherently an analog device; and consequently, interaction between these performance parameters cannot be avoided.

This paper theorizes that the function of the PLL can be implemented by digital techniques. These techniques are conducive to eliminating the interaction between performance parameters and to providing explicit performance boundaries.

3. Design Criteria. The design criteria established for clock reconstruction are:

- The reconstructed clock must follow the instantaneous changes in transport speed and electronic jitter without accumulating excessive phase error.

- The clock reconstruction circuitry must maintain the clock timing signal in the absence of data transitions.

If either or both of the above criteria are not satisfied, it is conceivable that the bit synchronizer will lose frame synchronization as the result of an addition or subtraction of a single clock interval.

In order to keep within a safe margin of the first criteria, the magnitude of time delay between the reconstructed clock and the disturbance at the head-to-tape interface must be minimized. The fact that the employment of such criteria would result in a jittering clock at this point in the reconstruction electronics is not deleterious. The primary function of clock reconstruction is to maintain the integrity of the timing signal with respect to the data transition on tape. All subsequent dejittering of the clock and data is accomplished by dejitter buffers.

To ensure that the second criteria is satisfied, the reconstruction circuitry must:

A. Define the beginning and end of the dropout zone.

B. Process only valid tape zero crossings.

C. Ensure that the artificial clock and the tape clock are phased coherently.

The dropout zone is defined by considering signal-to-noise ratio of the carrier and establishing an amplitude threshold. The beginning of a dropout zone is marked when the signal amplitude falls below the threshold for a time interval equal to or greater than 1/2 of a bit-cell interval. When the signal amplitude increases to above the threshold for a period equal to or greater than one bit-cell, the end of the dropout zone is detected.

Actual photographs of tape dropouts taken from a Bi-Ø-Level format are shown in Figure 1. The significance of these photographs lies in illustrating the two basic problem areas associated with dropout recognition.

The first problem to overcome is to insure that the detected zero crossings are independent of finite circuit hysteresis before the analog signal amplitude reaches the threshold of the dropout detector.

The second problem is related to making the dropout detector immune to spurious indications when the dropout amplitude hovers at or near the dropout threshold selected.

To ensure that only valid zero crossings are processed, provisions must be made in the clock assurance circuitry to eliminate the invalid transitions which are encountered at the boundaries of the dropout zone. Once the dropout zone has been detected, timing signals (that are generated from the reference source) are used to ensure that the reconstructed clock does not lose its phase relationship with the data transitions during the dropout period.

Under these conditions, then, the clock is considered assured as long as the time base error buildup (contributed by all sources of transport and electronic components) does not exceed ± 1/4 of a bit-cell time interval.

4. Design Considerations. In the digital scheme described, a clock, N-times the data transfer rate, coherent with the transport servo reference signal, is used to sense a data transition on tape to within 1/N of a data cell. The data cell itself is divided into N equally spaced increments. A cyclic counter that is resetable by the tape transition is used to generate the desired timing signals for data decoding.

4.1 Resolution. Resolution relates to the bit-cell guardband that must be allowed between the clock edge and the data cell transition being decoded. This guardband is necessary in order to take into account variations in logic element characteristics such as propagation delay times and flip-flop setup times. The resolution is most generally expressed by the relationship:

$$\text{percent resolution} = \frac{\epsilon_g}{\epsilon_a} \times 100$$

where ϵ_g = the guardband in nanoseconds

and ϵ_a = the nominal bit period in nanoseconds.

The major tradeoff for increasing resolution for a digital decoder is the power required to operate high speed logic elements.

4.2 Error Margin. Error margin differs from resolution in that this parameter takes into account variations between transition intervals as a result of time base instability. There are two sources of time base instability:

A. Nonlinear phase transfer characteristics of the head-to-tape interface.

B. Tape transport flutter.

By employing phase equalizers in the analog portion of the reproduce electronics, the major ill effects of phase distortion are normalized. However, there is always a net uncompensated phase distortion that induces a bit-to-bit jitter that is a function of the data content and is considered a non-cumulative error. The magnitude of bit-to-bit jitter is obtained by measuring the time base signature of the phase equalized electronics output. This signature will vary slightly as a function of head-to-tape interface constants and PCM format selected. Sufficient samples of empirical data have established the maximum limits for this quantity to be within 10 percent of the data period.

On the other hand, tape transport flutter, when integrated over a given tape length, will induce a TBE that is directly proportional to the magnitude of flutter and inversely proportional to the flutter frequency. The overall error margin must take into account both error sources.

The extent to which the time base error signature influences the design margin of the decoder is dependent on the magnitude of the differential time delay existing between the reconstructed clock transition and the tape transitions being decoded. By using digital techniques, the differential delay between the reconstructed clock strobe and the data transition is insignificant. Therefore, the allowable percentage deviation of the bit rate for proper decoding is independent of the frequency of this deviation.

4.3 Artificial Clock Generator. The coherency that exists between the sampling clock and the data transfer rate is conducive to an explicit solution to assuring clock timing integrity throughout the dropout interval. The phase of the last valid transition is stored in the cyclic bit counter and circulated at precisely the transfer rate. The only dependent variable that limits the clock assurance interval is the time base error accumulated over the entire dropout length.

5. System Operation for Bi-Ø-Level Formats. A block diagram for a Bi-Ø-Level decoder employing digital clock assurance is shown in Figure 2. Principle waveforms for the block diagram are shown in Figure 3.

The signal supplied by the analog signal conditioner is processed through two parallel paths. The invalid data detector provides the means for rejecting all data below a predetermined peak-to-peak threshold (symmetrical about the zero axis). The second detector, consisting of a limiter and Schmitt trigger, provides unrestricted zero crossing detection.

The dual threshold allows the dropout margin to be adjusted to fall within the signal-to-noise ratio constraints of the system while not inducing time base distortion for valid transitions near the boundaries of the invalid data settings. The gated 1/4 bit delay takes

into account the maximum phase shift inherent in the invalid data detector as the input signal approaches the threshold setting.

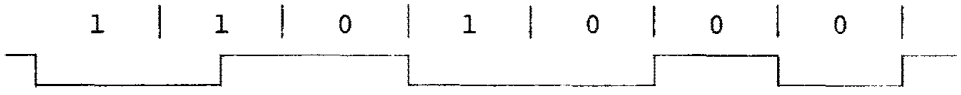
During normal data operation, the leading and trailing edges of the data are detected and passed through the cell-boundary detector implemented to pass only cell-center transitions to the reset input of the cyclic counter. A dropout is sensed whenever a leading or trailing edge occurs at the time invalid data is sensed.

During the dropout interval, the valid transition gate inhibits any further resetting of the counter; therefore, the counter will cycle at the bit rate. The 1/4 bit delay is also gated off at this time. This is to ensure that noise from the Schmitt trigger does not introduce a false transition when exiting a dropout region. The dropout detector is also sampled by the bit rate clock. Resetting of the dropout detector occurs only when a complete bit cell of valid data has been detected.

6. System Operation for Delay Modulation Formats. A block diagram for the delay modulation (DM) decoder employing digital clock assurance is shown in Figure 4. Principle waveforms needed for following the signal flow are shown in Figure 5.

A comparison of the block diagram between the Bi-Ø-Level and DM systems shows the commonality existing between the required functions. The major difference lies in the extension of the cyclic counter to two bit-intervals and the arrangement of the counter outputs. These outputs extract the clock during normal data and provide additional timing signals when operating in or exiting from a dropout region. Since the clock assurance timing is an integral part of the cyclic counter, the subsequent discussion will also include decoder principles of operation for reference.

6.1 Delay Modulation Format. The DM format described here has identical transfer characteristics to the more popular Miller code; however, the logic rules used for encoding are different.



Delay Modulation Example Format

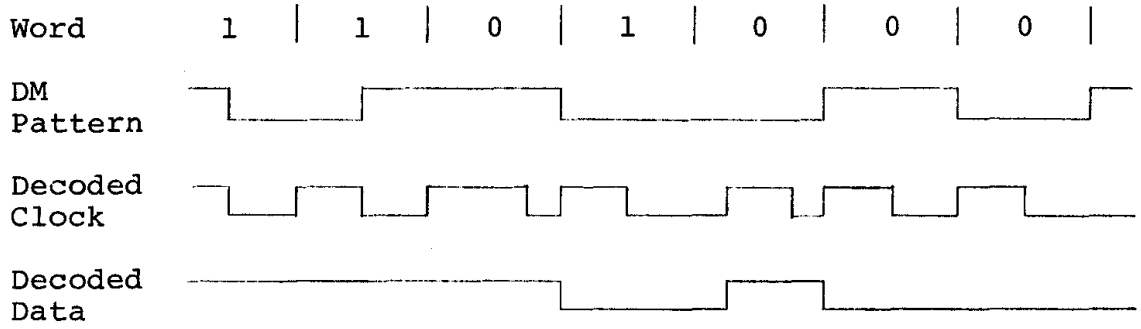
As shown in the figure, the rules for data transitions are as follows:

A. Logic “0” is represented by a transition at the end of a bit cell.

B. Logic “1” is represented by a transition in the center of the bit cell if the previous bit was also a “1”; however, if the previous bit was a logic “0”, a “1” is represented by no transition in that bit cell.

From the example, it may be seen that the decoder must distinguish between three different data periods. Resolution of the decoder must allow for an increase or decrease of bit periods due to recorder TBE and transition displacements due to head-to-tape interface nonlinearities.

6.2 Decoding Method. A high frequency clock, which is phase locked to the transport servo reference, is used in such a way that exactly 24 clock pulses occur between transitions of the shortest delay modulation period. The example below shows the clock and data decoded from the delay modulation data pattern.



6.2.1 The clock output is determined by decoding 12, 30, and 42 clock pulses. The rules for determining the decoded clock output are as follows:

A. A transition always changes the state of the NRZ clock output.

B. Decoding of the 12 or 30 clock pulses always causes a change of state of the NRZ clock output.

C. Decoding of 42 clock pulses always causes the NRZ clock output to go to “0” state.

6.2.2 The rules for decoding to NRZ data are as follows:

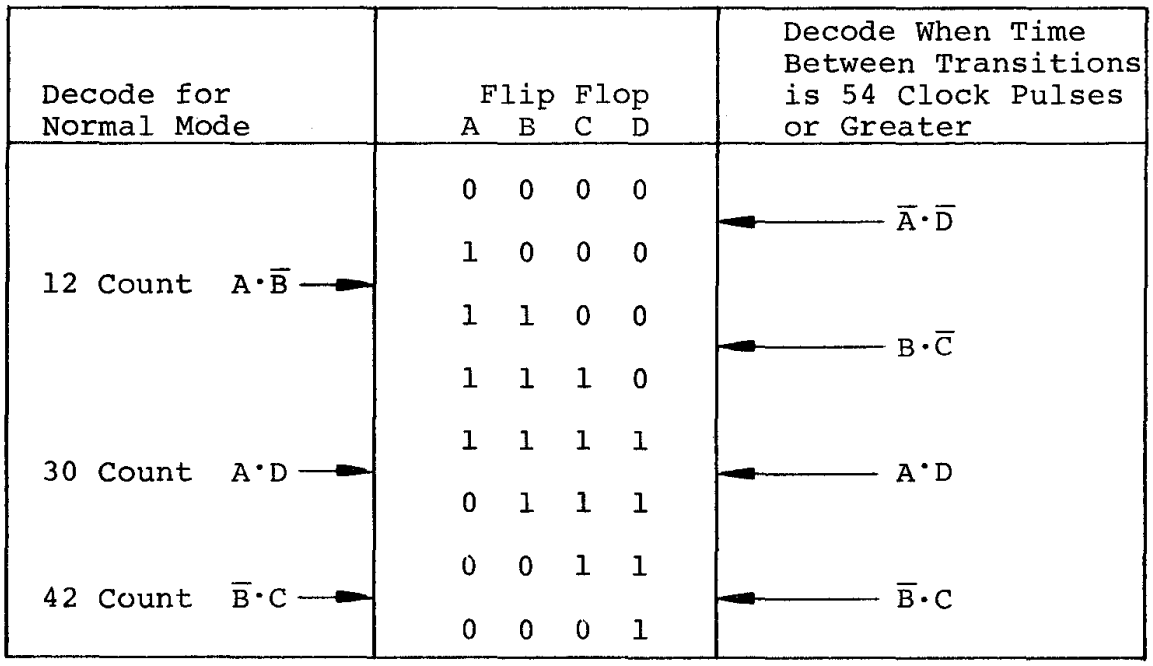
A. If the clock is a logic “0” and 12 or 30 clock pulses are decoded, the data out is “1”.

B. If the clock is a logic “0”, and a data transition occurs, data out is a logic “0”.

C. For any other case, there is no change in data out.

6.3 Method of Counting. The cyclic counter is divided into a modulo 6 counter that in turn clocks a modulo 8 counter. Reset of the cyclic counter occurs with each edge detection pulse. Counting and decoding will then continue until the next edge detection pulse.

Figure 6 shows the state sequence of the modulo 8 counter and the decoding associated with this counter. The decoding shown on the left of the count sequence is the NORMAL mode which is used when converting from DM to NRZ. The NORMAL mode decoding occurs when the time between transitions is less than 54 clock pulses. Should the time between transitions be 54 clock pulses or greater (as in a dropout), then decoding will be as shown on the right of Figure 6. Decoding will then continue to be that shown on the right of the figure until the next edge detection pulse causes decoding to revert to the normal mode.



Count Sequence - 8 Count

Figure 6

During the dropout, the DM decoder will continue to generate NRZ clocks until the longest possible DM bit width has occurred. This period would, for normal DM, occur during a 0-1-0 pattern, and is nominally 48 of the x24 clock pulses. Allowing for bit width distortion, the decoder waits until 54 clock pulses have occurred from the last transition. It will then cause artificial NRZ clocks to be generated until such time that transitions are declared valid. Thereafter, it will revert to its normal mode of decoding.

During normal decoding, the 42 count pulse is used to reset the NRZ clock flip-flop. This is the method of synchronizing the phase of the NRZ clock on the 0-1-0 pattern. However, during a dropout, the 42 count cannot be used to reset the NRZ clock flip-flop, or the phase of the clock prior to the dropout will not be preserved. Hence, during a dropout the counter decoding is changed such that the 42 count toggles the NRZ clock flip-flop instead of resetting it.

7. Conclusion The primary objective of this paper is to communicate the need for improving present and future tape recorder performance and the applicability of digital techniques to satisfy these needs. This design tool offers an alternative to the analog PLL and allows the designer to make a tradeoff between the two techniques and, consequently, achieve a more optimum design.

Since development of digital clock assurance techniques in 1971, Bi-Ø-Level as well as delay modulation applications have been used in four NASA sponsored and three Air Force sponsored recorder programs. However, the full potential of this digital technique is far from being realized. In some newer development programs, the digital approach has been expanded to include applications for continuously variable transfer rates as well as wide range rate seeking decoders.

In both the current digital clock assurance techniques and the expanded techniques, the primary conflict is power the conflict between the power allotted to the recorder and that which is required by the high speed logic elements associated with digital clock assurance techniques. Future applicability of these digital techniques will be influenced by the recorder power budget (high enough to match the increased functional complexity required) or by any improvements in the bandwidth/power ratios of the logic families used by the designer.

8. Acknowledgments. The author wishes to express his appreciation to Stephen Siegel (co-author of Digital Clock Assurance) and to Charles Lindquist and Al Fisher for their contributions in circuit design.

9. References.

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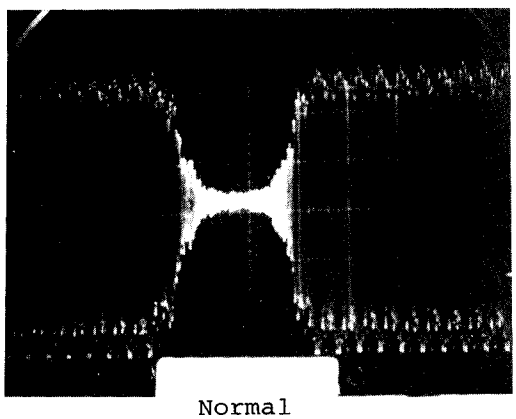
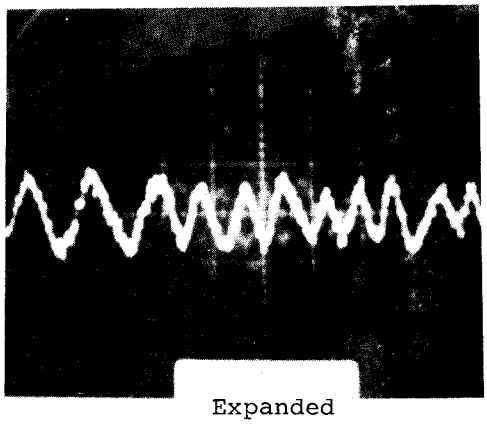
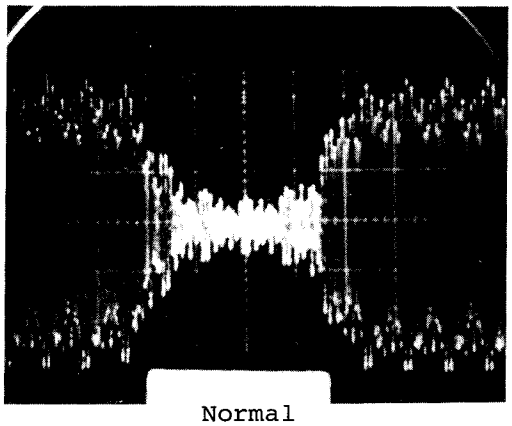


Normal

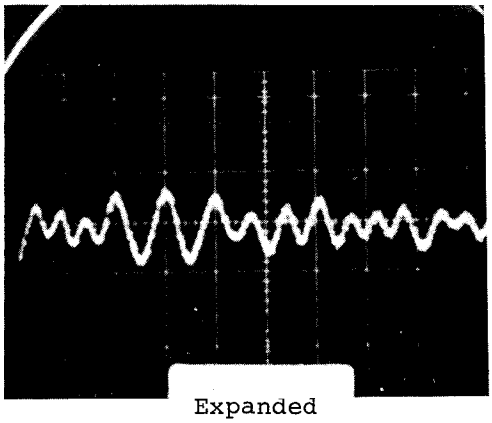


Expanded

A. 26dB Data Dropout With Minimum Phase Displacement Error



Normal



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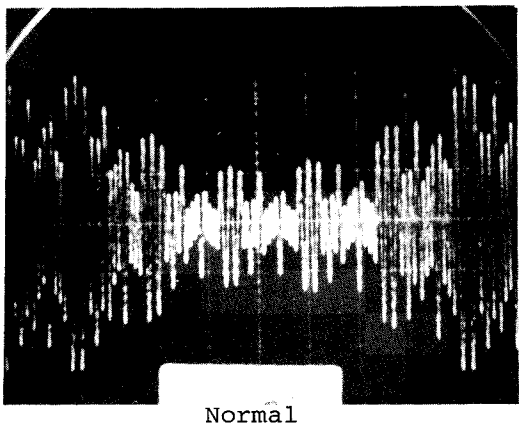
B. 26dB Data Dropout With Low Phase Displacement Error



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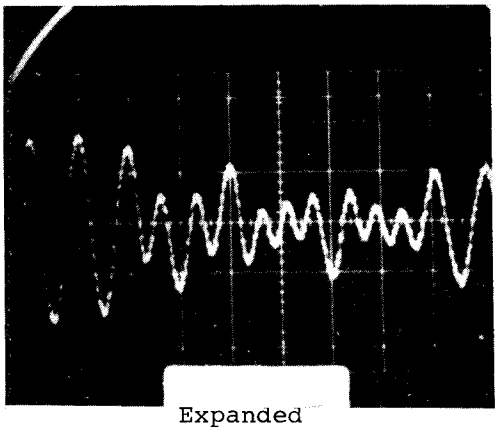
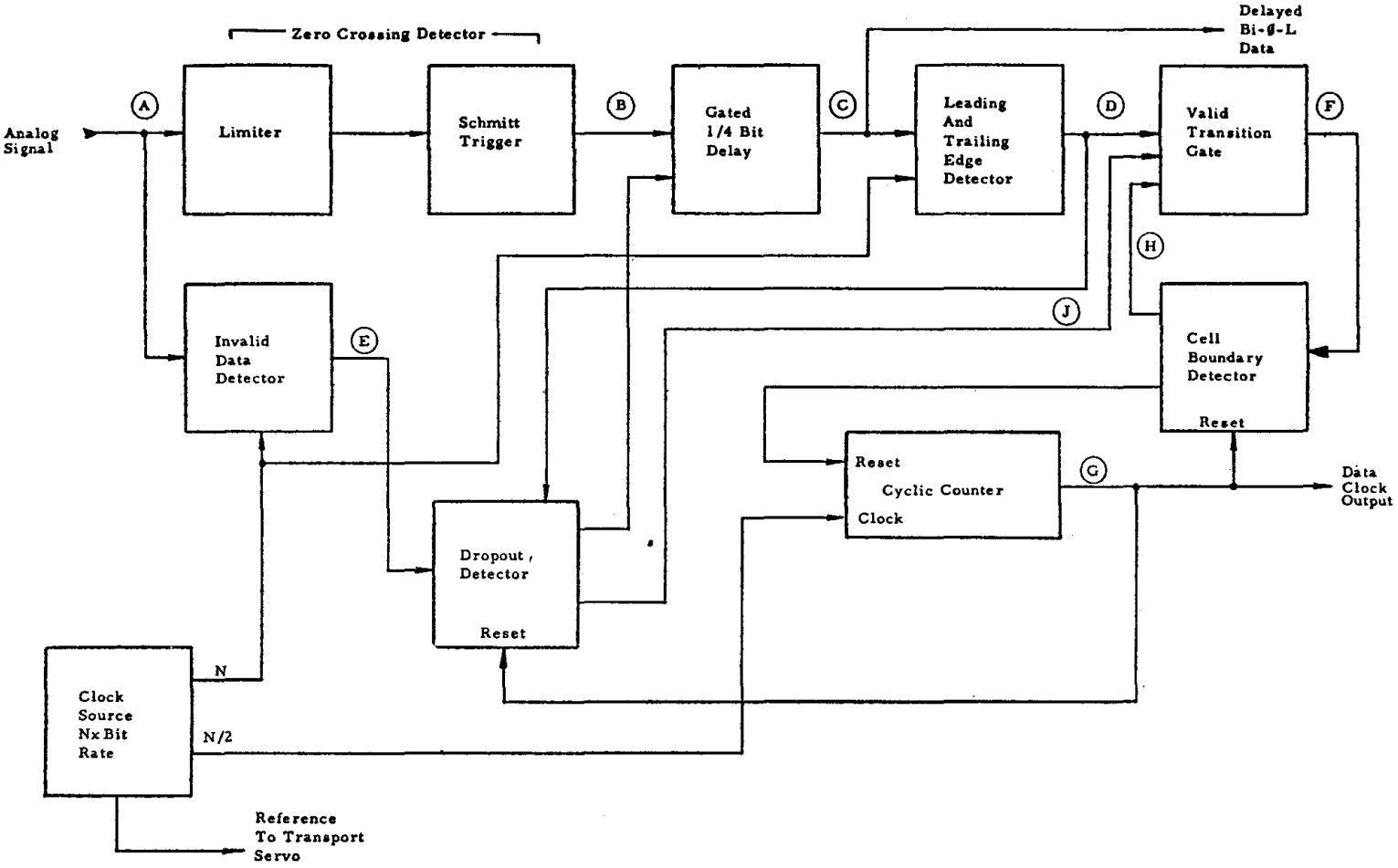


Expanded

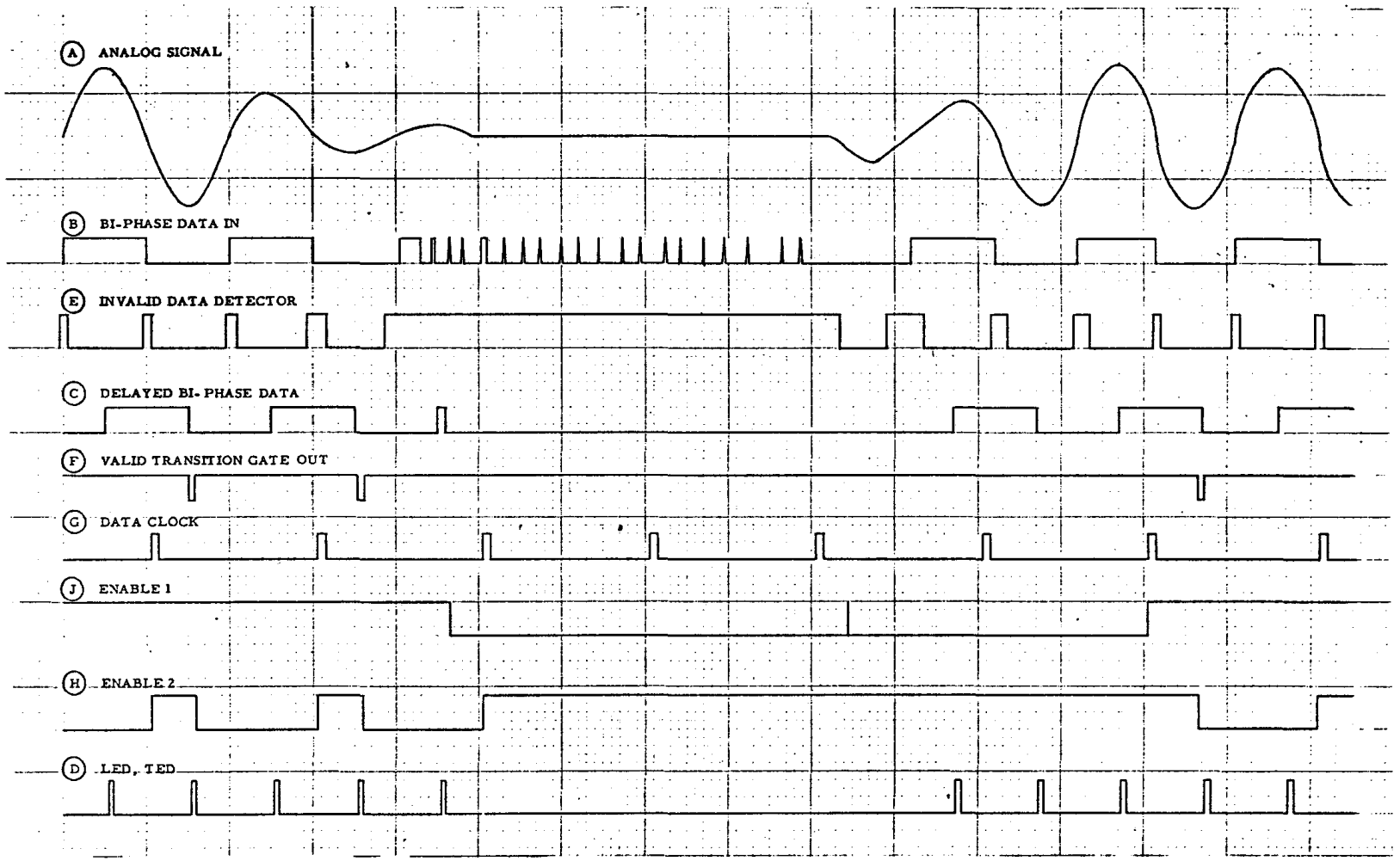
Analog Signals With Data Dropouts Present

Figure 1

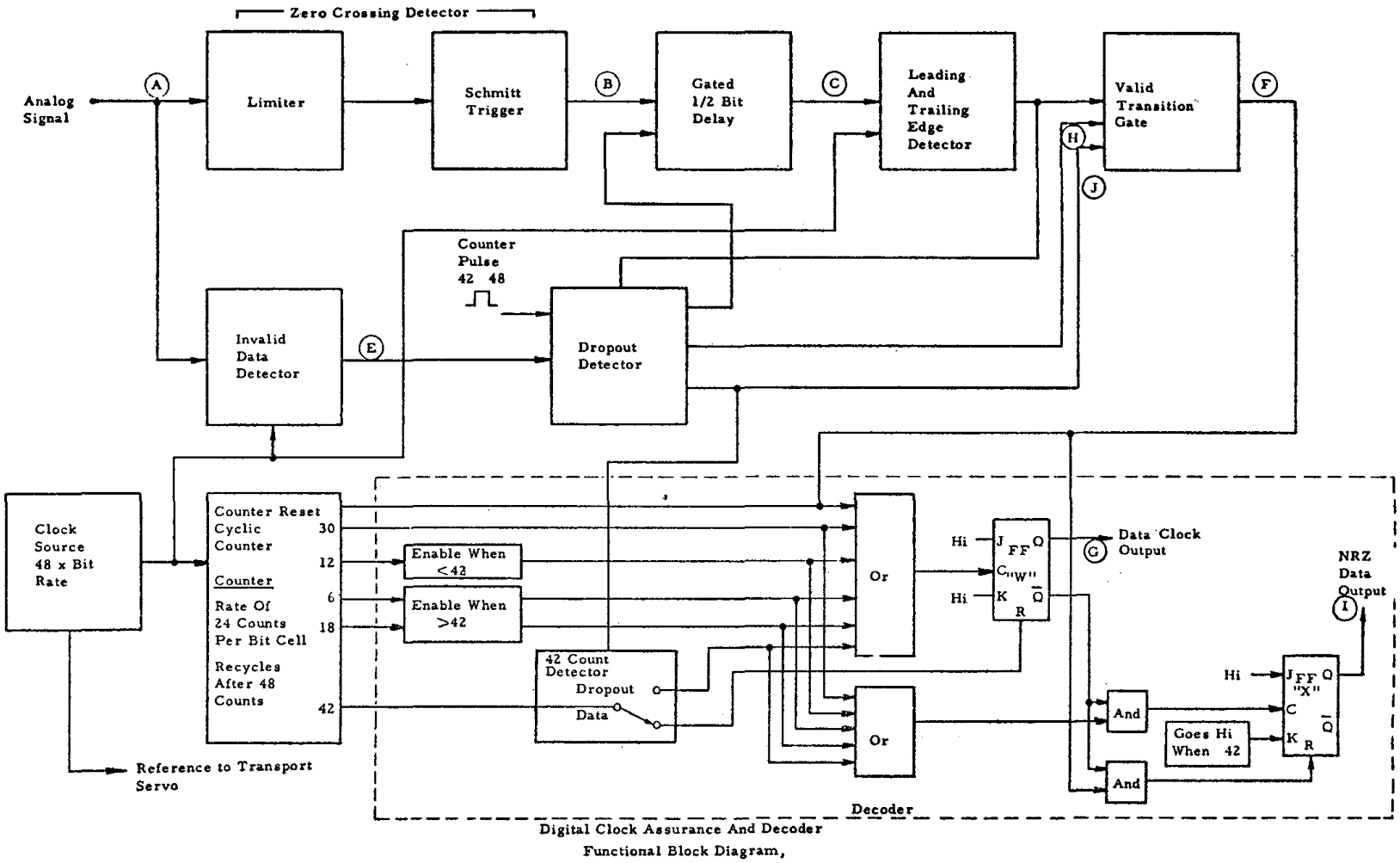


Digital Clock Assurance And Decoder
Functional Block Diagram,
Bi-Ø-Level

Figure 2

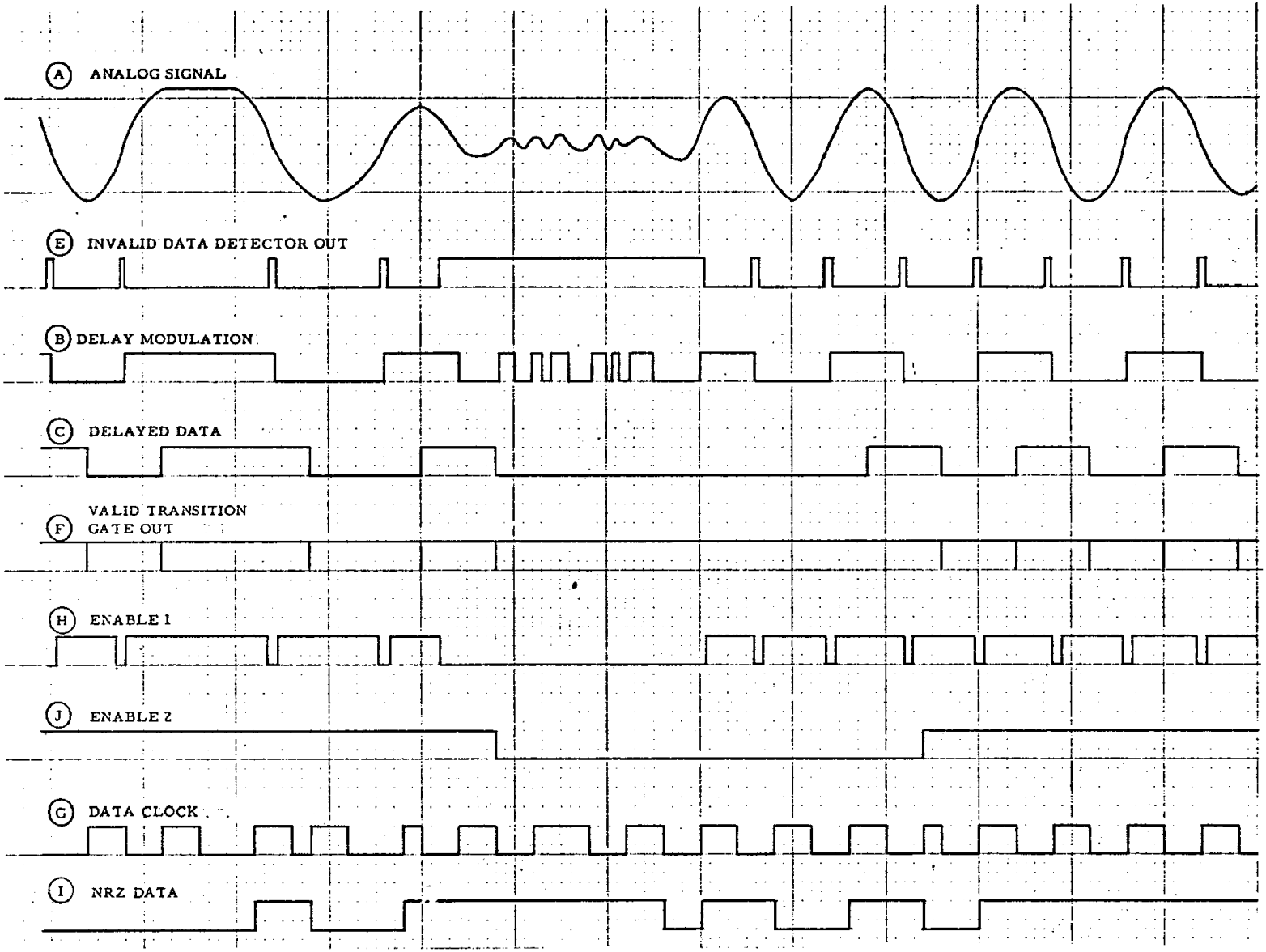


PRINCIPLE WAVEFORMS
Bi-Ø-Level DECODER WITH DIGITAL CLOCK ASSURANCE
FIGURE 3



Digital Clock Assurance And Decoder
Functional Block Diagram
Delay Modulation Format

Figure 4



PRINCIPLE WAVEF ORMS
DELAY MODULATION DECODER WITH DIGITAL CLOCK ASSURANCE
FIGURE 5