MICROPROCESSOR CONTROLLED THICK-FILM PCM TELEMETRY SYSTEM

DEMIRHAN HAKIMOGLU
Vice President of Digital Products
Aydin Vector Division

Summary This paper describes an approach to airborne PCM data acquisition that takes advantage of the latest technological advances in the fields of both the monolithic microcircuits and hybrid packaging. The result is a low cost system that provides a combination of long sought-after features ; flexibility, modular make-up, microminiature size, high reliability and low power.

Introduction The MMP-600 series micro-modular PCM systems exhibit the following distinguishing characteristics:

1. Built-in high reliability provided by completely thick-film hybrid construction. Device-to-PC card connections and card-to-card wiring (potential sources of failures) nonexistent.

2. Micro-miniature size. Typically a 10 cubic inch unit accepts more than 10 multiple-range high-level and low-level analog and bi-level (discrete) inputs, provides up to 10-bit binary resolution and performs most functions found in much larger, sophisticated PCM systems.

3. Modular, expandable design with plug-in module versatility. No longer is it necessary to pin down the types, quantities, signal ranges and sampling rates of the data channels ahead of time. As changes in these parameters become necessary in mid-stream, one can. simply draw upon a library of standard interchangeable modules to meet changing requirements.

4. User changeable PROM (Programmable Read Only Memory) controlled data sampling format flexibility. One can change the entire PCM format in the field by simply replacing or re-programming a single PROM which is accessible upon removing a cover. Sampling formats combining multiple subcommutation and supercommutation rates, as well as the synchronization words are controlled by this PROM.

5. Optional Delay Shift Register Modules that provide delayed PCM output which enables full recovery of data prevailing reentry through ionesphere where RF transmission temporarily collapses.

6. C-MOS logic throughout resulting in very low power dissipation.

Since its first introduction, MMP-600 PCM systems have been fully qualified for harsh-environment space applications and have successfully flown in numerous critical sattelite, rocket, missile and aircraft missions.

A typical MMP-600 PCM system consists of the following standard modules:

PS-607 Power Supply. This module also includes the basic oscillator.

TM-604 Timer. This module provides PCM and test point outputs, and includes premodulation filter.

FM-618 Formatter

PR-614 Processor

AD-606 Sample and Hold and Analog to Digital Converter

EP-612 End Plate. This module contains the removable PROM

The following modules are used in variable quantities depending on the data input requirements:

MP-601 32-Channel High-level Analog Multiplexer

MP-608 16-Channel Differential Analog Multiplexer

MP-602 3-Word (up to 30 bits) Bi-Level Multiplexer

LA-609 Differential Amplifier

SE-610 9207-bit Delay Shift Register

SR-611 9207-bit Delay Shift Register with Premodulation Filter

FL-619 Quad Filters

CONSTRUCTION AND PACKAGING

Vector series MMP-600 PCM Systems are fabricated completely by the processes and materials of thick-film hybrid technology. The system is completely modular, resulting in a plug-in expansion capability. Each module is housed in a rugged aluminum alloy frame with built-in peripheral hermaphroditic connection system that allows adjacent modules to plug directly into each other (see Figures 1, 2, and 3). Each module is completely covered and sealed, and is factory-repairable. External electrical functions are introduced directly into the appropriate module via microminiature, metal shell 37-pin or 9-pin connectors.

The over-all dimensions of each module are 1.7 inches by 1.5 inches by 0.25 inches high except the Power Supply and End Plate modules which are 0.687 inches and 0.440 inches high respectively. The housings are precision machined and final finished with electroless nickel resulting in excellent electrical bonding, interference shielding and corrosion protection.

Each module, except the end plate, contains a thick-film multilayer wafer assembly. Integrated circuits, transistors and diodes are interconnected on a multilayer ceramic substrate. The substrate also contains screen printed thick film resistors and attached monolithic ceramic capacitors. Compared to assembly of discrete packaged devices, hybrid assembly offers increased reliability which results from elimination of two complete levels of connections; those from device to printed circuit board and those from module to the mother-board.

Each module uses a 1.25 inch x 1.00 inch x 0.025 inch, 96 % alumina substrate. This provides a firm base with suitable thermal dissipation and dielectric properties. The basic construction of the thick film substrate is a multilayer ceramic structure formed by screen printing and individually firing successive layers of metallization separated by a crystallizable glass dielectric film. Conductive metallized interconnect patterns are formed by screen printing and firing a suitable gold ink material. This technique provides excellent adhesion and is suitable for thermal compression gold wire bonding. For soldering leads to the terminals of the substrate, a high adhesion (3000 psi) platimum-gold conductor is used with excellent solder wetting and leach resistance characteristics. All semiconductor devices are mounted to the substrate with a 100% solids, single component, conductive epoxy which contains fine gold powder and which does not outgas at temperatures up to 190°C.

Suitable resistor inks are used for most resistors. Where ultra-stable microminiature resistors are required, thin film tantalum nitride chip resistors with ±2 ppm/°C tracking characteristics are used. Thermal compression stitch bonding and ball bonding with 0.001

to 0.0015 inch diameter gold wire is used to interconnect the semiconductor devices to the gold thick film metallization.

FUNCTIONAL DESCRIPTION

The functional block diagram of the MMP-600 PCM system is shown in Figure 4. Any combination of single ended and differential analog and bi-level (discrete) data inputs are accepted by this system. Single ended high level analog inputs are time-division multiplexed by the MP-601 modules. Differential analog inputs, which can be low level or high level, are multiplexed by the MP-608 modules. The multiplexed differential signal is further conditioned by the LA-609 differential amplifier and merged with the high level PAM signal which is fed to the AD-606 sample and hold and analog to digital converter module. The A to D converter digitizes each analog sample into a binary number with up to 10-bit resolution (one part in 1023). This data is fed into the formatter module, FM-618, which also receives the multiplexed bi-level data from MP-602 modules. The formatter provides accurate threshold detection for bi-level inputs, merges them with the digitized analog data, inserts frame and subframe synchronization words and feeds the resulting composite multiplex data train to the timer module, TM-604, in serial form. The timer converts this data to desired PCM codes (NRZ, Bi-Ø, and Miller, Mark or Space), generates parity bit if required and provides premodulation filtering. Test outputs such as bit clock, word clock and frame sync pulses are also provided by the timer module.

The operation and timing of the entire system is under the control of the processor module, PR-614, which functions as a microprocessor executing the software program entered into a 256 x 8 programmable read only memory (PROM).

The MMP-600 employs a synchronous isolated power supply, the PS-607 module, which also contains the basic system clock with four externally programmable bit rates. The quad filter module, FL-619, provides four premodulation filters to enable effective filtering of the selected bit rate.

MULTIPLEXING CONTROL

The multiplexing sequence is determined by means of an eight-bit parallel address, A0-A7, generated by the processor module and bussed internally to all multiplexer and amplifier modules. The higher order address lines select a multiplexer module, and the lower order ones select a channel within that module. In the system program written into the PROM, each multiplexer module is assigned a unique address. Since all multiplexer modules of the same type are interchangeable, each multiplexer module is programmed by the user at its external connector to coincide with its assigned address. A module is enabled. when the

program made at its external connector agrees with the state of the address lines which update at the word rate.

Figure 5 illustrates the operation of the MP-601 analog multiplexer module. As shown in this figure, the MP-601 is configured as a stand-alone 32-channel random-address multiplexer in which address lines A5-A7 perform the multiplexer enable function and A0-A4 perform the channel select function. This approach ensures complete interchangeability of the multiplexer modules while providing flexibility in sampling sequence.

The operation of the MP-608 differential and MP-602 bi-level multiplexers are controlled in a similar fashion.

SIGNAL CONDITIONING CONTROL

Differential analog data inputs with multiple signal ranges are accommodated by using an LA-609 differential amplifier module for each signal range to be conditioned. Thus, for example, a system with 48 channels of 0 +50 mV and 15 channels of ±10 mV full scale range will require two amplifiers. Since each differential multiplexer module accepts 16 input channels, 0 +50 mV amplifier will service multiplexed output from three multiplexer modules and the ±10 mV amplifier from one multiplexer module. Figure 6 illustrates the operation of the amplifier module. Address lines A5-A7 control the insertion of the correct amplifier module into the PAM data train during the appropriate channel time slots. Each amplifier can be programmed at its external connector to be enabled during a unique multiplexer address, or a group of addresses. The latter is possible by a “don’t care” program obtained by connecting the desired program points to the corresponding address lines.

THE PROCESSOR

The PR-614 Processor executes the program entered into the 256 x 8 PROM to accomplish the following functional capabilities:

- Multiple subframes and subcommutation rates up to 1/32nd of the minor frame
- Unlimited supercommutation
- Any quantity, bit pattern and location of frame synchronization words

The architecture of the processor is such that, basically only one memory location is required for each input data channel regardless of its sampling rate or the number of output words within a major frame associated with that channel. This technique enables very long major frames (up to 7000 words long) to be attained by a single 256 x 8 PROM. The

maximum number of input channels is 240 (10 bi-level inputs are considered as one "channel" for a 10-bit system) as determined by the available memory capacity after accounting for the special instruction codes.

Figures 7 and 8 show the block diagram and the timing of the processor respectively. A machine cycle of the processor is carried out within a PCM word period. The machine cycle is divided into seven clock periods, T0-T6. During the first clock period, T0, the program counter updates to N. During the next clock period, T1, N is loaded into the address register. During T2, therefore, the memory output represents the contents of location N, hereinafter to be denoted by (N), which can be either a data channel address or an instruction code. Instruction codes are utilized to flag any one of the following conditions that require special treatment:

1. Subcommutated data word
2. Frame ID word
3. Frame sync word
4. End of frame

During T2, (N) is loaded into the instruction register. The instruction decoder interrogates this data for the presence of an instruction code. If negative, nothing further interesting happens until the end of the machine cycle at which time the data channel address is loaded into the output register and bussed to the multiplexer modules.

If, on the other hand, (N) is an instruction code, then the instruction decoder causes the program counter to update to N+1 during T3, and N+1 is loaded into the address register during T4. The instruction decoder further detects which one of the four special conditions listed above is applicable.

If a subcornmutated data word has been detected, then (N+1) is the initial memory address for that subframe, that is, the first of a group of consecutive memory locations where channel address of data inputs sampled in that subframe are to be found. The Arithmetic unit adds the contents of the frame counter to (N+1) to obtain the current subcom memory address. This arithmetic addition is performed under modulo control. The modulo information, which specifies the length of that particular subframe, is part of the instruction code and has been stored in the instruction register. The instruction decoder causes the address multiplexer to enable the current subcom memory address, which, during T5, is loaded into the address register. During T6, the subcommutated channel address, now present at the memory output lines, is loaded into the output register and bussed to the multiplexer modules.

The modulo technique of adding the frame count to (N+1) saves memory space where subframes of different lengths are present in the PCM format. For example, if the length of the maximum subframe in a given format is 32 frames but the length of the particular

subframe being processed is 8 frames then only 9 memory locations (one for each channel in the subframe and one for the instruction code) are required for that subframe. Thus, in this example, when the subframe count is , say, 23 the modulo adder will add 7 to (N+1) since, in frame 23, the 7th channel of that subframe is being sampled.

If the Frame ID Word instruction has been detected, then a command is issued to the formatter module to transfer the status of the frame counter to the PCM output. During the second phase of this instruction cycle (N+1) represents the maximum subframe length of the format. This information is used to reset the frame counter as appropriate.

In the Frame Sync Word instruction cycle (N+1) is the first eight bits of the frame synchronization code. For 10-bit systems, the last two bits of the frame sync code are included as part of the instruction code and stored in the instruction register. During T6, (N+1) is loaded into the output register and a command is issued to the formatter module to transfer the complete frame sync code to the PCM output. The frame sync word instruction can be issued any number of times to obtain the desired number of frame sync words. This instruction can also be issued to insert special words into the PCM format such as the flight number, equipment serial number, etc.

The End of Frame instruction is similar to the Frame Sync Word instruction except that during T3 the Program Counter resets to 0 instead of updating to N+1. The contents of memory location 0 are the first eight bits of the first frame synchronization word. Thus, in addition to marking the end of the minor frame, this instruction also causes the first frame sync word to be outputted.

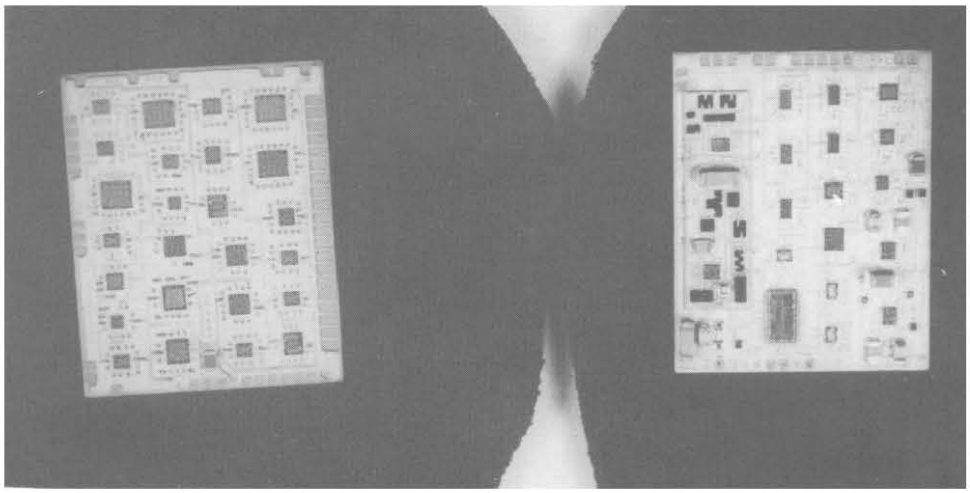


Fig. 1 Typical Multilayer Wafer Assemblies

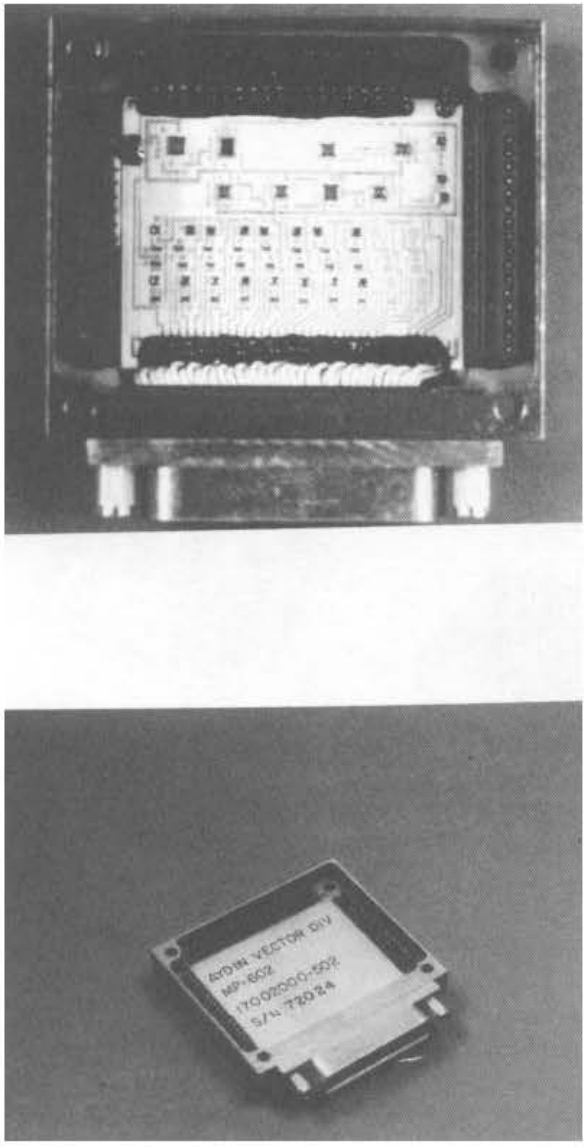
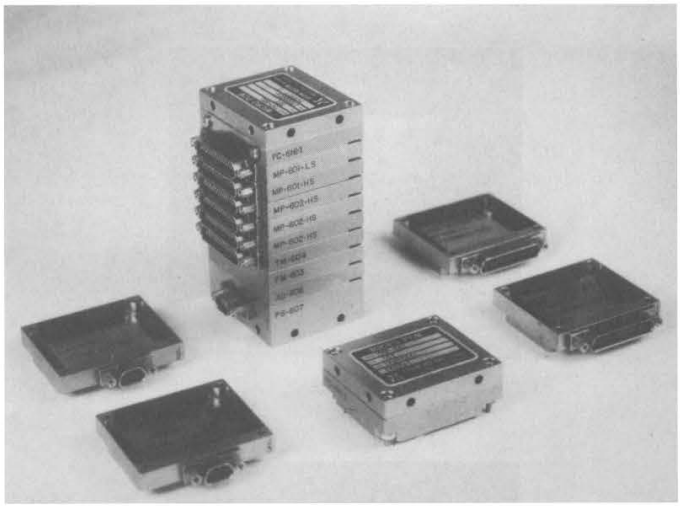


Fig. 2 Typical PCM Module with Cover Off and On



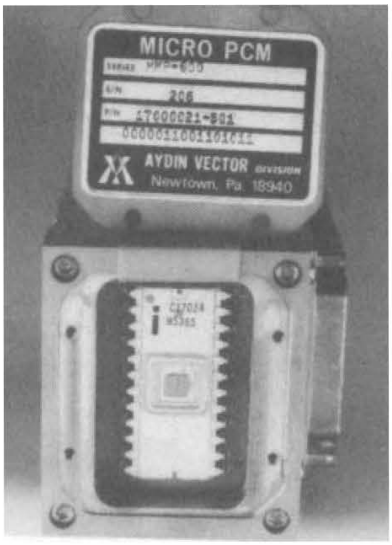


Fig. 3 MMP-600 PCM System with Accessible PROM Device

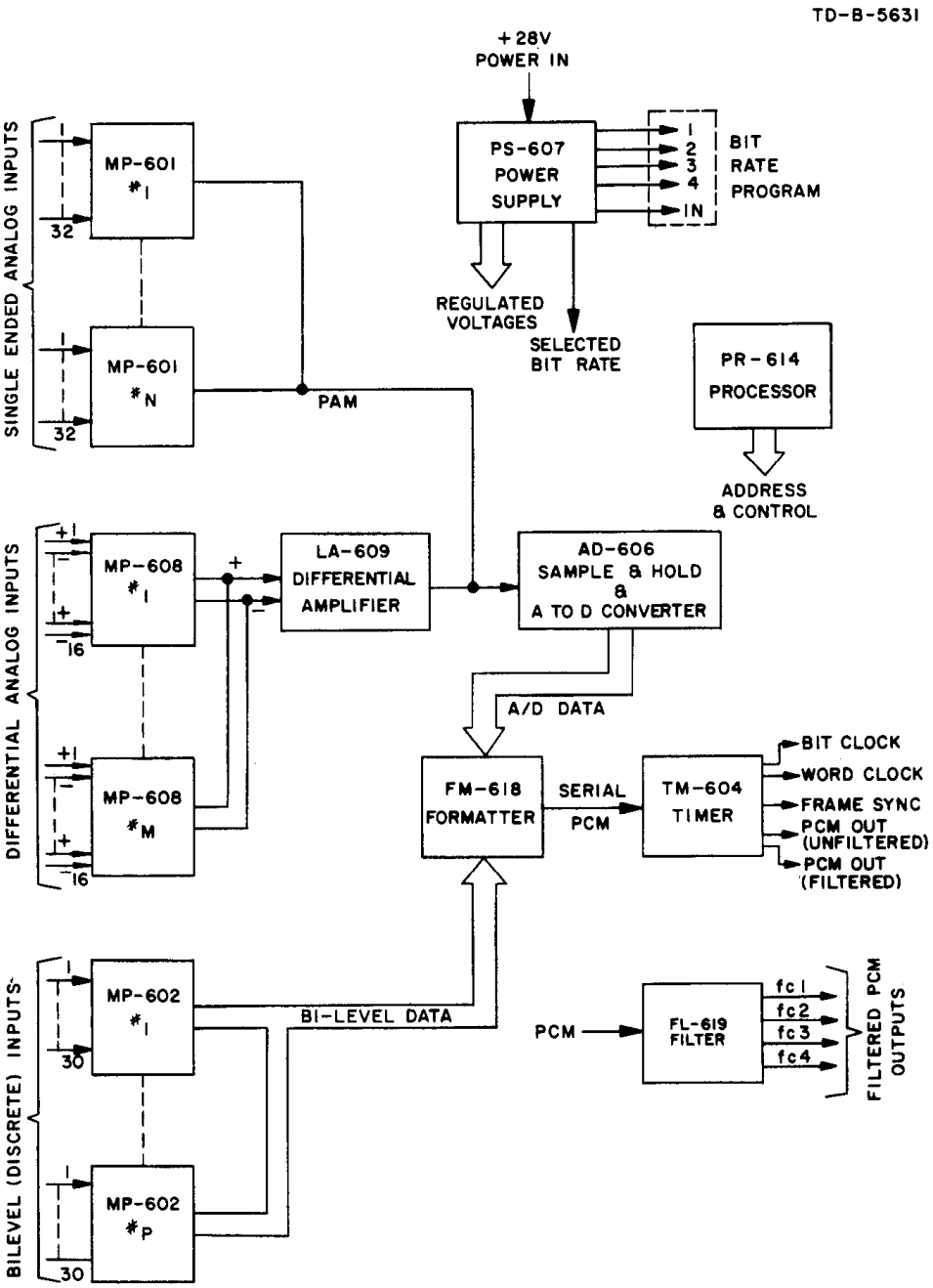


Fig. 4 System Block Diagram

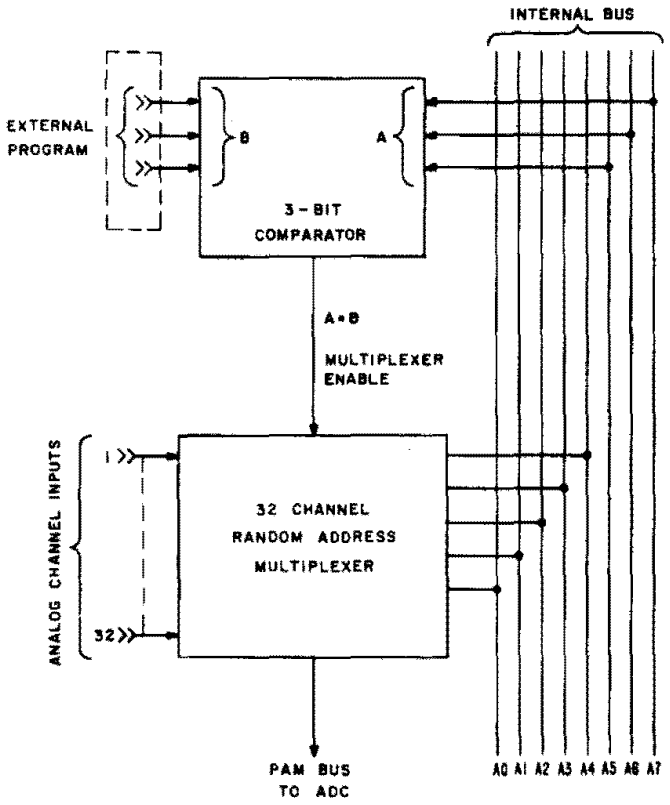


Fig. 5 MP-601 Analog Multiplexer Block Diagram

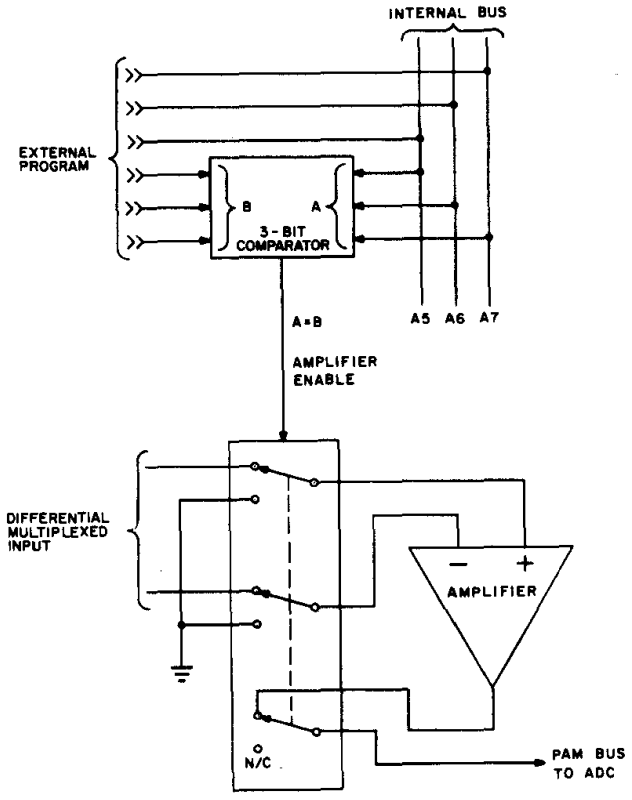


Fig. 6 Differential Amplifier Functional Diagram

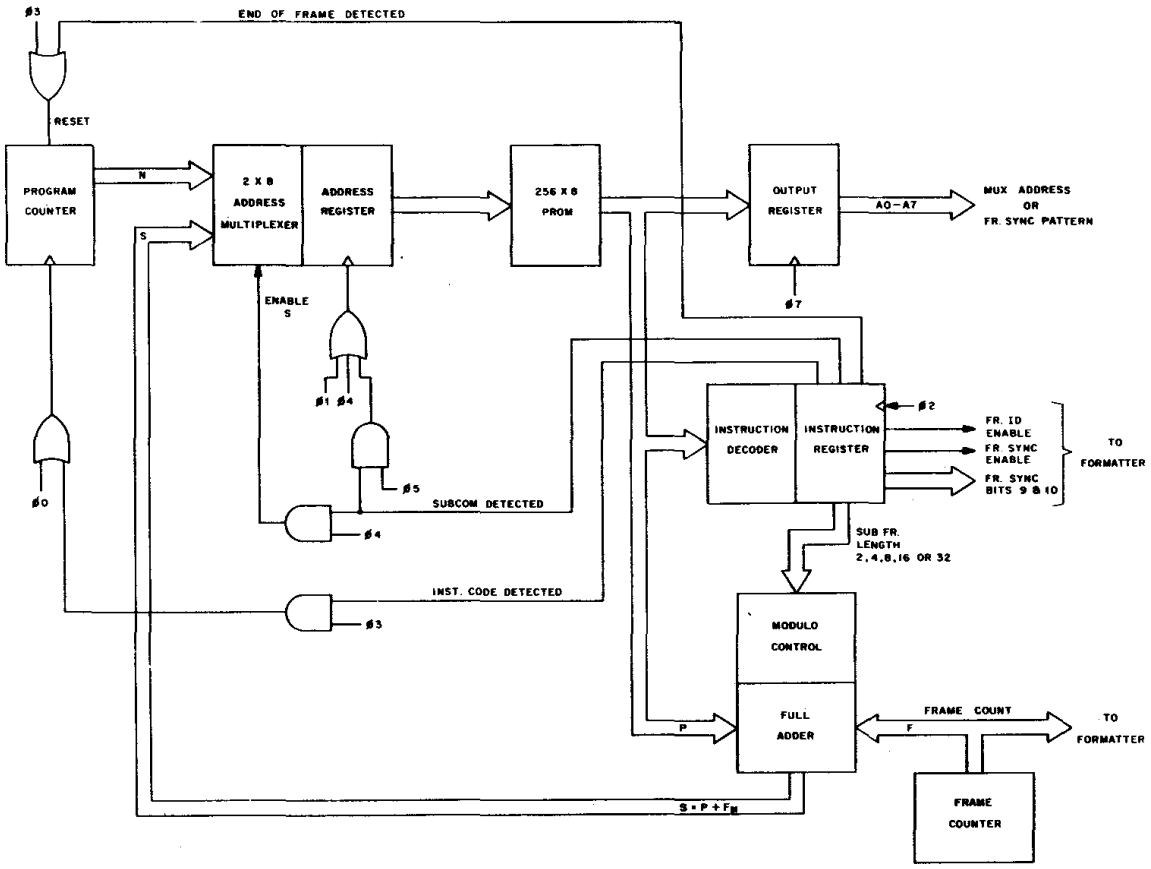
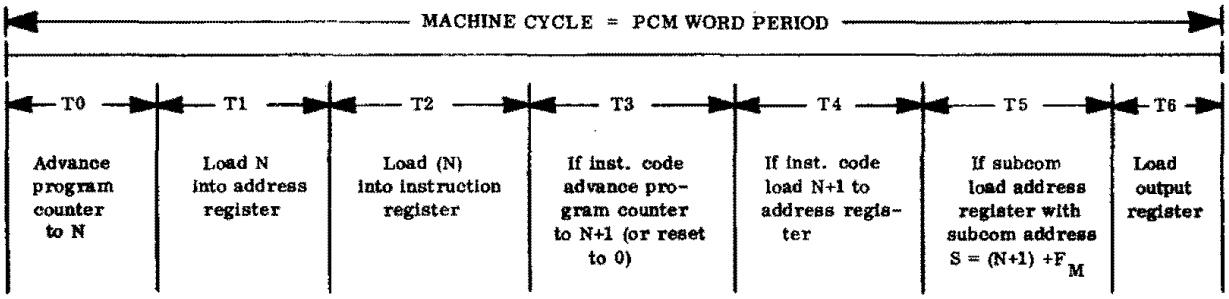


Fig. 7 PR-614 Processor Block Diagram



(N) = Contents of N

PR-614 PROCESSOR

TIMING DIAGRAM

FIGURE 8