SELECTION OF AN OPTIMAL FRAME SYNCHRONIZATION STRATEGY

E. H. STRAEHLEY
Principal of Straehley Associates
Santa Barbara, California

Summary. The operation of preprogrammed and adaptive frame synchronization strategies is simulated, based upon previous mathematical derivations. The simulation, coded in APL, describes operation over a range of Signal to Noise ratios of -4db to +14 db. Both the "Go-to-Lock" and the "Return-to-Search" modes of operation are studied. A specific optimal strategy is determined for the conventional synchronizer for each 2db interval over the range. This synchronizer is compared with an adaptive synchronizer, using the SPRT technique, and optimized for a -2db SNR.

The SPRT synchronizer reaches Lock significantly faster for SNR<8db, and reverts to Search faster for SNR<2db. It adapts less readily to improving SNR in the "Return-to-Search" operation, but will still produce optimum results in this mode with fewer controls than a conventional design.

Introduction. The efficient processing of primary frame synchronization patterns, is key to making effective use of PCM telemetry in many applications. An ideal synchronizer should quickly acquire lock status on the appearance of correct patterns and return to Search mode just as rapidly if synchronization with the incoming data stream is lost. These decisions should also be made with few errors, In the limit a tradeoff between speed and decision error probability (DEP) is required when determining the strategy to be used. Applications such as nuclear effects and missile re-entry often provide short bursts of data in a high noise environment. In these cases optimization of the speed vs. DEP trade-off is necessary to acquire all possible data and maximize the benefits of the experiment.

Traditionally, synchronization equipment and techniques have not measured up to this task. Most available equipment is controlled by preprogrammed parameters entered either electronically by a computer or manually by a human operator. These parameters include the number of allowable bit errors in each of the three normal modes of operation: Search, Verify, and Lock; consecutive acceptable patterns in Verify; and consecutive unacceptable patterns in Lock. A mathematical basis for optimizing these parameters for a specific noise environment exists; however it is not commonly reduced to practice. Control settings for

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this type of equipment are determined empirically in practically all operational situations. Even if an initial analytic determination is made, rapid compensation for changes in the noise environment cannot be made as the experiment progresses.

In an effort to improve this performance considerable interest has been shown in frame synchronizing circuitry which can adapt to the immediate noise environment, and make correct decisions without operator or computer intervention.

The first published works[1,2] describing an adaptive synchronizer concentrated upon initial acquisition of synchronization in the Search mode. In these papers Hawkes and his associates describe a synchronizer which leaves the Search mode based upon a "best pattern in the frame" criteria. It then uses the number of errors in this pattern to determine the number of errors to be allowed in Verify and Lock modes. The number of frames inspected in each mode prior to decision is preprogrammed. The results described focus upon speed of operation rather than reliability, and are only presented for an error rate of 0.1.

In 1967 Van de Houten[3] proposed an adaptive synchronizer whose operation is based upon the Sequential Probability Ratio Test (SPRT) described by Wald.[4] He describes the operation of this synchronizer in the Verify mode through a computer simulation based upon bit sequential testing. Bit Error Rate (BER) environments of 1% and 8% are considered. The operation of the SPRT synchronizer was compared with that of a conventional unit.

The SPRT synchronizer adapted by itself to the actual noise environment in Verify mode and could be modified to optimize its performance for a maximum desired decision error probability. The only controls required are a preset number corresponding to the worst expected BER environment and a selectable decision error probability.

Van de Houten provides an excellent mathematical exposition in his work. As his work forms the basis of extensions to be addressed here, the reader should refer to it if he is not already familiar with it.

Extensions to Van de Houten's work subsequently appeared in an unpublished document.[5] This work described a pattern sequential implementation. It also provided a derivation of operation of the SPRT synchronizer in Lock mode. This work is presented below.

In this paper optimal parameters for a fixed strategy are determined. The operation of this strategy is then compared for speed and reliability with a pattern-sequential SPRT strategy designed for a worse case BER environment of 0.2.

Fixed Strategy. The optimal settings for a fixed strategy can be determined for a specific requirement by calculating the decision error probabilities, α and β , as a function of BER and the programmed parameters. α is the probability that an incorrect pattern is accepted as a correct one, while β is the probability that a correct sync pattern is rejected. These terms are calculated differently in the Verify and Lock modes yielding four probability functions: α_2, and β_2 in Verify mode
and a2 and a2 in the Lock mode.

Van de Houten derives α_1 and β_1. In the Lock mode α_2 and β_2 become:

$$\alpha_2 = 1-(1-[Po, \tau, .5)^{\chi} \quad (1)$$

$$\beta_2 = (1-[P1, \tau, \epsilon\ ])^{\chi} \quad (2)$$

where: χ is the required number of frames
τ is allowable pattern errors
ϵ is Bit Error Rate

and P1, $$\tau\ ,\ \epsilon = \sum_{i=o} \binom{\ell}{i} (1-\epsilon)^{\ell-i}\epsilon^{i} \quad (3)$$

Po $$\tau\ ,\ .5= \sum_{j=o}^{\tau} \binom{\ell}{i}[.5]^{\ell} \quad (4)$$

and
1 = pattern length

α and β have been calculated for both Verify and Lock modes and tables constructed. To construct these tables χ is varied from 1 to 5 and τ from 0 to 9. BERs corresponding to ideal performance at 2db intervals from -4db to +14db are used to calculate the values of β.

From these tables, synchronizer parameters can be selected based upon a desired strategy. The strategy selected is to have the more critical probability, α in Verify and β in Lock, having a maximum value of 10^{-4} if possible. Where two strategies would yield this result, the one yielding the lower τ and high χ was chosen. The strategies chosen are presented in Table 1.

The speed of operation of the conventional synchronizer is then determined. In the Verify mode, the probability of Lock by frame F is

$$PL(F) = 1 - (\beta_1)^{F-P+1} \quad (5)$$

In the Lock mode the probability of reverting to Search is

$$PS(F) = 1 - (\alpha_2)^{F-P+1} \quad (6)$$

In each case P is the programmed frame limit.

To determine operational speed equations (5) and (6) were solved for increasing values of (F-P+1) until P(F) $\geq$.99. The resulting values of F are plotted as circles in figures 1 and 2. It is interesting to compare these times with the programmed strategies and discover that the decision is made at the first opportunity 99% of the time at SNR of 2db and above.

The value of eight from shown at the -4db SNR (.25 BER) is for a P(L) of only 89%. As the test period is increased beyond this point P(L) actually decreases. This phenomenon was not observed for any other condition tested.

SPRT Strategy. Van de Houten's exposition of the SPRT strategy is modified and extended for comparison with the conventional strategy described above. Its parameters are adjusted for a worst-case bit error rate environment of 0.2, to fit the most demanding current applications. The equations are then modified to reflect a pattern-sequential, rather than bit sequential algorithm. Finally, the mathematical description of the process is extended to include the "Return-to-Search" operation in the Lock -mode.

Increased Error Environment. Two specific requirements studied for application of the SPRT technique have a BER environment of 0.2. Van de Houten hypothesized a worst-case environment of 0.08 BER; therefore the decision parameters K and L selected by him must be changed to fit the new environment. This can easily be accomplished, using equations 5 and 6 of his paper. In this case:

$L=19.6$ for $\alpha = \beta = 10^{-4}$

and $L=14.7$ for $\alpha = \beta = 10^{-3}$ from (5)

therefore if $\alpha = \beta = 10^{-P1}$

$P1=.2L$

From (6) $K=1.95 \simeq 2$.

The design of a synchronizer using these parameters increases the acquisition speed in the Verify mode, but reduces the "Return-to-Search" speed (improves retention of true patterns) in the Lock mode.

Pattern Sequential Testing. Making decisions on a pattern by pattern basis is more convenient in many applications. Van de Houten proposed a bit by bit computation as being somewhat faster; however the increased speed is not considered significant, as the decision can really have no effect until the pattern boundary is reached in any event. The pattern by pattern approach, on the other hand, is more consistent with present hardware implementations which use parallel pattern detectors to achieve initial acquisition in the Search mode, and must be employed in any case if a multiple bit window is used to compensate for occasional slippage in high noise environments.

Restating the criteria for the case of a parallel determination of errors in a number (P) of patterns of length (N), the following expressions result:

$$\Sigma\varepsilon \leq \frac{P\cdot N-L}{K_p+1} \qquad \text{Correct Synchronization} \tag{7}$$

$$\Sigma\varepsilon \leq \frac{P\cdot N+L}{K_p+1} \qquad \text{Incorrect Synchronization} \tag{8}$$

$$\frac{P\cdot N-L}{K_p+1} < \Sigma\varepsilon < \frac{P\cdot N+L}{K_p+1} \qquad \text{No decision} \tag{9}$$

Using these criteria results in the following expression for the probability of reaching the Lock mode by frame K.

$$P(L(K))=1-(1-P(L1))(1-P(L2))\ldots.(1-P(LK)) \tag{10}$$

$$\text{Where: } P(L(j))=\sum_{i=0}^{\frac{j\cdot N-L}{K_p}} \binom{j\cdot K}{i} \varepsilon^{i} (1-\varepsilon)^{j\cdot N-i} \quad 1\leq j\leq K \tag{11}$$

These equations were solved and compared with Van de Houten's data. The results, presented in table 2, show no significant difference exists. In addition to verification of this modification this result provides a firm basis for the extension to follow.

Operation in the Lock Mode. To provide a complete comparison of the two techniques, the operation of the SPRT synchronizer in the Lock mode must be described and its performance calculated. Hillestad in (5) provides this description, using an

argument analogous to that used to describe the fixed strategy. He states that the probability of reverting to Search frame K is given by:

$$P(S(K))=1-(P(S1))(P(S2)....(P(SK)) \tag{12}$$

where

$$P(Sj)=\sum_{i=0}^{\frac{j\cdot N+1}{K_p+1}} \binom{N.j}{i} (.5)^{j\cdot N} \quad \text{for } 1\leq j\leq K \tag{13}$$

Experimental Results. Computer simulations of the two synchronizer strategies were constructed to facilitate comparison of their operation over a wide range of parameters and error environments. These simulations are coded in APL and can be run interactively on a time sharing system. The beauty of the interactive approach is that answers are returned almost instantly and new parameter combinations can be tried quickly.

A 24 bit synchronization code was used in preparing the data for this paper as this length provided a point of comparison with Van de Housten's 24 bit results. This length is also the criteria used in two specific applications investigated. The resultant data are indicative of most cases since the majority of synchronization codes fall into the 20 bit to 30 bit range. The code length is a parameter which can be easily changed when rerunning the simulation for applications with codes of other lengths.

A SPRT synchronizer optimized for a worst-case BER of 0.2 as described above, was constructed. P1 was set to 4, to yield $\alpha=\beta=10^{-4}$. Ideal BERs were taken at 2db intervals from -4db to ±14db as before. The data are plotted in figures 1 and 2 as stars to facilitate comparison.

The results in the Verify mode bear out the prior work. In high noise environments from -4db to +6db the SPRT synchronizer is substantially faster. The speed improvement ranges from three frames at -4db to one frame at +6db. At +8db and above, both synchronizers require only the minimum of one frame to achieve Lock mode. The benefit of the MT synchronizer in this region is its freedom from controls and its ability to adapt to a changing noise environment automatically.

The advantages in the Lock mode are not so clear cut. In the noise range for which it is designed, -4db to 0db, the SPRT synchronizer is demonstrably faster. Its "return-to-Search" speed is a constant four frames in all noise environments, however, and in a low noise environment, an optimized conventional synchronizer returns to Search faster when presented with an incorrect pattern. This result is not surprising in view of the fact that equation (10) is not a function of bit error rate.

Conclusions. A conventional programmed synchronizer can be optimized to achieve Lock mode with a decision error probability $\leq 10^{-4}$ for bit error rates less than or equal to 0.25. When the signal-to-noise ratio is +8db or greater (BER $\leq 6x10^{-3}$) the conventional synchronizer acquires Lock on the first pattern in the Verify mode 99% of the time.

An SPRT synchronizer designed for a worst case BER environment of 0.2 reaches Lock significantly faster than the conventional,synchronizer for high noise environment, with a decision error probability of $\leq 10^{-4}$. For SNR.$\geq$+8db any speed advantage is not significant at this confidence level since a minimum of one pattern in Verify mode is required in any event.

The clear advantage of the SPRT synchronizer in "Go-to-Lock" operation is that once set for the worst noise environment expected, it always adapts itself to perform as well as, if not significantly better than conventional synchronizer as the environment improves. The conventional synchronizer must be adjusted for the exact noise environment to be encountered, or suboptimum performance results.

In "Return-to-Search" operation both types of synchronizers must be adjusted for the actual noise environment to be encountered if a decision to go to Search is desired as soon as possible. The SPRT synchronizer reverts faster for the same confidence level than a conventional unit when operated close to its design environment.

A control to adapt the SPRT synchronizer for several expected bit error rate ranges can be implemented easily. This control is useful when it is desired to revert to Search rapidly in a low noise environment. Three or four control positions should be sufficient to provide optimum performance in any environment. With this control added, the SPRT synchronizer is simpler to operate than a conventional synchronizer, while achieving equal or better performance.

Present day solid-state technology makes the implementation cost of an adaptive synchronizer using the SPRT competitive with that of a conventional synchronizer. The operational benefits of improved data with less operator attention make it attractive for use in all but the least critical applications.

References

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TABLE 1. SYNCHRONIZER SETTINGS FOR FIXED STRATEGY

SNR	BER IDEAL	VERIFY E	F	α	β 10⁻⁴	LOCK E	F	α	β 10⁻⁴
-4.	2.5E-1	8.	4.	3.3E-5	4.0E-1	9.	4.	1.5E-1	8.9E-6
-2.	2.1E-1	8.	4.	3.3E-5	1.8E-1	7.	4.	1.2E-1	1.6E-4
0.	1.7E-1	8.	4.	3.3E-5	5.2E-2	6.	4.	4.5E-2	9.7E-5
2.	1.0E-1	8.	4.	3.3E-5	1.3E-3	4.	4.	3.1E-3	5.2E-5
4.	6.0E-2	7.	3.	3.3E-5	1.5E-4	3.	4.	5.5E-4	7.7E-6
6.	2.0E-2	5.	2.	1.1E-5	1.3E-5	2.	3.	5.4E-5	1.7E-6
8.	6.0E-3	2.	1.	1.8E-5	4.0E-4	3.	1.	1.4E-4	1.3E-5
10.	8.0E-4	2.	1.	1.8E-5	1.0E-6	2.	1.	1.8E-5	1.0E-6
12.	1.0E-4	1.	1.	1.5E-6	2.8E-6	1.	1.	1.5E-6	2.8E-6
13.	1.0E-5	1.	1.	1.5E-6	2.8E-8	1.	1.	1.5E-6	2.8E-8
14.	1.0E-6	0.	1.	6.0E-8	2.4E-5	0.	1.	6.0E-8	2.4E-5

TABLE 2. COMPARISON OF RESULTS REPORT BY VAN DE HOUTEN WITH THOSE OBTAINED BY SIMULATION OF PATTERN SEQUENTIAL SPRT.

Conditions BER	pl	Frame	Bit Sequential (from Van de Houten)	Pattern Sequential
8%	3	1	90%	87.9%
		2	99.8%	99.9%
8%	4	1	71%	70.0%
		2	99%	99.6%
1%	3	1	99.99%	99.99%
4	1	99.8%	98.87.	

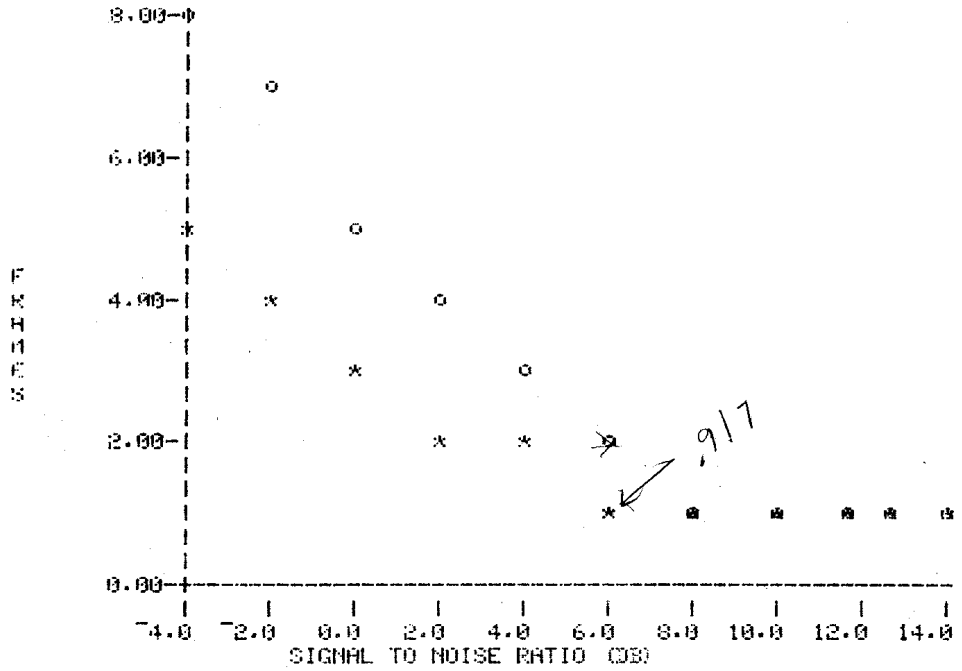

FIGURE 1. FRAMES TO ACQUIRE LOCK
o=FIXED, *=SPRT

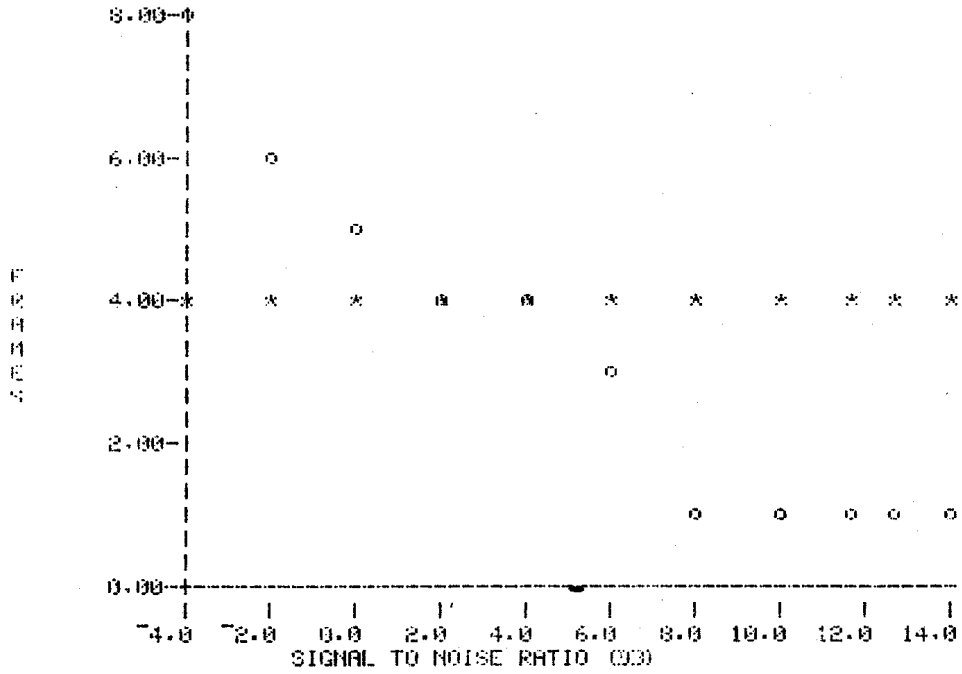

FIGURE 2. FRAMES TO RETURN TO SEARCH
o=FIXED, *=SPRT