A LOW LEVEL AMPLIFIER FOR PRECISION MULTIPLEXING

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Summary. An amplifier has been designed for high or low level multiplexing for aerospace PCM data acquisition systems. It was designed to provide "instrumentation amplifier" quality under conditions of high common mode, high or low rate random access operation and broad operating temperatures. It has shown versatility in operation, provides common mode rejection in excess of 125 db (RTI) and can be tailored for a drift temperature coefficient of less than 0.2 μV/°C (RTI) .

Introduction. Contemporary PCM systems cannot multiplex low level differential signals with high common mode content without degraded accuracy. This results from a lack of high quality instrumentation amplifiers suited for Pulse Amplitude Modulation (PAM) service. Where high accuracy is desired, see Figure 1, channel (or instrumentation) amplifiers are used. These reject common mode signals while signal conditioning the low level (millivolt) , low frequency, data sources into high level (e.g., 5 volt) single ended signals for multiplexing and digitization. Since satellite and booster users cannot tolerate the weight of channel amplifiers for each data point, a low level differential multiplexing scheme is desirable (see Figure 2). But this requires an especially designed PAM amplifier as standard instrumentation amplifiers are not suited for PAM operation.

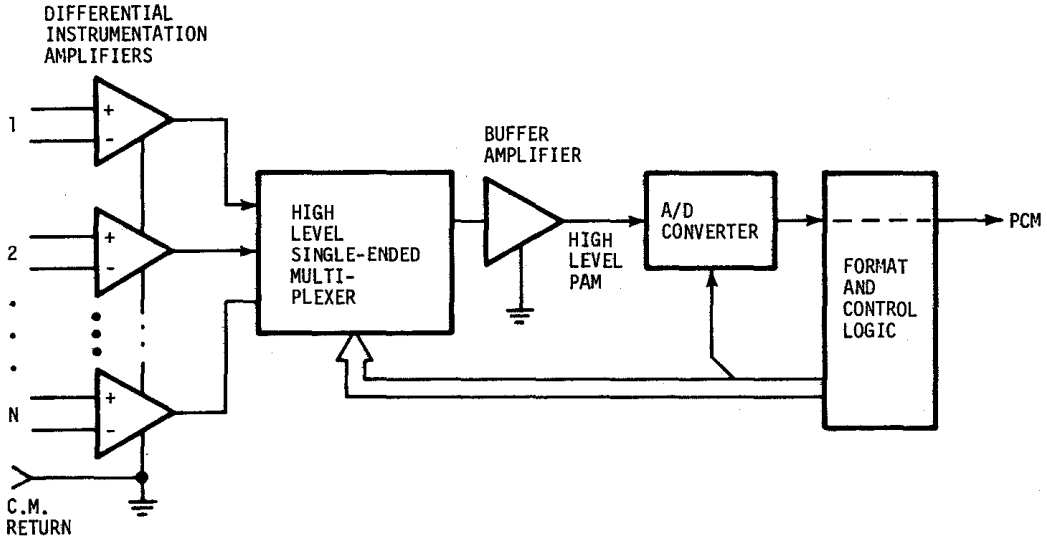

Figure 1. PC M Encoder with Channel Amplifier

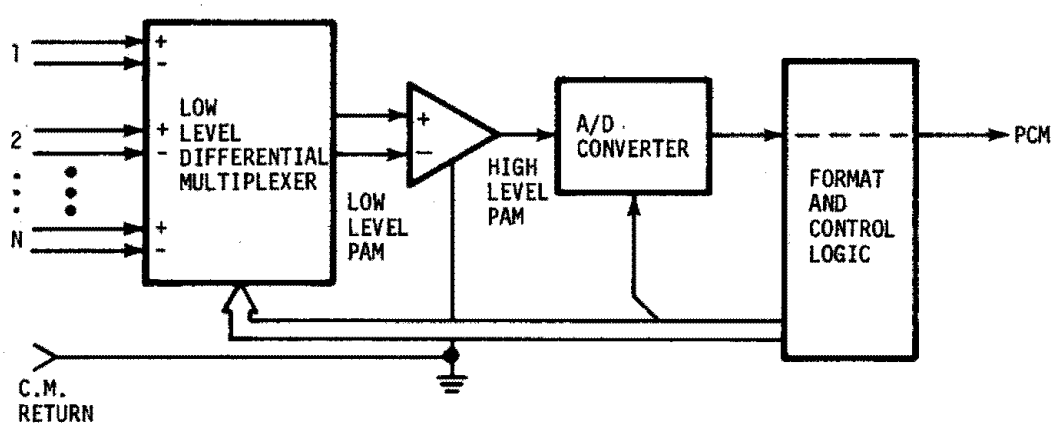

Figure 2. PCM Encoder With PAM Instrumentation Amplifier

A PAM amplifier must provide accurate signal conditioning under pulsed conditions. Since it amplifies PAM step functions, it must be broadband, whereas channel amplifiers operate at the lower data bandwidths. For example, a 1000 channel system multiplexing 10 hertz data at 5 samples per cycle dictates a PAM signal of 50,000 samples per second. This requires the amplifier to settle to a desired degree of accuracy within 20 microseconds. That is, the PAM Amplifier differential response bandwidth must be greater than 50 kHz, which is the PAM rate. Channel amplifiers used as in Figure 1 require only 10 Hz bandwidths. Pulsed operation also requires fast common mode rejection properties. A channel amplifier whose common mode rejection is specified at 60 (or 400) Hertz may be completely useless at a PAM rate of 50,000 channels per second. Figure 3 illustrates the effect of a DC Common Mode Voltage (CMV) input to channels 3 and 5 of a differential multiplexer. The amplifier “Sees” common mode rates at 50,000 channels per second. A slow common mode response yields an error which will be digitized. Therefore, the common mode response must also be less than 20 microseconds.

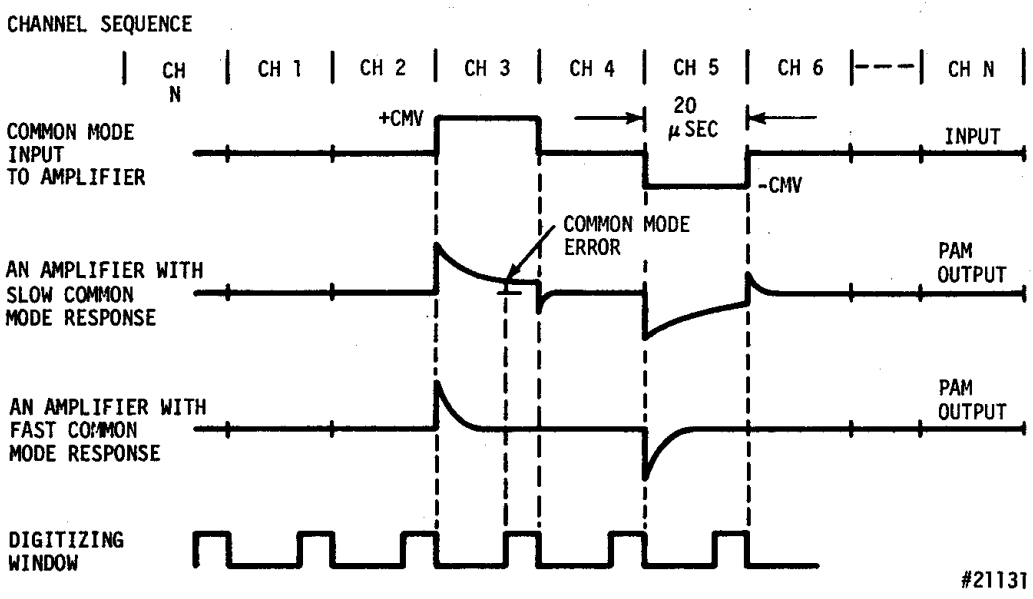

Figure 3. Pulse Common Mode Conditioner for PAM Amplifier

Since amplifier gains from unity to 1000 are common for instrumentation channels, an input offset (with temperature) of 1 millivolt (RTI) provides an error of 1 volt at the output. For a 5 volt full scale system, an error of 20% results - clearly unsatisfactory. Therefore, the input temperature drift must be below 10 microvolts for 0.2% error. For a temperature range of 25°C±50°C, the input drift must be better than ±0.2 microvolts per °C for gains of 1000, or ±1.6 microvolts per °C for gains of 125. To achieve this, the following stabilization techniques have been considered:

- Drift stabilization or compensation
- Calibration
- DC restoration or sampled feedback (analog correction)
- Digital correction
- Chopper stabilization

Drift stabilization is performed by designing compensating circuits at the input gain stage of the amplifier. Usually done with a well controlled transistor pair. To a system user, this is the most attractive solution because the amplifier can operate at a 100% duty cycle. Low level channels can be randomly selected and no channel sequence (programming) restrictions are necessitated.

Calibration is a special case for drift stabilized amplifiers. Its premise is drift stabilization, as previously discussed. If the drift error does not saturate the amplifier, but is outside desired error bounds, periodic calibration is feasible. To do this, calibration channels are assigned within the data acquisition system PCM format and data errors are removed by ground or airborne data processing.

DC restoration, as an example of analog correction, can effectively reduce offset drift but at a duty cycle penalty. One method uses a switching system which disconnects the multiplexer inputs to the amplifier, grounds the amplifier input terminals, and stores the DC drift error at the output. The error is phase inverted and reapplied during the next data sample thereby cancelling the amplifier offset. This technique suffers in that time must be allocated for disconnection, grounding and storing for each data channel. Hence, restrictions are placed on PCM programming since the amplifier is typically useful at only 50% duty cycles. (Very low speed systems can be more efficient since very fast amplifiers can be DC restored in less than 100 microseconds.) The complexity of this approach is the requirement for extensive timing and control circuitry. Another example of analog correction is sampled feedback. The amplifier offset is stored during a time where channel data is not sampled or transferred, e.g. , during digital or frame synchronization words. (Either the existence of naturally occurring “dead times”, or a restriction on duty cycle is a prerequisite for analog correction.) In either case, the offset is used as a correction factor during normal channel times.

Digital correction requires the PCM system design to monitor and correct out-of-bound offset errors. This can be performed by periodically digitizing the offset error (as in "dead times"), and correcting analog channels by a digital subtraction process. This is usually done with the analog-to-digital converter. But this technique required overly complex logic. Chopper stabilization (in the classical sense) is a well known technique but was not considered because of circuit complexity.

This report will describe the design technique for the development of a drift stabilized low (or high) level PAM amplifier which provides instrumentation quality accuracy under random pulsed operation.

Design Approach. The well established balanced bridge configuration shown in Figure 4A was selected as the nucleus of the amplifier. This configuration allows for separation of common mode rejection (CMR) and gain. The gain depends on "a" and "b" while CMR is adjusted by making $R_1/R_2=R_3/R_4$. Using available integrated circuit operational amplifiers, gain, and gain stability, were satisfactory. CMR, however, was measured at only 100 db. (Unless otherwise noted, CMR will be taken at a gain of 250 or 48 db.*) To improve CMR, see Fig. 4B, a common mode feedback loop was designed to drive the input amplifiers bias voltages with the common mode voltage. Rejection was measured at 130 db for a voltage swing of 20 volts peak-to-peak, about ground, demonstrating the value of "floating" the front end. However, care was exercised not to exceed the input range of the output amplifier (A3), which is limited by fixed power supply lines. The circuit configuration favors such use since the output amplifier, A3 (sometimes called a common mode stripper), has a differential gain of +1, hence a +10 volt common signal at A-B is divided to +5 volts at each of the amplifier input terminals.

When the amplifier of Figure 4B was tested with a varying rate PAM input, instead of a sinusoid, the CMR rolled off as expected, but a regenerative lock-up mode was observed. Lockup occurred when the input "square" wave had too high a slew rate, or contained spikes on the leading or trailing edge. This should be expected since the integrity of the common mode voltage (CMV) at junction C depends upon the transient response of

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*The CMR is customarily measured referred to the input (RTI), hence:

$$CMR(db) = 20 \log\left\{\frac{V_{in}(CM)}{V_{out}(CM)}\right\} + 20 \log\{Gain\}$$

When testing, $V_{in}(CM)$ is the common mode input causing $V_{out}(CM)$, the output error. Gain is the desired differential gain converting the full scale low level multiplexer input to the full scale high level analog-to-digital converter input.

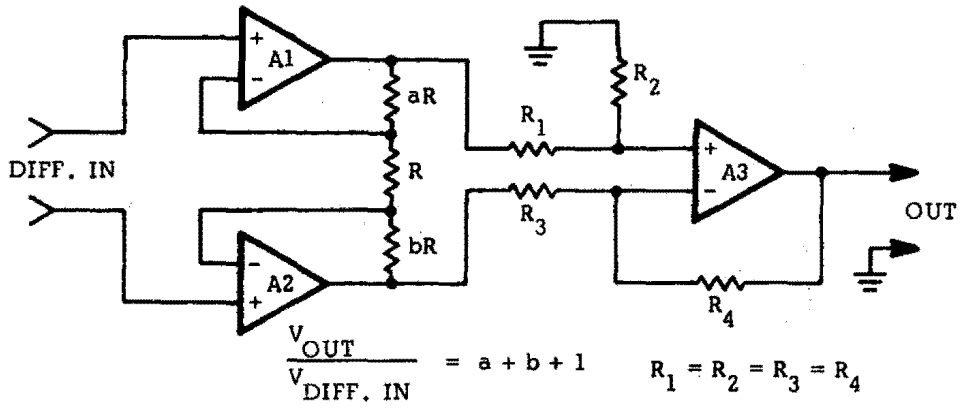

Figure 4A. Bridge Circuit

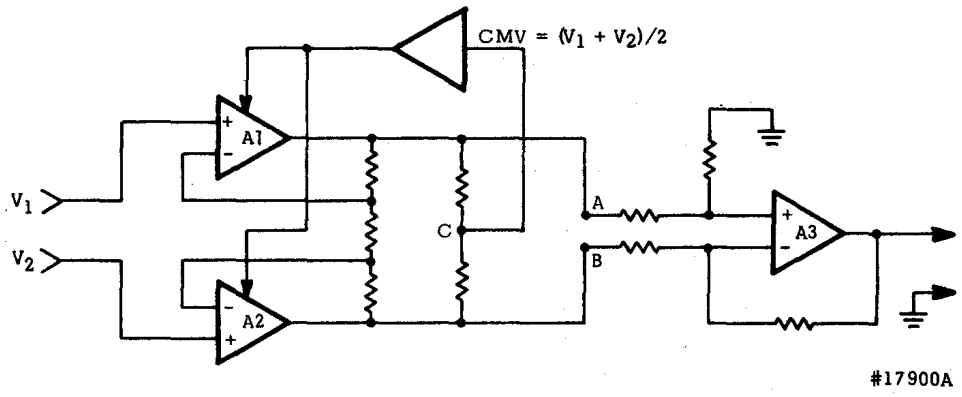

Figure 4B. Common Mode Feedback

amplifiers A1 and A2. Two effects occur: 1) the input stage of A1 and A2 saturate (and invert phase) before the correction signal is applied, or; 2) a transient coupled to the CMV driver drives the lines in the wrong direction. By examining Figure 4B, if the output of A1 goes to +15 volts and A2 to -15 volts, the CMV remains at zero and no correction is possible.

High speed common mode operation was obtained by converting to a feed-forward circuit shown in Figure 4C. This allowed operation with a 25 kHz square wave common mode input - which is equivalent to 50,000 channels per second.

With careful circuit tailoring, common mode rejection was measured as high as 140 db at a gain of 1000 (60 db). Typical performance was recorded around 130 db at a gain of 250 (48 db) for a CMV of +10 volts.

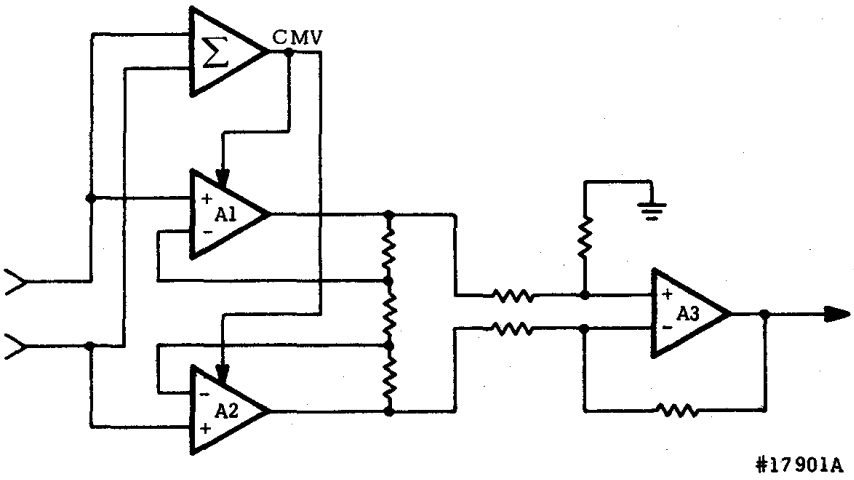

Figure 4C. Common Mode Feed Forward

Amplifier Design. The amplifier designed around the feedforward technique is shown in Figure 5. The Input Stage is a bridge circuit (Q1, A1, A2) which amplifies the differential input signal while maintaining a common mode gain of one. The Output Stage provides a differential to single ended conversion (at a gain of +1) while rejecting the common mode signal.

The input stage depicts the manner in which input resistance, temperature stability, and common mode performance can be designed to be mutually exclusive in the first order. First consider the manner in which the FET offset (of Q1) is temperature stabilized. Assume for the moment that the input common mode voltage is zero. A bias voltage, V_{DD} is applied to the drain resistors, R_D, at node A. A precision zener applies V_{DD}-V_Z to the non-inverting inputs of the operational amplifiers A1 and A2. The amplifiers operate, by virtue of their extremely high open loop gain, to feedback voltage until the difference between the inverting and non-inverting inputs of A1 or A2 approach zero. This sets the FET drains to V_{DD}-V_Z . Then the voltage across each R_D is V_{DD}-(V_{DD}-V_Z)=V_Z . This allows the use of a precision zener voltage to set the drain currents of Q1 . An adjustment potentiometer (T.C.) allows for balancing the drain currents of Q1A and Q1B for near zero temperature drifts. A typical amplifier at a gain from 1 to 1000 can be adjusted for offset drifts of less than ±0.2 µV/°C referred to the input. With care, temperature coefficients of less than ±0.1 µV/°C can be achieved. The limiting factor for low input stage gains is the temperature coefficient of A3.

When a common mode signal is applied, the FET common mode driver (Q2) algebraically adds the CMV to all terminals of the FET (Q1) front end. Hence, the drain currents are fixed by V_Z but the FET (Q1) terminal voltages (source, drain, and gate) float with CMV, providing excellent common mode rejection. Without common mode floating, it is difficult to obtain rejection better than 100 db, due to the low (and unbalanced) output resistance of FET stages.

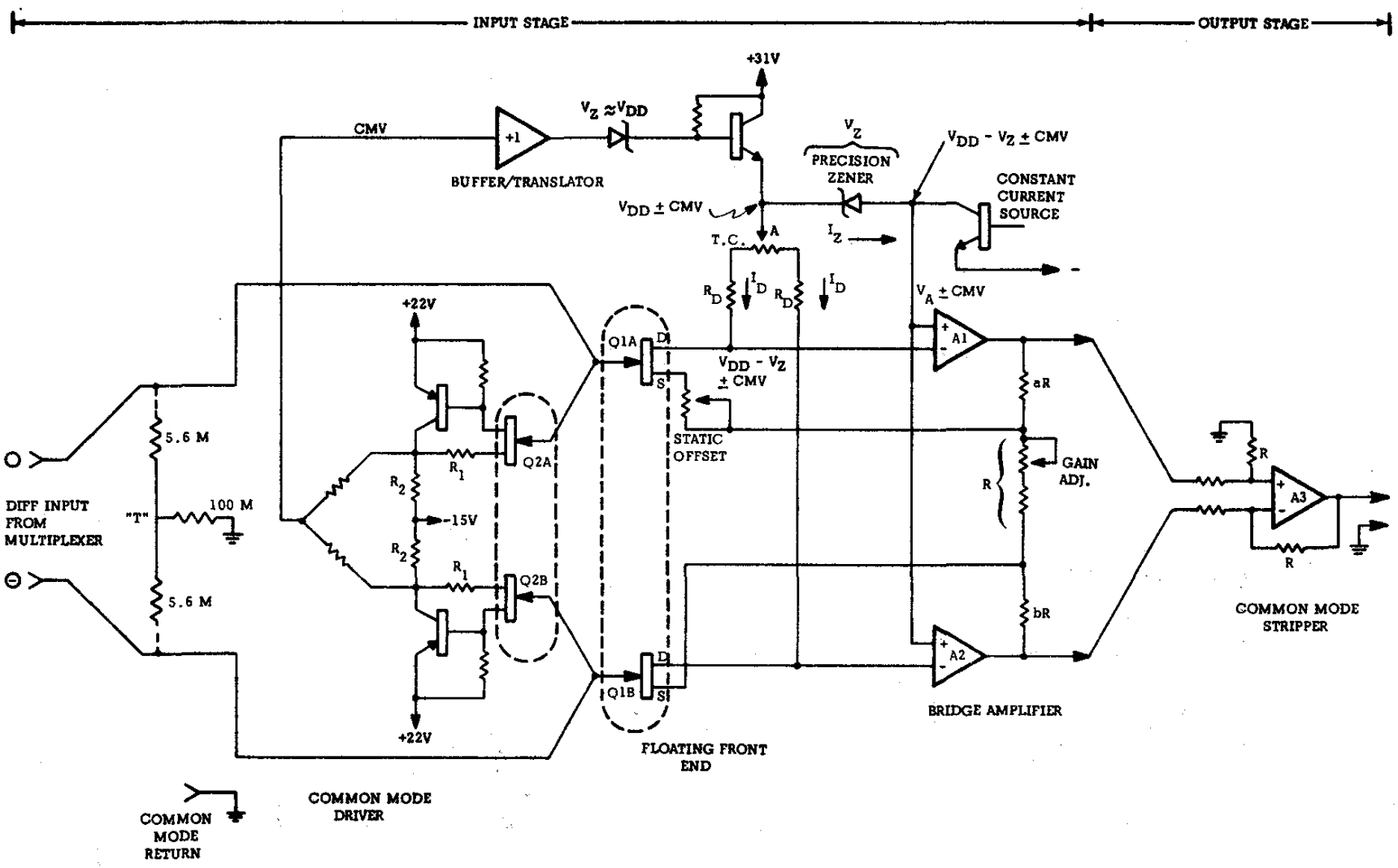

Figure 5. PAM Instrumentation Amplifier

The Output Stage (common mode stripper) is straightforward. If a gain of +1 is desired, each resistor has the same value and the differential signal is converted to a single-ended output. The intrinsic CMR of A3 must be high and care must be exercised to balance the resistors in the fashion $R_1/R_2=R_3/R_4$. Otherwise, overall CMR will rapidly degrade.

When using the amplifier, as in Figure 2, the data sources can be connected with or without a common mode return (signal ground) by reason of the following: Since the amplifier inputs are the gates of JFET's the input bias and offset currents are low. Therefore, if "floating" or two wire connections are desired, a "T" resistor connection can be added to the input so that the amplifier is referenced to ground. Since the JFET bias current is low, the "T" resistors can be very high, providing good CMR for high source resistance unbalances. Typical values are shown in Figure 5. But for best CMR, the "T" should be excluded and the common mode return utilized.

In order to obtain good gain stability and fast differential response, A1 and A2 must have high gain-bandwidth products, as to a lesser extent must A3. Gain stability is then limited by the feedback resistors which were ±1 ppm/°C Vishays. The output noise is a function of gain and bandwidth. At a gain of 125, the output noise is typically less than ±1.0 millivolt peak-to-peak measured from dc to 10 kHz. The primary contribution, short term instability and "flicker" (i/f noise), was measured on an Esterline Angus recorder. The broadband contribution was obtained by using a wave analyzer and an oscilloscope. In use, a single-pole low pass filter follows the output stage. Its bandwidth is restricted compatible with the required PAM rate, so that crosstalk is prevented.

Conclusions. The amplifier has been used in many airborne PCM systems and has allowed the reduction of hardware by the elimination of channel amplifiers for high accuracy systems. With careful design, its use has allowed for true 10 bit, 20 millivolt full scale, random access PCM encoders at bit rates beyond 128 kbps. At higher bit rates noise will increase since the output filter must be set for broader bandwidth unless the differential gain is lowered. However, if high gain and bandwidth must be used, digital filtering can be applied.

REFERENCES

1. Hilbiber, D. F., "Stable Differential Amplifier Designed Without Choppers", Electronics, January 25, 1965, pp 73-75.

2. Graeme, J. G., et alia, "Operational Amplifiers, Design and Applications", McGraw-Hill, 1971.