A High Data Rate Recorder/Reproducer

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Summary. — A High Data Rate Recorder (HDRR) has been developed under contract with Engins Matra, France, to be used in the European Spacelab. Engins Matra is responsible for the design and testing of the Command and Data Management System (CDMS). The HDRR is part of the CDMS which performs on-board data processing, multiplexing and storage. The Spacelab is a primary payload of the U. S. Space Shuttle Orbiter. The HDRR interfaces with the Spacelab High Rate Multiplexer, which, in turn, provides the inputs to the Tracking Data Relay Satellite (TDRS) down-link system for transmission to the ground.

The HDRR is capable of recording and reproducing at a maximum rate of 32 Mb/s. The total continuous record time allowed at this rate is 20 minutes. Thus a total of 3.84×10^{10} bits can be stored.

The HDRR has a versatile command and data interface that allows for recording at any rate between 1 Mb/s and 32 Mb/s. Reproduction can be performed at 2 Mb/s, 4 Mb/s, and any rate between 8 and 32 Mb/s.

Introduction. — As increased sensitivity and resolution are required from spaceborne sensors, the output data rates from these sensors become increasingly higher. When it is required that this data be stored before being sent to the ground station such as during the TDRS black-out region, a digital tape recorder capable of handling these high data rates is required. It is for this purpose that Odetics has developed the High Data Rate Recorder (HDRR).

Text. — The High Data Rate Recorder is a longitudinal type magnetic tape recorder/reproducer with a storage capacity of 3.84×10^{10} bits of digital data. This total capacity can be filled by using any one of a large number of combinations of data rates and record times; that is, at the highest data rate acceptable (32 Mb/s), the total allowable record time is 20 minutes ($32 \text{ X } 10^6$ Mb/s X 60 seconds X 20 minutes = $3.84 \text{ X } 10^{10}$ bits). At the lowest allowable input rate (1 Mb/s), the total allowable record time is 640 minutes (1 Mb/s X 60 seconds X 640 minutes = $3.84 \text{ X } 10^{10}$ bits). Since the input rate is continuously variable from 1 to 32 Mb/s, the total allowable record time can vary from

20 minutes minimum to 640 minutes maximum. A similar situation exists during reproduce except here the allowable reproduce rates are 2 Mb/s, 4 Mb/s and continuously variable between 8 and 32 Mb/s. Thus, the fastest reproduce (dump time) for a fully loaded recorder is 20 minutes.

Besides the high data rate capability, one feature that makes this recorder unique for the manned Spacelab application is the ability to change tapes during the flight mission. This capability allows the Spacelab crew to record a full reel of data; then, instead of needing a 20 minute reproduce time (if TDRS has a higher priority) they can choose instead to change tapes and begin a new record process.

At a more convenient time, the previously recorded tape can be placed back on the recorder and reproduced. The tape change itself is done semiautomatically. More details about the mechanics of the tape change will be given later.

The HDRR is physically packaged as two separate units. The first unit, termed the Transport Unit, houses the tape, its associated mechanisms and the electronics that are intimately related to the mechanisms. The second unit, termed the Electronics Unit, contains the remainder of the required electronics such as the 24 high-density encoders and decoders.

The interface with the HDRR is accomplished solely through the Electronics Unit. The command interface to the HDRR is as follows:

Power On

Power Off

Record - This command is enabled only when the clock is present and the proper record frequency has been selected. Recording continues until end of tape.

Reproduce - Same comment as Record.

Stop/Start-Stop and start times are the same—5 seconds.

Fast Forward - The maximum time from beginning of tape to end of tape is 7.5 minutes.

Fast Rewind - The maximum time from end of tape to beginning of tape is 7.5 minutes.

Input/Output Rate Select - This is a five-line command describing the required record or reproduce rate.

Self Test - This command starts the HDRR through its self-test sequence.

The digital monitors describe in which of the above modes the HDRR is operating. In addition, the following digital status signals can be monitored.

EOT - The HDRR is at the end of tape.

BOT - The HDRR is at the beginning of tape

Servo Sync - The HDRR is operating at the proper speed.

Tape Position Indication - This is an eight-bit monitor that gives the tape position with a resolution of 1/256 of tape length.

E.U. BITE - This signal goes true if the Electronics Unit fails self-test.

T.U. BITE - This signal goes true if the Transport Unit fails self-test.

Self-Test Underway

Local Control Busy - This signal is true when the HDRR is under local control (more about local control later).

Power Supply Status - A true state indicates all of the internal power supplies are within their normal tolerances.

The following analog monitors are also available:

Motor Current - This signal provides a measure of the capstan motor current.

Temperature - This measures the temperature near the magnetic heads.

Analog Trend - This signal provides a measure of head/ tape wear.

Power Supply - One monitor for each internal power supply voltage is provided.

Another input to the HDRR is the unregulated 28 VDC input power. If for some reason this power should be removed from the unit during an operating mode, the HDRR is equipped with a braking system which engages drums attached to the brushless D.C. motor.

One of the above listed commands is self-test. The self-test command can be used to verify the proper operation of the HDRR. If there is a malfunction, the self-test function will isolate the problem to either the Transport Unit or the Electronics Unit. The sequence of operation of self-test is as follows. When a self-test command is received, the self-test underway status line goes true, and all new commands are inhibited until the completion of selftest. The first operation of self-test is to perform a check of the Electronics Unit. In this test, a specific 2976-bit data word is generated by the self-test circuitry. This particular word is routed into the serial data input along with its clock—much as the normal data would be. This data is then serial-to-parallel converted and group encoded; but instead of being routed to the T.U., it is brought back to the reproduce side of the E.U. where it is group decoded and parallel-to-serial converted. The result is a 31-bit repeating data pattern that is checked for errors by the self-test circuitry. If the error check detects any errors, the E.U. BITE line is set true, indicating that the Electronics Unit is faulty. If there are no errors in the Electronics Unit test, the self-test proceeds to the Transport Unit. Here, essentially the same test is performed except that the data is routed onto the tape via a record command. A fast rewind command is then given and the data is reproduced. This reproduced data, when routed through the Electronics Unit, results in a 31-bit word that is checked for errors by the self-test circuitry. If an error rate greater than one in 10^6 bits is detected, the T.U. BITE line goes true. If the error rate is less than one in 10^6 bits, the Self-Test Underway line goes false, and the HDRR is ready to accept a new command.

The self-test can be initiated either from the Remote Acquisition Unit or from the Local Control Panel. The Local Control Panel is located on the Transport Unit; and in addition to the self-test initiation, the tape change is also accomplished using the Local Control Panel. When a tape change is required, the tape must be rewound to the end-of-tape sensors. The hinged cover on the Transport Unit is then opened, exposing the Local Control Panel and the tape pack. To initiate the tape change, the Local/Remote switch is turned to the Local position. This locks out all commands from the Remote Acquisition unit and gives control to the Local Control Panel. Next, the Unload switch is turned. This switch runs the tape from its stopped position to the actual end of tape. A very simple zipper-like mechanism allows the removal of the old tape and the attachment of the new tape to the leader. The Load switch is then energized. This switch runs the tape past the end-of-tape sensors. The Local/Remove switch is now turned to Remote, and the Transport Unit cover is closed. The HDRR can now be run to the beginning of tape and will be ready to start a new recording.

A list of some of the pertinent HDRR characteristics is given in Table I, and an HDRR functional block diagram is shown in Figure 1.

Table I
HDRR Characteristics

Size	Transport Unit: 19" X 19" X 19" Electronics Unit: 16" X 17" X 5"
Weight	95 lbs.
Data Rate	32 Mb/s maximum
Packing Density	20 Kb/inch per track
Total Storage	3.84 X 10^{10} bits
Tape Speed	Record/Repro 32 Mb/s: 88.6 ips Fast Forward/Fast Rewind: 254 ips
Tape Tracks	24 on an IRIG Standard 28 track interlaced head
Error Rate	Less than one in 10^6 bits with screened tape
Fast Forward/ Fast Rewind Time	7.5 minutes maximum
Command/Data Interface	Line Driver/Line Receiver
Input Data	NRZ-L and Clock

Electronic Functional Description. — From an electronic point of view, the HDRR may be considered to consist of four major elements: the data electronics, control and status electronics, tape motion control, and the power supply. The following functional description elaborates upon each of these elements.

Data Electronics

Line Receivers - Located in the Electronics Unit (E.U.) —Two line receivers are provided for the receipt of the serial data and clock inputs to the HDRR. The receivers are differential, low noise, wide bandwidth, high common mode rejection discrete circuits which provide an ECL output.

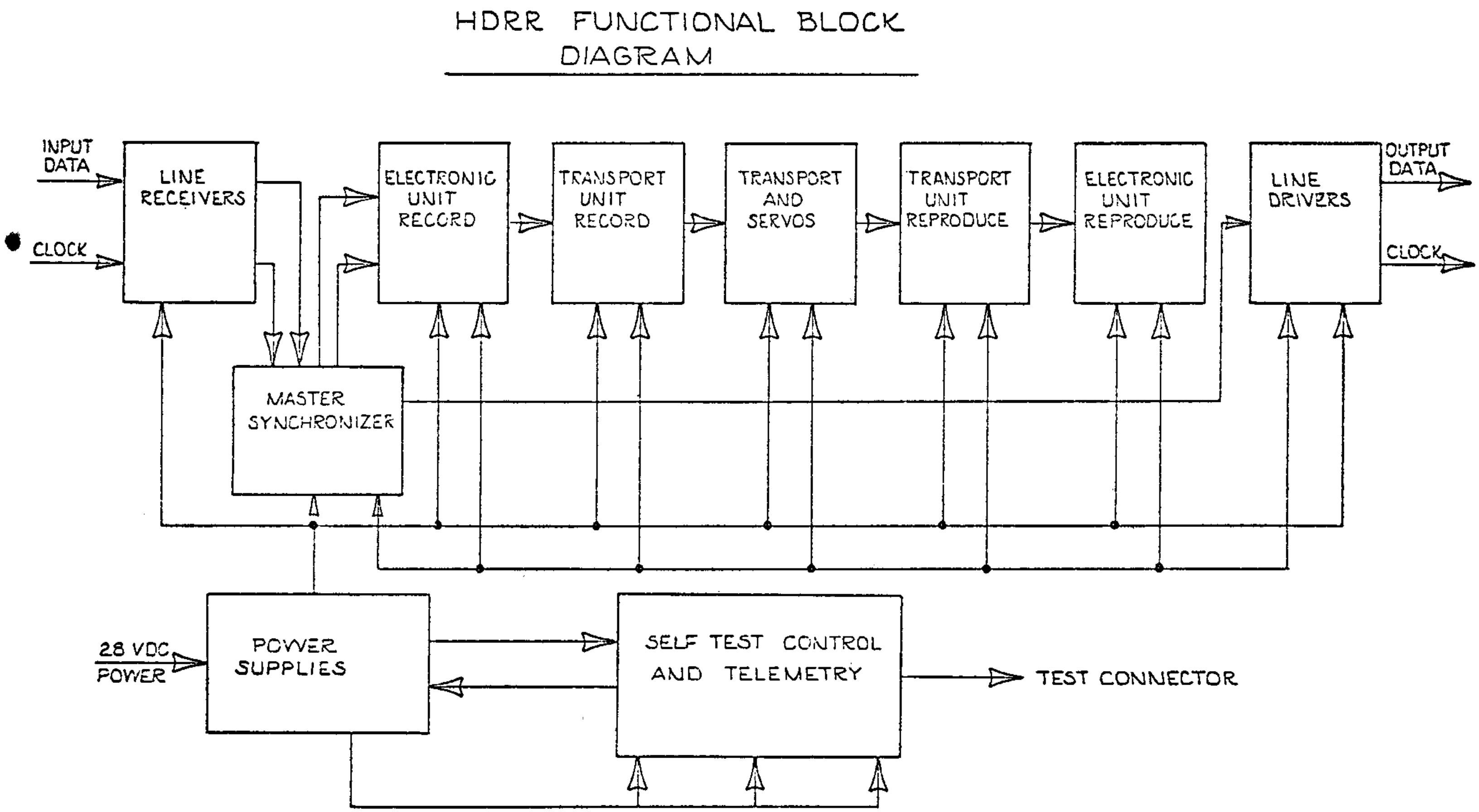
HDRR FUNCTIONAL BLOCK DIAGRAM
INPUT DATA
CLOCK
LINE RECEIVERS
ELECTRONIC UNIT RECORD
TRANSPORT UNIT RECORD
TRANSPORT AND SERVOS
TRANSPORT UNIT REPRODUCE
ELECTRONIC UNIT REPRODUCE
LINE DRIVERS
OUTPUT DATA
CLOCK
MASTER SYNCHRONIZER
28 VDC POWER
POWER SUPPLIES
SELF TEST CONTROL AND TELEMETRY
TEST CONNECTOR

Figure 1

Adjustable delay lines are provided for both the received data and clock. These delay lines allow for the compensation of differential delay between the two line receivers. A data selector for clock and data selects the incoming signals or the self-test signals, as appropriate, and drives a reclocking flip-flop.

Master Synchronizer (E.U.) - In the record mode, the Master Synchronizer performs two basic functions: the generation of timing signals needed in the record process and the initial demultiplexing of the serial data input to two parallel lines.

All necessary timing signals are derived from a phaselocked loop which is locked to the HDRR input clock. A 24-bit synchronization word is also generated on the Master Synchronizer. This sync word is ultimately used in the reproduction process to realign all data tracks prior to multiplexing the parallel data back to a single serial output.

E.U. Record Electronics (E.U.) — The E.U. record electronics consists of two identical assemblies: one for the 12 even numbered data tracks and the other for the 12 odd data tracks.

The serial data into each of the 12-channel record amplifiers is first demultiplexed to 12 parallel lines. Each resultant channel of data is then converted from the NRZ format to a group encoded format. This format converts each group of four incoming bits to a group of five bits. For each of the 16 possible states of the four input bits, there is a specific state of five encoded bits. The encoded five-bit output groups are chosen so that no more than two consecutive bits without a transition may exist.

The group encoded data is then loaded into a RAM buffer which serves the purpose of storing data while the sync word is inserted. The 24-bit sync word is inserted once for each group of 960 data bits on a per track basis. This sync word, along with the five-bit for four-bit group encoded data, account for an overhead of 28.125%. The data is then routed to the T.U. through a differential line driver selected to drive the 10 meter E.U./T.U. interconnect cable.

T.U. Record Electronics - Located in the Transport Unit (T.U.) — The T.U. record electronics consists simply of line receivers and push/pull saturation head drivers. The record head assembly contains the odd and even heads as well as head-current-normalizing resistors.

A resistor value is selected for each head so that the specific heads in the assembly will conduct optimum current for a fixed input voltage. This approach allows for the changing of heads in the field without the need for any adjustments.

The T.U. record electronics also includes the erase head which provides for full tape width erasure prior to recording.

Servos and self-test are discussed later; however, the head drivers associated with recording the servo feedback track and the self-test data-position-location markers are included on the record electronics. These drivers are push/pull saturation head drivers similar to the data head drivers.

T.U. Reproduce Electronics (T.U.) — The T.U. reproduce electronics includes the Reproduce Head/Preamp Assembly and two nearly identical 13-channel amplifiers. The head/preamp assembly is designed for field replacement without adjustment. Attenuator networks are adjusted in conjunction with a standard tape at Odetics prior to shipment to provide for this field level interchangeability.

The 13 channel amplifiers are identical with the exception of the 13th channel on each assembly. The odd track amplifier includes the servo feedback track preamplifier while the even track amplifier includes the self-test data-position-location marker preamplifier. The servo preamp is a current mode amplifier which requires no gain equalization for tape speed changes. The self-test position-mark-amplifier is a fixed gain voltage amplifier since only one tape speed is used in conjunction with self-test.

The remaining 12 channels on each assembly are identical and provide both phase and amplitude equalization as well as filtering and zero crossing detection. All equalization and filtering networks are programmable to accommodate the variety of reproduce data rates. A three-line to eight-line decoder is included for programming the proper equalization and filter settings.

The preamplifier data is first passed through an all-pass filter network. The all-pass network provides phase equalization for the lower frequency spectral content of the data. This network is programmed to one of four configurations: 2 Mb/s, 4 Mb/s, 8-16 Mb/s, or 16-32 Mb/s.

Following the all-pass network, the data is amplified by a programmable gain equalizing amplifier. A specific gain setting is available for each of the following eight data rates: 2 Mb/s, 4 Mb/s, 8-10 Mb/s, 10-12.5 Mb/s, 12.5-16 Mb/s, 16-20 Mb/s, 20-25 Mb/s, and 25-32 Mb/s.

Phase equalization to compensate for the differentiation of the head-to-tape interface is provided by a programmable differentiator.

After the differentiation equalization, the data is converted from an analog signal to a digital signal by a zero crossing detector. This digital signal is then routed to the E.U. through a differential line driver.

The analog data is tested for quality by the dropout detectors. Should the amplitude of the analog data fall by 26 dB below the nominal value, the dropout detector indicates a lack of data to the E.U.

E.U. Reproduce Electronics (E.U.) — The. E.U. reproduce electronics is comprised of six identical four-channel assemblies. These assemblies perform three basic functions: clock extraction, five-bit group to four-bit group decoding, and buffering to remove jitter and the sync word from the reproduced data.

Both data and dropout sense signals are received by differential line receivers at the E.U./T.U. interface. Data is routed to a selector which switches either the T.U. data or the E.U. record data, depending upon the operational mode. In the first step of a self-test sequence, the E.U. record data is selected; in all other reproduce functions, the T.U. data is selected.

Data is then routed to the clock assurance circuit where a clock assurance circuit operates in conjunction with the dropout detectors to insure that clock pulses are not derived from unusable data when a dropout occurs. During dropouts, the clock assurance circuit will continue to provide properly spaced clock pulses, avoiding a loss of synchronization even though data may be lost.

Using a clock extracted from the data, the data stream is constantly scanned to detect sync words. Sync word detection controls the operation of the dejitter/degapper buffers as discussed later.

The NRZ-L data is then decoded from five-bit groups to four-bit groups with a five-bit array. The data is then loaded into the buffer with the tape-derived clock. This clock will contain some jitter but the unload clock is derived from the spacecraft reproduce clock supplied to the HDRR. Through this process all data jitter is removed.

Master Synchronizer (E.U.) — In the reproduce mode, the Master Synchronizer phaselocked loop generates a clock frequency which is 20 times the reproduced data frequency. This 20-times clock is used by the clock assurance circuit in extracting the data clock from the data as well as for buffer unloading. The buffer unload clock, of course, is divided down to a 1 times rate.

The data unloaded from the 24 individual buffers is multiplexed to one serial line on the Master Synchronizer and routed to the line driver/receiver assembly for output from the HDRR.

Line Driver/Receiver (E.U.) — The serial data stream is reclocked with the output to minimize the delay between clock and data. Both clock and data are then routed through adjustable delay lines to further minimize the delay between the clock and data at the HDRR output.

Control and Status

The control logic interfaces with virtually all other assemblies to affect the orderly change of electrical conditions in response to a command from either of two interfaces.

Commands are received through optical isolators and must be greater than 500 μs in duration to be recognized. Received commands are memorized, and mode command memory is independent of octave command memory.

The memorized mode command is routed to the mode logic where appropriate control and status signals are generated for the power switching logic, BITE, telemetry, and T.U. controller.

The memorized octave command is routed to the Master Synchronizer to control the octave range of the phaselocked loop and is routed to telemetry. The T.U. Controller is the control focal point in the transport and receives commands from the control logic and the local control panel. Servo control commands from the E.U. control logic are intercepted by a selector allowing servo control to be modified in response to signals from the slew logic located within the T.U. controller.

The BOT/EOT circuitry consists of two modulated source drives, four sensors, and a band-pass filtered detector. Any of the four sensors may input to the single detector circuit as determined by mode and capstan direction.

The self-test position-mark-generator supplies mark data to the T.U. record assembly in response to a command from the BITE assembly.

The self-test position-mark reproduce data is amplified, signal conditioned and frequency discriminated to form self-test “position-mark-sense” for routing to the BITE assembly.

BITE Logic — The BITE Assembly operation is somewhat autonomous relative to the remaining assemblies in that it acts on only self-test start commands from the control logic or transport local control panel.

The BITE assembly consists of sequence logic generating commands to the control logic and other assemblies and monitoring to determine if self-test has been completed satisfactorily.

Associated with the BITE Assembly is the word generator/error counter on the line receiver/driver assembly. The word generator outputs the self-test record data word. The error detector is self synchronizing and compares reproduce data with the expected data.

The telemetry outputs of the BITE assembly are Self-Test Underway, E.U. BITE, and T.U. BITE. These signals are routed to the telemetry assembly and the transport local control panel. Self-Test Underway status is true for the duration of the test and will go false upon the satisfactory completion of all tests. E.U. BITE or T.U. BITE, as appropriate, will go true and remain true if an unsatisfactory condition is encountered.

Tape Motion Control

The longitudinal motion of tape during record, reproduce and high speed wind and rewind is controlled by three servo control systems. A capstan servo controls the velocity and instantaneous position of the tape while two reel servos (one for each of the two reels) control tape tension.

Capstan Servo — Fundamentally, the capstan servo may be characterized as a position servo, driving a brushless DC motor. Several loops may be considered in a description of the servo. The motor driver is, itself, a minor loop employing current feedback. The use of current feedback compensates for the motor back EMF voltage and enhances the wide speed range operation of the motor. A pulse-width modulator drives the commutation motor drive switches, minimizing power consumption. Current feedback is obtained from a small value resistor in series with the motor armature.

The motor driver loop is, in turn, driven from one of two major loops. When the motor is accelerating, decelerating or the HDRR is in a Rewind, Fast Forward, Load or Unload mode, a rate, or velocity, feedback loop is employed. When the commanded speed in Record or Reproduce is reached, the rate loop is opened, and servo operation is switched to position feedback.

In the rate feedback mode, the reference input is provided by a linear ramp generator. This input is summed with a feedback signal obtained from the motor optics. The feedback signal is frequency demodulated to provide a voltage proportional to motor speed for summing with the reference ramp, and the servo controls tape speed.

In the position feedback mode, the reference input is a clock signal provided by the master synchronizer. The frequency of the reference is proportional to desired speed. This reference is compared to a feedback signal derived from either the tachometer or the servo track. In either case, the comparison is one of phase or angular position, and the servo functions to control the instantaneous tape position, minimizing tape induced time-base-error.

The tachometer is used as feedback during record since no servo track is available on tape. When in the reproduce mode, the servo track recorded on tape during record is employed as the feedback signal.

Reel Servo (T.U.) — The Reel Servo functions to control the tension of the tape. An identical servo is associated with each reel.

The reference input to the servo is the torque applied to the compliance arm by the tension spring. Feedback is provided by the torque applied to the compliance arm by the tape. Thus, the arm serves as the summing junction and is coupled to a rotary variable differential transformer. This transducer converts the position of the arm, which is proportional to the difference of input and feedback torque to an error voltage.

The remainder of the servo is essentially the same as the capstan servo, including stability compensation and a current mode motor driver.

Power Supplies

E.U. Power Supply — The main power 28 V is applied directly to the E.U. power supply assembly where it is routed first through a circuit breaker and a power on/off relay. The 28 V at this point powers a small standby regulator which provides ±12 V for the control logic and telemetry circuits.

The 28 V is then routed through a current limiting circuit to the main E.U. switching regulator and to the T.U. Power Supply Assembly, which will be described later. This current limiting circuit consists of a series 100 Ω resistor shunted with a relay contact which closes only when the input filter capacitors of the E.U. and T.U. regulators are charged to within approximately 4 V of the main power input. The current limit circuitry and relay are powered from the standby regulator.

The main E.U. switching regulator is designed as a high efficiency DC to DC converter with feedback from its output. Its features are well regulated outputs, a controlled ramp start-up, output current limiting and overvoltage protection. It operates at a full load efficiency of approximately 90 percent.

This main E.U. regulator supplies power directly to the master synchronizer and through relays to the E.U. record and reproduce electronics. The appropriate voltage distribution relays are energized by the control logic. When the E.U. regulator is enabled, the output voltages come up slowly in accordance with a programmed ramp within the regulator, thus limiting surge currents through the relays and circuit capacitors to a safe value of less than 300 mA.

T.U. Power Supply — The T.U. power supply consists of two separate sets of preregulators and DC to DC converters. The first one supplies power to the entire reel servo system as well as the capstan motor. This regulator is enabled by +12 V from the E.U. standby supply whenever power is enabled in the E.U. The second T.U. regulator supplies power directly to the capstan servo electronics and T.U. controller and through relays to the T.U. record and reproduce electronics. This regulator and the appropriate voltage distribution relays are enabled by the E.U. control logic. To protect the relays from excessive current surges, the control logic first enables the appropriate relays, then enables the T.U. regulator, and, when powering down, disables the regulator before de-energizing the relays.

As in the E.U., the output voltages of the regulators are ramped up slowly to avoid excessive surge currents in the switching relays and in circuit bypass capacitors.

Also within the T.U. power supply assembly is a 10 KHz oscillator that supplies a 5 V RMS sinewave excitation voltage to the Rotary Variable Differential Transformer tension arm sensors and detectors.

Conclusion. — In summary, the HDRR is the first longitudinal recorder/reproducer developed for short manned space missions or long-life unmanned space missions. The relatively conservative choices of track count and per track digital packing density make it a prime candidate for future expansion. For example, data rates of up to 200 Mb/s and storage capacities of up to 1×10^{11} bits are achievable with only minimal changes to the HDRR design.