A Data Acquisition System Featuring On-Board Processing*

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Summary. — A data acquisition system for the telemetry data on the Technology Development Vehicle (TDV) program is presented. To meet the major experimental objectives of the TDV mission—the collection of high frequency vibration and acoustic data on a re-entry vehicle—required some unusual design approaches.

It is shown that collection of this data requires a great deal of data compression. This was accomplished using a technique of on-board data processing—actually performing the first step of data reduction in flight.

The entire data acquisition system is described in light of the requirements imposed by the data with emphasis on unusual problems and solutions.

Results of ground tests in an anechoic chamber are presented, and a brief discussion of the errors involved in onboard processing is given.

Introduction. — In 1974 Mr. Maschhoff, one of the present authors, presented a paper before this conference on a technique for on-board high frequency data processing.[1] In the ensuing years this technique has continued to be developed and implemented in actual flight hardware by Data Systems Division of Gulton Industries. The culmination of this effort is reflected in the SAMSO TDV program. The first flight of this Re-entry Vehicle (RV) program occurred on June 14, 1977 returning data from high frequency sensors of unparalleled quality And accuracy using a high frequency data processor as one component of Gulton's data acquisition system.

This report places the entire data acquisition system into perspective, highlighting important design decisions and techniques in the Wide Band Processor (WBP) as well as

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the rest of the system. Although the WBP is a key element of the TDV program, it must be considered in the context of the entire system.

<u>Data Acquisition Requirements</u>. — The basic problem in any telemetry system may be simply stated as how to most efficiently collect data from a wide variety of sources, convert each data source to a compatible medium and format the results for transmission on a RF link in such a way as to minimize the number of RF transmitters and the required bandwidth.

Modern experience has shown that most telemetry data is most efficiently handled in a sampled data system where each source—usually a low frequency voltage source—is converted to binary representation and encoded for PCM transmission. Often the amount of analog data to be so collected and digitized utilizes only a small portion of the available RF bandwidth. Thus the emphasis in recent years has been to extend the capabilities of PCM encoders such that they collect more and more different types of data sources, translating each source to binary words and merging all the words together into one output bit stream.

These non-analog sources include a variety of serial and parallel digital information, some of which are direct sampled and some which undergo elementary processing—for example, pulse frequency encoded data.

Other data sources of interest include wideband sources. Wideband data may be roughly defined as data whose bandwidth exceeds one or two kilohertz, thus requiring sample rates in the 5 to 10 KHz range—usually beyond the reasonable capabilities of a PCM encoder. It is the wideband processor whose design addresses this problem.

Another requirement often encountered on re-entry vehicle programs involves the recovery of data collected during reentry blackout. The plasma build-up along the surface of a re-entry vehicle during atmospheric re-entry acts as an RF shield preventing transmission (and reception) during what is often the most critical and dynamically interesting portion of the flight. Thus some means must be provided to retransmit the data occurring during this phase of the flight after recovery from blackout.

If an fm/fm telemetry link were used instead of PCM then this blackout data must be recorded on wideband analog tape recorders. This of course has many obvious disadvantages including weight, power, size, reliability and accuracy limitations.

A PCM system, on the other hand, transmits data in binary form from the PCM encoder. This data can be stored in digital solid-state memories with a savings in weight, power, size, reliability and accuracy, if the blackout period is short enough and the data rate low enough. This storage is done on the TDV program with a Digital Delay Unit (DDU) which is functionally a long shift register. The anticipated blackout duration on TDV is 8 seconds and the data rate is 172,800 bits/sec. requiring 1,382,400 bits of storage.

The TDV Data Set. — As mentioned, a modern PCM encoder must collect data from a wide variety of sources. These sources may be broadly characterized by two criteria: The electrical nature or form of the signal and the frequency content of the information. The electrical nature of the signal will determine the type of signal conversion mechanisms required: analog to digital, frequency to digital, parallel digital to serial digital, charge to voltage to digital, etc. The frequency content will determine the necessary sample rate to satisfy the well-known Nyquist sampling theorem. Other considerations such as dynamic range and desired accuracy will determine details of the system such as analog to digital quantization step size, number of bits in the binary representation of the sample, special processing, etc.

This particular system must collect high and low level voltage inputs, serial digital inputs, pulse frequency modulated inputs, wideband voltage inputs and wideband charge inputs. Each of these inputs must be sampled at a rate consistant with its bandwidth, processed to a form meaningful for the nature of the input and converted to a binary word consistent with the dynamic range and accuracy requirements. A summary of these requirements for TDV is given in Table 1.

System Overview. — Now we shall discuss the TDV data acquisition system in light of various inputs to be collected. First note that the sample rates given in Table 1 are determined by the nature of the input source and are specified to satisfy the sampling theorem. The first four signal groups give a total bit rate of 139,200 Hz. If the next four signal groups are sampled at 5 times their upper cutoff to avoid aliasing errors, then this direct sampling would require an incredible bandwidth of 86 MHz for digital transmission!

Clearly a better solution than direct sampling is required. The solution lies in the nature of the data itself. The data, in this case, are supplied by vibration and acoustic transducers and are a measure of the fluctuating external pressure environment of a re-entry vehicle. The analyst studying this data is not interested in the time domain reconstruction of the data but in the time history of the spectral content—that is he would like to know the power spectral density of the data and how that PSD changes with time.

Two basic items must thus be specified. The frequency resolution and the time-historic resolution. In this case, octave resolution in the frequency domain is found to be sufficient. The time-historic resolution needed depends on how rapidly the PSD changes with the time. There is some interest in shock-type events where the input data changes rapidly from a relatively low level to a high level. Thus the system must have a large

Type of Input	Number	Full Scale	Sample Rate/Bandwidth	Binary Representation	Number of Bits
High-Level Differential Voltage	68 85 4	0-5.1V 0-5.1V 0-5.1V	100 sps 20 sps 200 sps	20mV/bit	8
Low-Level Differential Voltage	55 10 48	0-5.1mv 0-5.1mv 0-14.5mv	20 sps 50 sps 50 sps	20µV/bit 56-86µV/bit	8 8
Serial Digital TTL	3	16 bits	200 sps	Direct	16
Pulse-Frequency Modulated TTL	3	0-150 KHz	200 sps	Proportional to Input Pulse Rate	16 8
High Frequency Charge	1 5 6 2	160 pC rms 16 pC rms 8 pC rms 4 pC rms	3.2-102.4 KHz (5)	Proportional to average power in 200 msec.	8
High Frequency Voltage	3 2 1	1 Vrms 0.355Vrms 0.122Vrms	3.2-102.4 KHz (5)	Proportional to average power in 200 msec.	8
Low Frequency Charge	14	16 pC rms	50-3200 Hz (5)	Proportional to average power in 200 msec.	16
Low Frequency Voltage	3 2 1	1 Vrms 0.2Vrms 0.063 Vrms	50-3200 Hz (5)	Proportional to average power in 200 msec.	16
Sync and ID	5	N/A	100 sps	N/A	8

TABLE 1 - INPUT CHARACTERISTICS

dynamic range (the goals were 40 dB for the high frequency and 60 dB for the low frequency wideband data) and a relatively short time window during which the spectrum is analized. This time window was set at 200 msec. (or 5 samples per second).

From the above considerations emerges the mechanism for collecting the wideband data. Each input source is filtered by bandpass filters into octave spaced bands then the outputs of each band are squared and integrated over a fixed interval of 200 msec., thus computing the in-band energy.

Since the nature of this processing is somewhat divorced from the regular data sampling function of the PCM encoder, a separate unit, the Wide Band Processor (WBP) is used. It interfaces to the PCM encoder as a serial input channel outputting the processed results in a fixed order upon demand from the PCM encoder.

Thus the data acquisition system is split into a PCM encoder handling predominantly direct sampled signals and the WBP handling processed signals. Another natural split in the system is the digital delay memory previously mentioned to deal with re-entry blackout. This unit, the Digital Delay Unit (DDU), is effectively an 8 second delay shift register, thus providing two digital bit streams to be transmitted on two RF downlinks—a real-time and delayed data stream. Both these data streams are continuously transmitted, so when blackout is over, real time data and data 8 seconds old—occurring before then during blackout—are both received by ground station equipment. This delayed data method of blackout recovery provides a redundant downlink helping overcome fading and noise problems on the RF link, alleviates the problem of not knowing exactly when re-entry blackout will occur, and provides a more reliable downlink when blackout is an intermittent phenomenon.

Another split in the system was found to be desirable in the WBP. Many of the inputs to the WBP are very sensitive charge inputs. It was found best to separate these inputs into a separate unit, the Signal Conditioning Unit (SCU), to prevent these sensitive analog inputs from picking up digital noise from the digital signals in the WBP. This also resulted in being able to make all inputs to the WBP identical, that is the SCU normalizes each signal to the same full scale level. This greatly simplifies testing of the WBP since each high frequency and each low frequency input is identical in bandwidth and full scale rms voltage level.

Thus we have four separate units, the SCU, WBP, PCM and DDU all playing in concert, operating as one functional Data Acquisition system. The complete system configuration is shown in Figure 1.

PCM Encoder. — The PCM Encoder is the central workhorse of the system. It digitizes and formats all direct sampled signals as well as selecting and formatting the processed signals from the WBP. The PCM Encoder used for the TDV Data Acquisition System is a modular, PROM programmable system composed of standard modules of Gulton's 7000 Series PCM Encoder. The central elements of the system are a series of PROM's which contain the address sequences for various inputs. These PROM's address various analog multiplexer inputs, digital register inputs, frequency to digital converters and external sources.

There are five high-level differential multiplexers for the high level analog inputs. Each multiplexer controls 32 inputs through a two level MOS Multiplexer. The output of the 32 point multiplexer is buffered by a unity gain amplifier and output to a common analog line via a third level analog switch. Each voltage input has a unique address given by the selection PROM's. The common analog line goes directly to the sample/hold circuit of the A/D converter.

The low-level multiplexers are identical in design and function to the high-level except the buffer is replaced by a precision, low-noise high gain amplifier. The 51mv signals go to an amplifier with a gain of 100, and the 14.5mv signals to an amplifier with a gain of 350, both resulting in 5.1 V full scale signals being presented to the A/D converter.

The A/D Converter is a successive approximation type operating at twice the sample rate, thus providing a 1/2 sample for settling the sample/hold circuitry and making the critical MSB decision.

Serial data is collected by 16 bit shift registers loaded from an external source by an independent (external) clock. When selected, the data is dumped to an output register and serially shifted directly to the output bit stream.

Pulse-Frequency modulated data is collected from counter circuits which count the input pulses. The counters are reset when the count is addressed and collected by the selection PROM's. An interesting design problem encountered here was to prevent loss of an input pulse occurring during readout. This was done with a latch on the input designed such that if an input pulse occurred during the counter readout and reset time, that pulse transition was saved until the end of the readout time. The occurrence of two pulses during the readout/reset time is prohibited by the maximum input frequency. This design is shown in Figure 2.

The output section of the PCM Encoder contains a parity generator (words are transmitted 8 bits at a time plus a vertical parity bit), sync code generators and ID counters for identifying the output format frame numbers.

The final serial digital data stream is then passed through a pre-modulation filter with a cutoff frequency of 0.8 times the bit rate before it is sent to the RF transmitter. A second pre-modulation filter is used by the output of the DDU for filtering the delayed data before transmission.

Digital Delay Unit. — Essentially the DDU is a 1,382,400 bit shift register. This number of bits is required to delay the 172.8 kbit/sec data stream from the PCM encoder a total of 8 seconds. In actual implementation the design is somewhat more complicated.

The shift register devices used on the DDU are silicon gate dynamic MOS 1024 bit devices (Signetics 2525). These devices were choosen as the best compromise for memory capacity, size, speed and power. To store 1,382,400 bits requires 1350 of these devices, so clearly power becomes a major factor. These devices consume 35 mwatts each at a clock rate of 172.4 KHz, the input data rate, for a total of 47.7 watts. This is unacceptably large. For this reason the memory array is divided into 27 parallel channels and the data is multiplexed into these 27 arrays as shown in Figure 1. This has two benefits: first, the duty cycle of the array is reduced by 1/27th to a shift rate of 6.39 KHz, resulting in a total power of 1.8 watts, second, a single point failure in the shift register chain will cause loss on only 1/27th of the data and that loss will not occur in the same word of the data frame by frame, i.e., any particular word in the output format would only be lost once every 27 frames. This is a very important consideration since regardless of the inherent reliability of the shift register, the loss of one stage of 1,382,400 shift stages could cause loss of all the data if all devices were connected in series rather than multiplexed.

Signal Conditioning Unit. — The SCU must convert each of the 40 wideband data inputs listed in Table 1 to a normalized voltage output for processing by the WBP. This simple-sounding task required some very unique design considerations.

To appreciate some of the problems one must understand something of the nature of the source signal. Some of the voltage inputs are derived from acoustic pressure transducers similar to strain gauges. During acceleration and deacceleration phases of the flight these exhibit a low frequency bias due to acceleration effects. This must be filtered on some inputs with a four pole high pass filter with a cutoff frequency of 40 Hz, so that this acceleration wave does not cause an excessive "dc" bias through the WBP gain ranger. A typical voltage amplifier is shown in Figure 3. Notice that an instrumentation amplifier is required to provide good common mode rejection, high input impedance and ground isolation for the transducer.

The charge inputs are derived from piezoelectric transducer elements. These must be converted to voltage inputs and amplified to normalize the full scale signals into the WBP. This is done with a charge converter and voltage amplifier as shown in Figure 4.

The charge converter is essentially an operational amplifier with a capacitance feedback. The amplifier output, V_o, is given by;

$$V_o = q_i/C_F$$

where q_i is the input charge and C_F the feedback capacitance. In practice a large value feedback resistance, R_F, is required to prevent DC saturation. This additional component provides a 6 dB/octave roll-off with a -3 dB frequency of $1/2\pi R_F C_F$.

The transfer function of the complete charge amplifier is then given by;

$$\frac{V_o}{q_i} = \frac{-K}{1+K} \cdot \frac{sR_F}{1 + sR_F\left(\frac{C_t}{1+K} + C_F\right)}$$

where, K = amplifier open loop gain
and, C_t = transducer and cable capacitance.

The term $C_t/1 + K$ is very small compared to C_F, so the denominator reduces to $1 + sR_FC_F$. This is the characteristic form of a simple first order roll-off as mentioned with $\omega = 1/R_FC_F$ and a terminal slope approaching 6 dB/octave. Also notice that since the transfer function is practically insensitive to variations in the input capacitance, it is insensitive to the cable length and capacitance of the transducer.

One of the more difficult design problems on the charge inputs is related to the mechanical nature of the transducers. These piezoelectric transducers, some hardmounted and some ported (that is mounted to holes in the vehicle skin) exhibit very strong (≈30 dB) resonances at about one octave above the frequency of interest. These resonances can cause saturation of the charge amplifier unless the gain is very low, which then causes noise problems. Thus a passive pre-filter is required before the change amplifier with a zero at the resonance frequency.

The design of this prefilter requires somewhat unusual considerations since the input and output are specified in terms of charge rather than voltage. A LC filter, as shown in Figure 3 is employed. Its transfer function is;

$$\frac{q_o}{q_i} = \frac{(1 + s^2LC_3)}{[(1 + sR(C_1 + C_2)] \; (1 + s^2LC_3) + s^2LC_1 + s^3C_1C_2RL} \cdot$$

By selecting a proper value of C_3 and L a -40 dB attenuation at the resonance frequency has been obtained. A typical measured prefilter response plot is shown in Figure 5.

Another unusual problem with charge amplifiers is vibration induced noise due to the input cable and electrostatic and electromagnetic interference from the power supply and adjacent PC boards.

The noise generation from the cable is mainly due to the “Triboelectric” effect associated with the relative motion between the cable dielectric and the outer shield around the dielectric. This effect necessitates using a special low noise cable.

The capacitance variation between the prefilter and the DC power line also generates a high noise level under vibration. This effect is further worsened by the electrostatic charge on the conformal coating of the PC board. Assuming vibrations of the PC board generates a 0.1 pF capacitance variation between the prefilter and +15 Vdc power on adjacent boards, the effective noise input becomes 1.5 pC. In the worst case this noise level becomes 37% of the full scale signal (4pC) - a S/N ratio of only 8.5 dB.

It was thus necessary to pay very careful attention to component layout and to encapsule the charge amplifier feedback resistor and capacitor and the prefilter in a conductive, grounded case.

Wide Band Processor. — The WBP takes each output of the SCU and divides it into several frequency bands with active bandpass filters. The lower frequency inputs (below 3200 Hz) are then commutated with an analog multiplexer and converted to digital form with a successive approximation ADC. The output of the ADC is squared then added to the sum of the previous squares obtained in that band. After 200 msec, the PCM encoder demands the result. The processed number is truncated to 16 MSB bits and transmitted to the PCM encoder. The sum is reset and new samples begin a new sum. This signal path is shown in functional form in Figure 6.

The higher frequency inputs (from 3.2 KHz to 102.4 KHz) are not converted directly to digital but are squared by an analog multiplexer and integrated with an analog integrator as shown in Figure 7. When the PCM encoder demands this data, it is converted to digital by the same ADC as the low frequency bands and the integrator is reset. The resulting 8 bit number is then transmitted to the PCM encoder.

Both types of processing result in numbers which are proportional to the energy in the respective bands:

$$\int_0^T f^2(t)\,dt \approx \sum_{k=1}^{N} f^2(k\Delta t)\,\Delta t,$$

where Δt is the ADC sampling interval, thus permitting calculation of the rms voltage in each band:

$$\sqrt{\frac{1}{T}\int_0^T f^2\,(t)dt} \approx \sqrt{\frac{1}{N\Delta t}\sum_{k=1}^{N} f^2\,(k\Delta t)\,\Delta t}$$

Note that this method of processing while resulting in a great deal of data rate reduction at the output does not relieve the necessity of proper sampling of the input data. The output of each bandpass filter must be sampled at above the Nyquist rate. To minimize aliasing errors, this sample rate is choosen to be 5 f_c where f_c is the cutoff frequency of the four-pole symmetric Chebychev bandpass filters used for octave splitting. For this reason the processor is divided into four identical processing sections, each with its own ADC and squaring/summing circuits, thus allowing a reasonable ADC rate of 1.783 MHz.

The bandpass filters operating on the input signals are arranged such that the -3 dB points of adjacent bands (the 1/2 power points) coincide so that the sum of the outputs of the bands is equal to the total power input. This arrangement is shown in Figure 8.

The output of each filter is scaled by a scaling buffer to maintain the dynamic range of the input signal in each band. This is necessary since each octave filter has a power spectral bandwidth less than the next highest filter by a ratio of 2. Thus if the time averaged spectral input is expected to be nominally flat, each successively lower filter must be scaled up by a gain factor of $\sqrt{2}$. Other anticipated nominal input spectra require other normalizing scaling constants if one wants to realize the best possible band-to-band dynamic range.

The outputs of the low frequency filters are digitized with an ADC developing a 7-bit plus sign representation of the bipolar 5.1 volt full scale signal where the binary representation is based on a step size of 40 mV per bit.

This number then becomes the address vector to a ROM whose output is programmed to values which are the square of the address vectors. This square is then stored in a shift register and serially summed with the previous sum of squares for that band. Serial arithmetic was used since the resulting sum may be up to 25 bits long and a parallel adder/memory combination was found to require far too many ICs.

The high frequency inputs require an analog multiplier and integrator for each band since they are too high in required sampling rate to be processed digitally with time-shared circuitry. In addition, the low frequency filters are designed using National Semiconductor LM124 quad operational amplifiers, each filter requiring only one of these devices. The high frequency inputs require four individual operational amplifiers since the LM124 does not have the required bandwidth. Thus each high frequency filter requires a considerable amount of space. Therefore to save space and power, the 20 high frequency inputs are divided into four groups of five inputs and time share the same set of filters, squarers and integrators. Thus each high frequency input is integrated for only 40 msec out of each 200 msec interval. The assumption here is that the duration of the phenomena in this region will be long compared to 200 msec. such that sampling in this manner is adequate to define the levels.

Each integrator on each high frequency band is periodically digitized by the ADC but only the last value obtained before the output is demanded by the PCM encoder is kept. This greatly simplifies the commutation of the various filters into one ADC.

The actual output collection task is initiated by receipt of a frame sync pulse from the PCM encoder. Any particular PCM frame contains all 6 bands of particular low frequency input, 5 bands of a high frequency input and a gain word. So when a frame sync pulse occurs a collection cycle is initiated to collect these 11 processed words plus the gain word, reset all 11 sums and integrators and update the input gain ranger.

The input gain ranger is an amplifier circuit with 5 gain settings: 1, 2, 4, 8 and 16. This applies gain to the original input signal before filtering. When the data for a particular channel is collected the processed word for each band is compared to two digital thresholds. If any word exceeds the upper threshold, the gain is reduced for the next integration interval. If all words are below the lower threshold, the gain is increased for the next interval. These gain decision points lie 12 dB apart but the output is proportional to the power in the bands so the 12 dB interval corresponds to the 6 dB gain steps at the input. This gain range method extends the dynamic range of the WBP by 24 dB. The resulting dynamic range of the system is 45.1 dB for the high frequency inputs and 71.2 dB for the low frequency inputs. The differences for the two methods of processing stem from the output word size possible with each method: 16 bits output for digitally processed bands and 8 bits output for analog processed bands.

Resulting Data Reduction. — The total wideband data requirements just outlined consist of 120 sixteen-bit words to be output every 200 msec and 20 eight-bit words to be output every 40 msec. The resulting bit rate is 13,600 bits/sec. If instead of on-board processing direct encoding with 8-bit accuracy were used, then the twenty 3200 Hz channels output continuously at a sample rate of 16 k sps and the twenty 102.4 KHz channels time shared in four groups and output continuously in four words at a sample rate of 512 KHz result in a bit rate of 18,944,000 bits/sec. The net bit rate reduction using onboard processing is 1393:1.

This reduction ratio is even more impressive if time sharing the high frequency channels is not done. In this case, if 16 bits on 120 low frequency bands are output every 200 msec and 8 bits on 100 high frequency are output every 200 msec, the resulting bit rate is still 13,600 bits/sec, but the direct sampled rate becomes 84 MHz. A net reduction of 6212:1.

On-Board Processing Errors. — It is interesting to note that the errors associated with digital processing are substantially less than those associated with analog processing of wideband data. This is mainly due to the virtual elimination of quantization and offset errors by the averaging nature of the digital processing.

The quantization errors may be modeled as an input noise source having a rectangular distribution with zero mean and variance of E2/12 where E is the quantization step voltage (40 mV). If a_i is the true value of sample i and $a_i + e_i$ is the actual value where e_i is the rectangular distributed error value, then the difference between the true value and error value over N sums of the squared samples is

$$\sum_{i=0}^{N} (a_i + e_i)^2 - \sum_{i=0}^{N} a_i^2 = 2 \sum_{i=0}^{N} a_i e_i + \sum_{i=0}^{N} e_i^2.$$

The expected value, then, is

$$E[2 \sum_{i=0}^{N} a_i e_i + \sum_{i=0}^{N} e_i^2] = 2 \sum_{i=0}^{N} E[a_i e_i] + \sum_{i=0}^{N} E[e_i^2].$$

Now, assuming a_i and e_i are uncorrelated, the the first term becomes $2 \Sigma_0^N E[a_i] E[e_i] = 0$ since $E[e_i] = 0$. The second term is merely N times the variance, N $E^2/12$. When the power is calculated a division by N is performed leaving an error of $E^2/12$. This is the mean value of the error. By the strong law of large numbers, the actual error approaches this value with probability 1 as the number of samples increase.

The offset errors behave in a similar fashion. If the input rms voltage is X, then $E[X] = \mu$ is the offset (or DC component). The true value has an expectation $E[(X-\mu)^2]$ σ^2.

The measured value is $E[X^2]$, but $\sigma^2 = E[X^2] - \mu$ so $E[X^2] = \sigma^2 + \mu^2$. The difference is then $E[(X-\mu)^2] - E[X^2] = \mu^2$. So only a second order term for the offset appears as an error in the output.

The actual processing errors are due to two sources: finite integration time, and aliasing type errors due to sample rate. An interesting derivation of these errors for a deterministic input is given as an appendix.

The total theoretical error, determined for worse case temperature variations, component tolerances and leakages was found to be 4% for analog processed bands (above 3.2 KHz) and 3% for digital processed bands (below 3.2 KHz). In actual laboratory tests under simulated environments the analog processed bands were better than 3% and the digital processed bands were better than 1% through the entire WBP.

Results of Ground Tests. — Flight data results are not yet available for publication, however extensive ground tests were performed by AVCO on the entire re-entry vehicle in an anechoic chamber.[2]

Since the TDV program will return data that for the most part had never been obtained before, it was necessary to develop a high degree of confidence in the validity of the data returned by the WBP. For this reason the outputs of each gain range amplifier in the WBP were made available at an external connector. Four of these were used to modulate constant bandwidth FM subcarrier oscillators in one particular ground test. The data from these FM links was analyzed by computer. On the following page is a table of this representative run.[3]

Octave Band (Hz)	WBP level minus Computer Analysis Level (dB)			
	Input 1	Input 2	Input 3	Input 4
50 - 100	+0.6	+2.0	+1.6	0
100 - 200	0	0	0	0
200 - 400	-0.1	+0.3	0	+0.5
400 - 800	-0.2	+1.1	+0.1	+0.6
800 - 1600	+0.2	+1.3	0	-1.6
1600 - 3200	-1.2	+0.2	+0.1	+1.0

The results are in very good agreement, well within the error bounds, especially considering the problem of trying to match the computer analysis band-pass response to that of the WBP.

Another type of testing performed was to hardwire additional transducers to the vehicle shell and compare their response to the response of the on-board system. An exact match is, of course, difficult to achieve. The transducer response are not identical. The location, and thus the stimulus is not identical. And the computer analysis of the hardwired sensors is not identical to the WBP analysis. However, excellent results were obtained, once again. Figure 9[4] is a representative plot of actual test results of a low frequency input showing the vibration amplitude derived from the WBP data for all six octaves processed and the vibration amplitude derived from the hardwired source. It is interesting to note that the WBP response was considered more accurate than the hardwired response, due to 120 Hz contamination of the hardwire signal.

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Appendix - Derivation of Processing Error Envelope

When a periodic wave form is sampled, the error envelope may be derived as follows.

Consider a sine wave of arbitrary frequency and phase: $V(t) = V \sin(2\pi ft + \phi)$. Let $k = tf_s$ be the sampling index for a sampling frequency f_s. The WBP performs the following calculation:

$$\overline{P} = \frac{1}{N}\sum_{k=1}^{N} V^2 \sin^2(2\pi kf/f_s + \phi) = \frac{V^2}{2N}\left[N - \sum_{k=1}^{N}\cos 2(2\pi kf/f_s + \phi)\right]$$

by trigonometric identities. Changing the range of the summation index, and letting $\theta = 2\phi$, $\beta = 2\pi f/f_s$,

$$\overline{P} = \frac{V^2}{2}\left[1 + \frac{\cos\theta}{N} - \frac{1}{N}\sum_{k=0}^{N}\cos(k2\beta + \theta)\right].$$

The last term converges*, giving

$$\overline{P} = \frac{V^2}{2}\left[1 + \frac{\cos\theta}{N} - \frac{1}{N}\cos(\theta + N\beta)\sin[(N+1)\beta]\frac{1}{\sin\beta}\right]$$

$$= \frac{V^2}{2}\left[1 - \frac{\cos(\theta + N\beta)\sin[(N+1)\beta] - \sin\beta\cos\theta}{N\sin\beta}\right]$$

* Summation of Series, L.B.W. Jolly, Dover, pp. 90-91, Series Number 480.

Using sin A cos B = 1/2 sin (A-B) + 1/2 sin (A+B),

$$\overline{P} = \frac{V^2}{2}\left[1 - \frac{1}{2N \sin \beta}\left\{\sin [(N+1)\beta - \theta - N\beta] + \sin [(N+1)\beta + \theta + N\beta] - \sin (\beta-\theta) - \sin (\beta+\theta)\right\}\right],$$

$$= \frac{V^2}{2}\left[1 - \frac{1}{2N \sin \beta}\left\{\sin [(2N+1)\beta + \theta] - \sin (\beta+\theta)\right\}\right].$$

Using sin A - sin B = 2 sin 1/2 (A-B) cos 1/2 (A+B),

$$\overline{P} = \frac{V^2}{2}\left[1 - \frac{1}{N \sin \beta} \sin \frac{1}{2} [(2N+1)\beta - \beta] \cdot \cos \frac{1}{2} [(2N+1)\beta + \beta + 2\theta]\right]$$

$$= \frac{V^2}{2}\left[1 - \frac{1}{N \sin \beta} \sin N\beta \cos [(N+1)\beta + \theta]\right].$$

Replacing β and θ,

$$\overline{P} = \frac{V^2}{2}\left[1 - \frac{\sin (N2\pi f/f_s) \cos [(N+1)\ 2\pi f/f_s + 2\phi]}{N \sin (2\pi f/f_s)}\right].$$

Now, define an error as

$$e = \frac{P_{actual} - \overline{P}}{P_{actual}} = \frac{V^2/2 - \overline{P}}{V^2/2} = 1 - \frac{\overline{P}}{V^2/2}$$

or, from (1),

$$e = \frac{\sin (N2\pi f/f_s) \cos [(N+1)\ 2\pi f/f_s + 2\phi]}{N \sin (2\pi f/f_s)}$$

Rearranging, and letting $N=f_sT$, where T is the total summation period,

$$e = \frac{\sin 2\pi fT}{2\pi fT} \quad \frac{2\pi f/f_s}{\sin (2\pi f/f_s)} \cos (2\pi fT + 2\pi f/f_s + 2\phi) . \qquad (2)$$

The error will be enveloped by the first two factors, while its actual value will be determined by ϕ in the last factor. Thus the error envelope is

$$E = \pm \frac{\sin 2\pi fT}{2\pi fT} \quad \frac{2\pi f/f_s}{\sin (2\pi f/f_s)} .$$

The first factor is due to the finite “integration” period, and the second is due to the sampling operation and is a measure of the aliased power.

A minimum sampling ratio of $f/f_s = 1/5$ is maintained throughout the WBP, giving a worse case value for the second factor of 1.32. The first factor has a worse case value in the lowest band, 50-100 Hz, at 51.25 Hz, but this band is sampled at 4 KHz, so $f/f_s = .0128$. With T = 200 msec, these values are

$$\frac{1}{2\pi(51.25)(.2)} \quad \frac{2\pi(.0128)}{\sin\,[2\pi(.0128)]} = (0.0155)(1.001) = 0.0155.$$

The worse case error is thus ±1.55% of reading. A typical mid-band error is ±0.2% of reading.

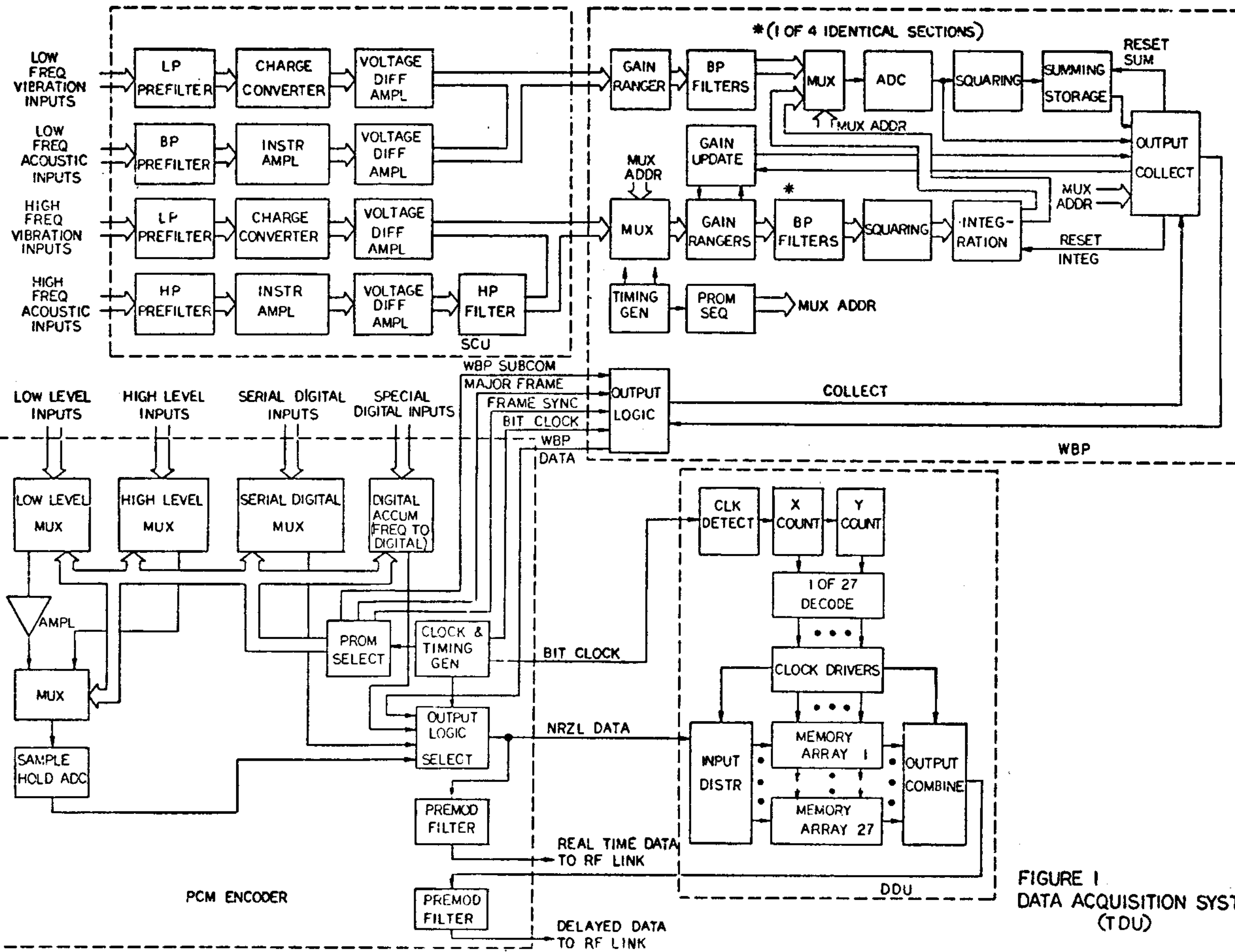

FIGURE 1
DATA ACQUISITION SYSTEM
(TDU)

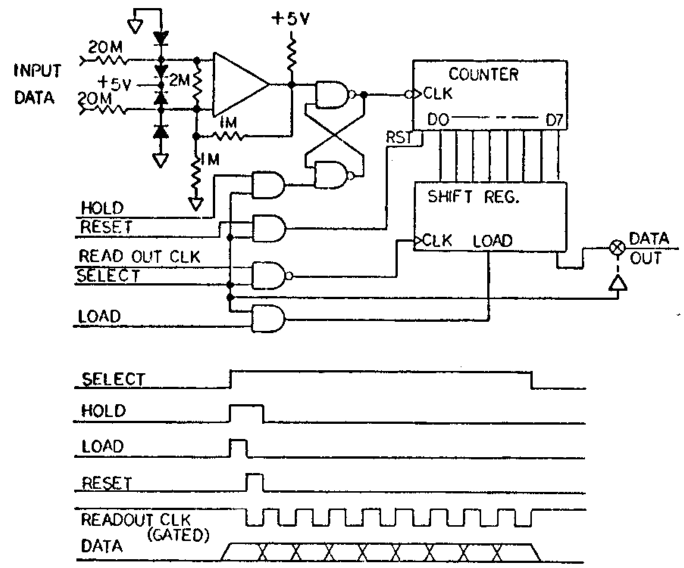

FIGURE 2 FREQUENCY TO DIGITAL CIRCUIT

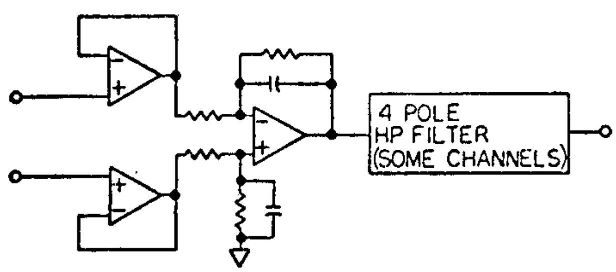

FIGURE 3 VOLTAGE AMP

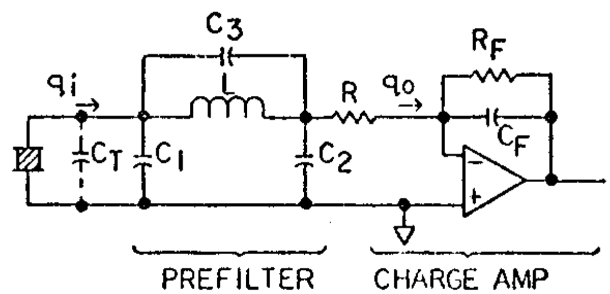

FIGURE 4 CHARGE AMP AND PREFILTER

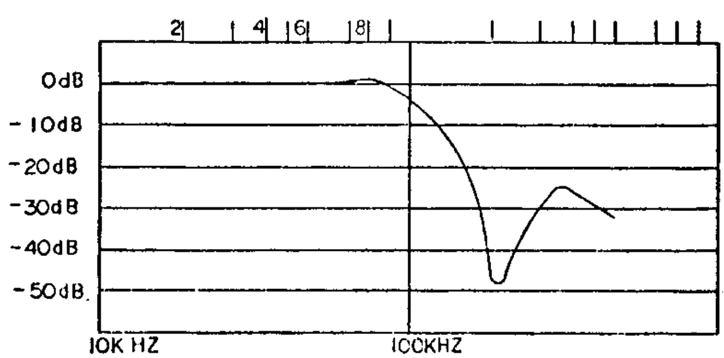

FIGURE 5
FREQUENCY PLOT OF THE PREFILTER

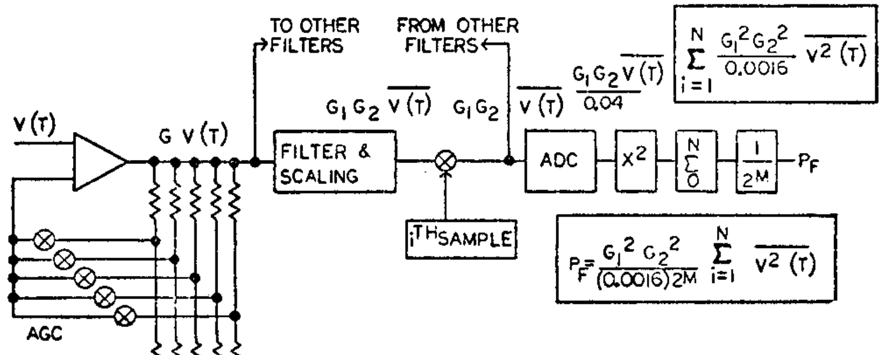

FIGURE 6
CHARACTERISTIC DIGITAL
PROCESSING PATH

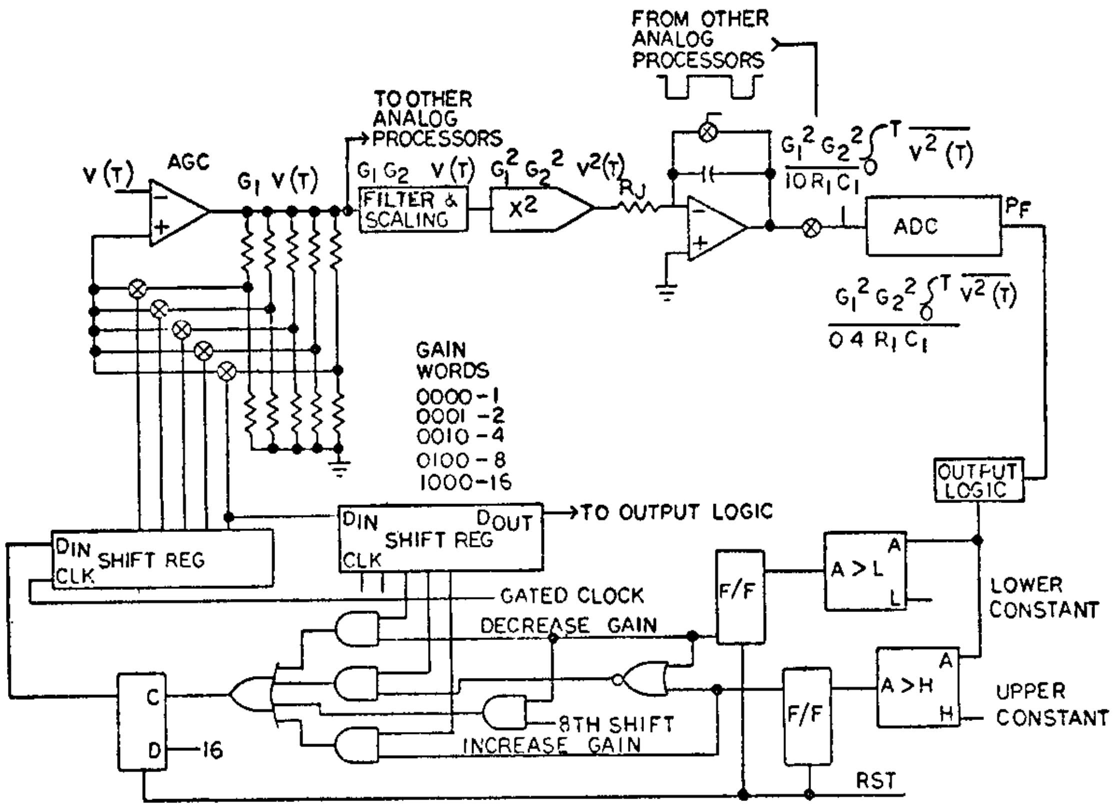

FIGURE 7 CHARACTERISTIC ANALOG PROCESSING PATH

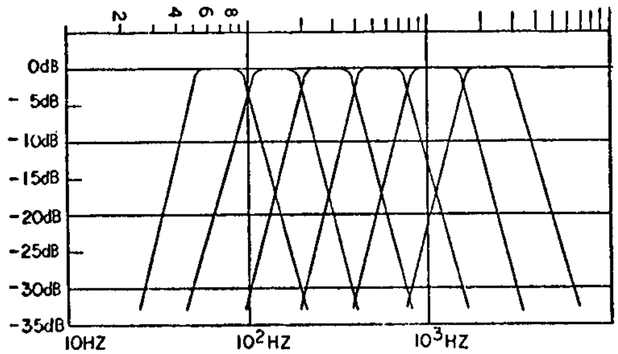

FIGURE 8 OCTAVE BANDS LOW FREQUENCY REGIME

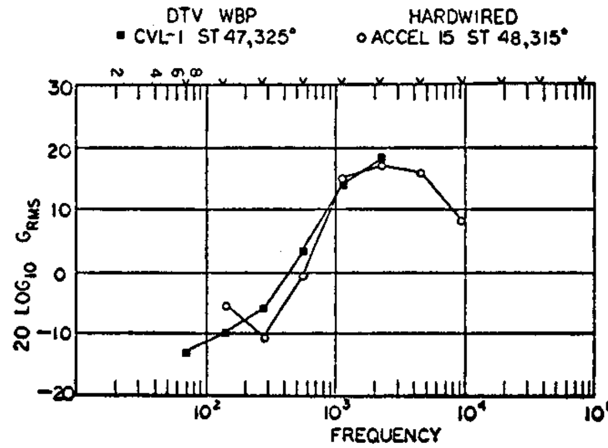

FIGURE 9
HARDWIRED VS WBP
GROUND TEXT RESULT