APPLICATION OF MICROPROCESSORS TO SPACECRAFT SYNTHETIC APERTURE RADAR PROCESSING*

Wayne E. Arens
Member of the Technical Staff
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California 91103

ABSTRACT

A ground-based digital synthetic aperture radar (SAR) processor capable of correlating images from raw spacecraft data at real-time rates is currently under development. The processor design requirements are particularly formidable due to (1) range migration effects resulting from planetary curvature and rotation, (2) antenna beam pointing errors, and (3) variation of the doppler reference function with changing orbital parameters. Based upon the current effort, this paper describes a candidate real-time on-board SAR processing implementation approach that might evolve for future spacecraft applications. Key features include the use of custom large scale integration (LSI) charge-coupled device (CCD) technology to accomplish the correlation functions and microprocessor technology to effect control.

INTRODUCTION

The Caltech Jet Propulsion Laboratory (JPL) is conducting a SAR processor advanced development program as part of an existing NASA Research and Technology Objective and Plan (RTOP). In turn, this RTOP is an approved and vital element of the NASA End-to-End Data System (NEEDS) program. The current RTOP is funded to design and build a real-time stand-alone Developmental SAR Processor (DSP) for operation in a laboratory environment. The DSP will have the capability to process SEASAT-A SAR data at real-time rates to produce four-look, 25-meter resolution radar images covering a 20 Km swath. The objective is to demonstrate this capability by the end of FY'80. Since the NEEDS program is emphasizing the development of a future on-board processing capability, it is important that the DSP architecture be designed to be amenable to implementation for on-

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board SAR processing applications. Future on-board applications must utilize advanced semiconductor technology to realize acceptable power, weight, and size characteristics. Current implementation proposals, evolving from the DSP program include the use of custom large-scale integration (LSI) charge-coupled device (CCD) filter chips for correlation and LSI microprocessor chips for control.[1,2,3,4,5]

SAR PROCESSOR DESCRIPTION

System

A functional block diagram for a candidate real-time on-board SAR processor implementation is defined in Figure 1. Referring to Figure 1, the data interface unit receives, conditions, and distributes incoming raw SAR video and parametric engineering data required to process SAR images. The range correlator performs the range correlation function. The azimuth correlator performs the azimuth correlation function, antenna beam pointing correction, digital magnituding, and multi-look superposition. The microprocessor controller computes the necessary corrections and effects control functions for all functional elements of the processor.

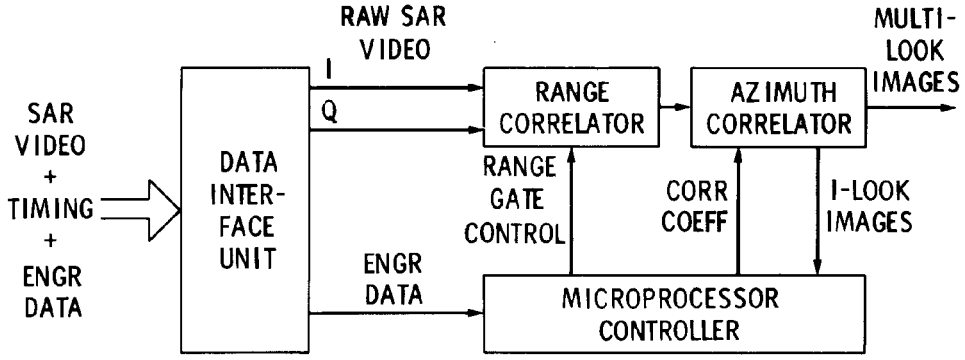

Figure 1 - Real-Time SAR Processor Block Diagram

Range Correlator

The range correlator of Figure 1 must provide complex correlation of the incoming real (I) and quadrature (Q) echo sample components with the original transmitted reference function. The range correlation function could be achieved in the time domain using four M-stage transversal filters as shown in Figure 2. The number of stages, M, is determined by the range time-bandwidth product and represents the number of echo samples required to accommodate the complete reference function signal.

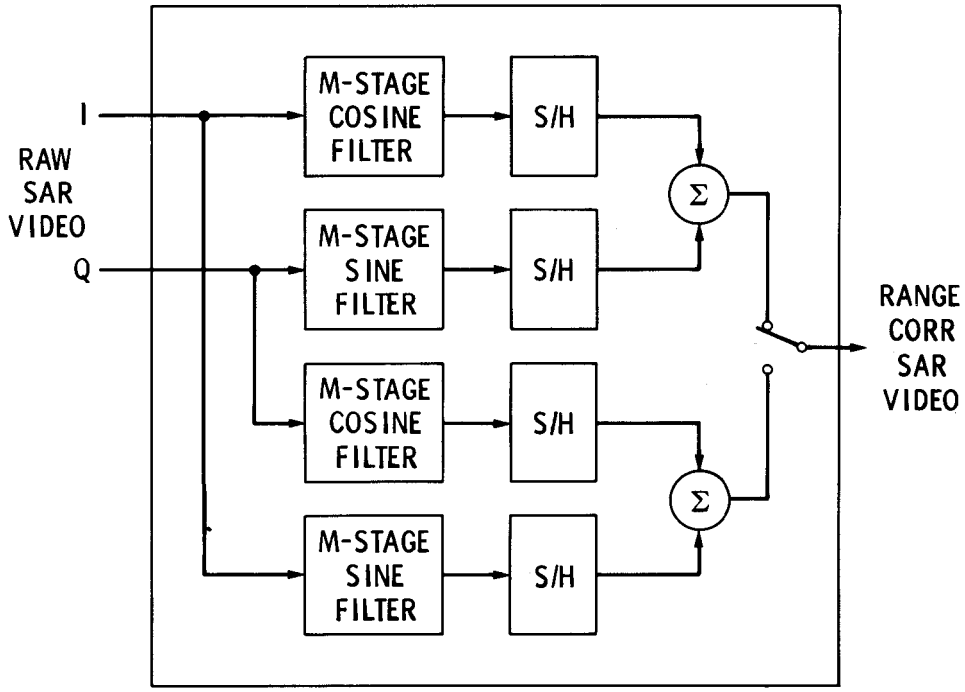

Figure 2 - Range Correlator Block Diagram

The range correlator transversal filters of Figure 2 may be implemented using current charge-coupled device (CCD) technology. Referring to Figure 3, a CCD transversal filter of length M provides M stages of storage while performing M signal-by-weighting coefficient multiplications each clock period. In Figure 3, each sample of the sampled radar reflection data is shifted through stages D_1 through D_M of the filter while the weighting functions h_1 through h_M conform to the originally transmitted reference function. Once the register is filled, for each radar data sample shifted into the register, a complete correlation of all M points in the register with the reference function is automatically accomplished and a correlated output produced. The correlation function is therefore achieved by nothing more than shifting the radar return data through the shift register.

Currently, 800-stage integrated circuit (IC) CCD transversal chips have been developed and successfully demonstrated. The powerful computational capability offered by this technology provides a potentially attractive approach for future real-time on-board SAR range correlation applications.

Azimuth Correlator

A potentially attractive implementation architecture for achieving the azimuth correlation function in real time is defined in Figure 4. The functions required to produce a complete image line are accomplished by each of N parallel CCD azimuth filter chips. Since N pulses must be coherently integrated to produce an image line, the output rate, if only one

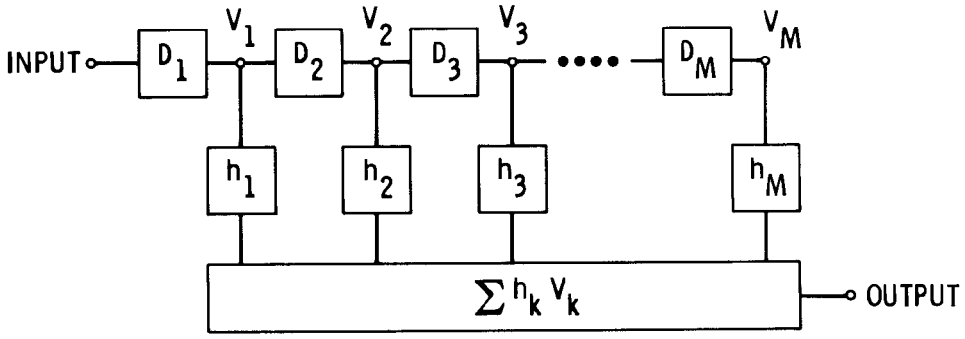

Figure 3 - CCD Transversal Filter

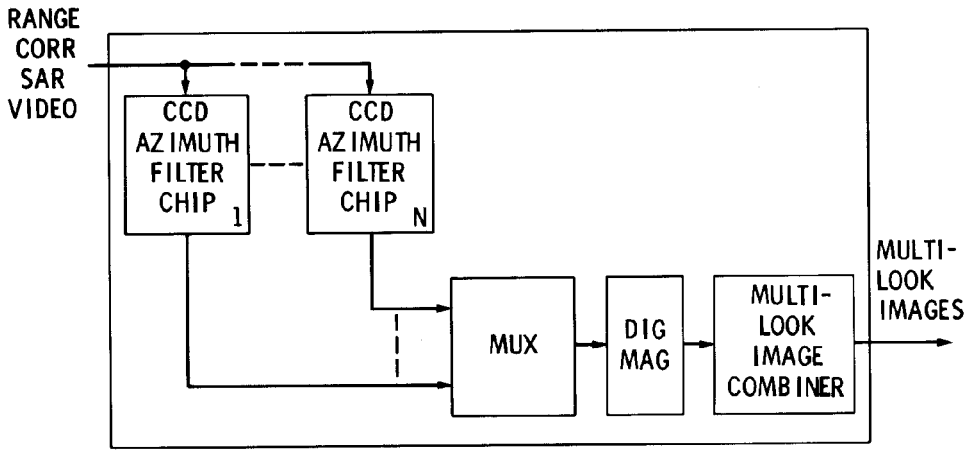

Figure 4 - Azimuth Correlator Block Diagram.

azimuth filter chip were used, would be 1/N of real time. By employing N chips in a parallel processing mode, a real-time throughput rate may be achieved.

A functional description of the CCD azimuth filter chip is provided in Figure 5. Referring to Figure 5, each such chip independently achieves (1) range migration correction by placing each incoming sample in the proper range bin, (2) multiplication with the proper filter weighting function, and (3) accumulation of filtered range line information over the desired portion of the azimuth beam. As noted from Figure 5, the range migration correction is effected by selectively gating the desired range line samples to a complex multiplier. The complex multiplier is used to weight the corrected range line samples with the desired azimuth chirp reference function. The doppler reference coefficients can be updated as necessary from the microprocessor controller of Figure 1. Following complex multiplication, the I and Q samples for each such range line are temporarily stored in an accumulator register. Following N such accumulations on a given chip, corresponding to the transfer of N range lines, an accumulator register will contain the I and Q samples of correlated image data for an entire line. At this point, the I and Q image data is read out for digital magnituding purposes to form pixels. By multiplexing between chips on a line-by-line basis, a continuous real-time data flow is achieved.

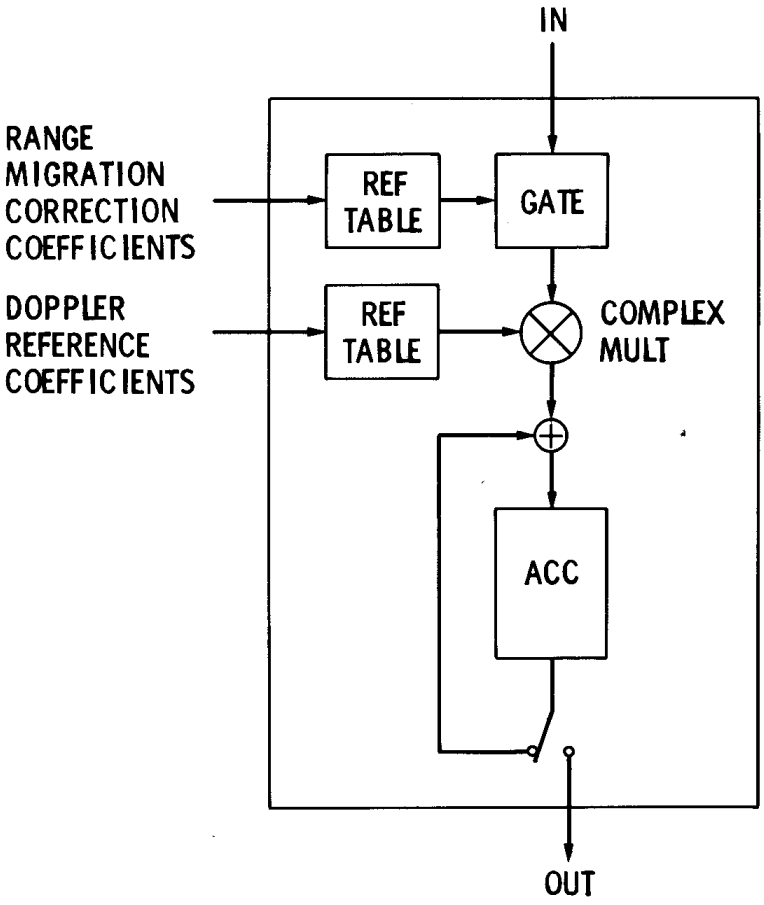

Figure 5 - Azimuth Filter Chip.

Currently, a customized LSI azimuth filter chip, as described in Figure 5, is under development as part of the JPL DSP task. This chip will be capable of operating at 3.5 MHz clock rates and will provide a capability of accumulating 1024 range lines.

MICROPROCESSOR CONTROL FUNCTIONS

The function of the microprocessor controller of Figure 1 is to provide the basic timing, control, and correction signals functionally required by the SAR correlator blocks. This includes the computation and generation of correction signals for azimuth correlation reference function variations, range migration effects, and antenna beam pointing errors.

Azimuth Reference Function Generation

For spacecraft applications, the azimuth correlation function is affected by numerous orbital parameters. Therefore, the reference function required for processing in azimuth will change due to orbital variations and must be updated accordingly.

In order to compute the correct azimuth correlation function for image processing purposes, specific information as shown in Figure 6 must be available to a given accuracy. Assuming this information is available to the microprocessor controller, Figure 6 defines the major computational steps that must be implemented to provide updated azimuth reference functions for the azimuth correlator. The computational blocks of Figure 6 could be implemented using microprocessors.

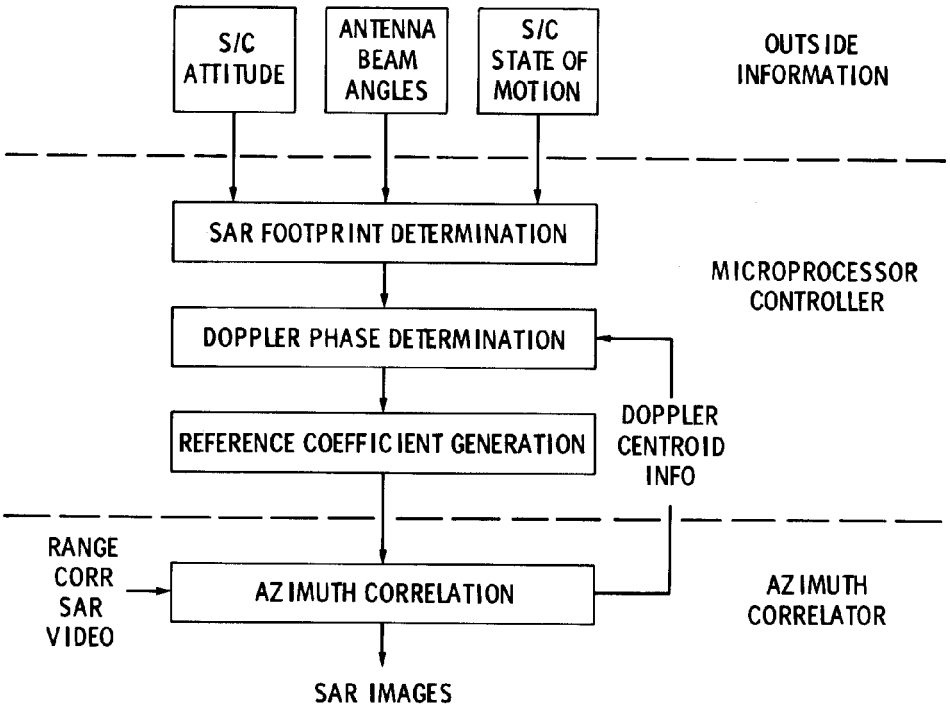

Figure 6 - Azimuth Reference Function Generation

Beam Center Range and Doppler Offset Determination

Due to planetary curvature and rotation, a given sample may not remain in the same range bin during the full azimuth integration time. This effect is referred to as range migration. Unless corrected, the azimuth resolution will be degraded. Range migration correction is achieved in two ways. The linear term (range walk), which is predominant, is accommodated by controlling the beginning of the sampling window on a pulse-by-pulse basis. The quadratic term (range curvature) must be compensated for by selecting the samples that are gated into the multipliers of the azimuth filters of Figure 4. Also, modification of the doppler reference function may be necessary to compensate for antenna beam pointing errors where physical pointing accuracy of the antenna is not adequate.

The specific computations required to determine the beam center range and doppler offset are defined in Figure 7. Two control functions are provided. One is routed to the range and

azimuth correlators of Figure 1 to control the range gating circuitry so that a constant range is maintained. The second control signal is provided to electronically move the beam, by means of azimuth correlation function selection, to compensate for doppler frequency errors due to an antenna beam pointing offset.

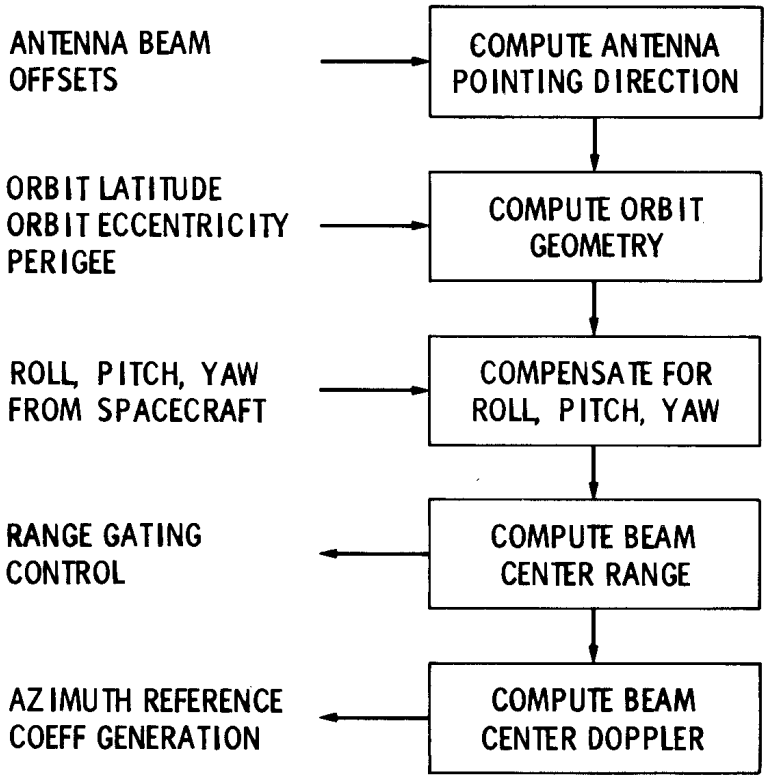

Figure 7 - Beam Center Range and Doppler Offset Computations

Clutterlock Control

A closed loop clutterlock system for determining and dynamically correcting for variations in antenna beam pointing using image data derived from multi-look processing is also included in the design of Figure 1. Figure 8 functionally illustrates the error detection concept while Figure 9 defines the error correction process. As noted from Figures 8 and 9, four microprocessors are required to achieve the total clutterlock control function.

Referring to Figure 8, the clutterlock control system receives single-look images from the azimuth correlator of Figure 1. The first microprocessor performs statistical accumulation and beam image generation. In performing this function it collects values from selected range and azimuth locations and integrates them into appropriate positions in a random access memory. After a suitable period of integration, the contents of this memory form a two dimensional histogram whose amplitude distribution approximates the surface referenced spatial distribution of reflected power in the radar signal. System timing is

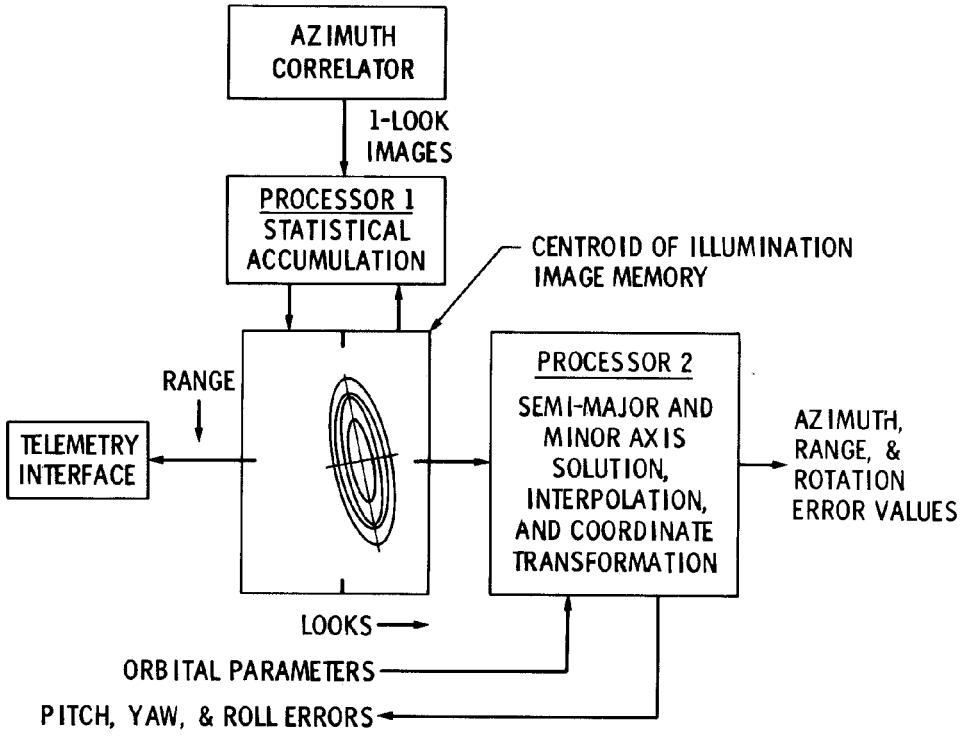

Figure 8 - SAR Antenna Pointing Error Detector Concept

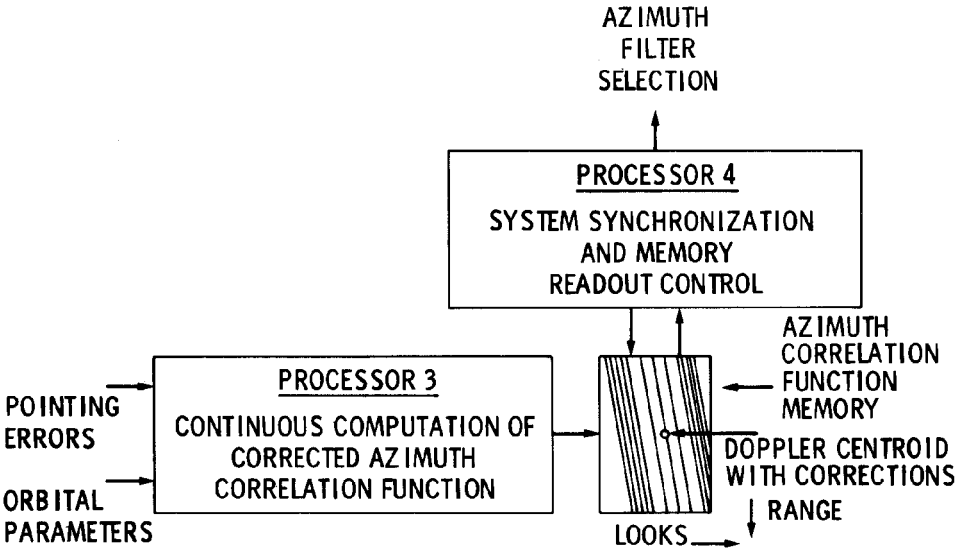

Figure 9 - SAR Antenna Pointing Error Corrector Concept

selected so that the coordinates of this memory are related directly to constant range and doppler terms (determined by orbital parameters, radar pulse repetition frequency, and time-bandwidth product). As the centroid of radar illumination may not coincide with the doppler centroid (due to attitude control errors) the histogram will usually be offset from the central coordinates of the memory. The beam image will exist with three degrees of freedom in position (range, azimuth, and twist) and two in size (major axis length and minor axis length).

The second microprocessor of Figure 8 functions as an ellipse solver. As such, it continuously processes the contents of the beam image memory and computes the position and orientation of the semi-minor and major axes of the illumination ellipse. It is in this processor that positional anomalies present in the beam image are translated, by appropriate coordinate transformation, into error values for spacecraft pitch, yaw, and roll. The option exists for providing these signals to the spacecraft attitude control subsystem in the form of residuals if desired. In addition to the computation of attitude control errors, the ellipse solver also computes the magnitude and character of orientation errors and their derivatives in the radar antenna coordinate system.

As noted previously, the implementation of Figure 9 uses the error detection information from Figure 8 to compute the error correction function. Referring to Figure 9, microprocessor 3 functions as the azimuth correlation function generator, continuously processing pointing error information. These values are stored in appropriate locations in an azimuth correlation function memory from which they are periodically delivered to the azimuth filter chips of Figure 4. The result of this process is the migration of the vertical doppler centroid toward the illumination centroid of the radar beam.

In view of the numerous azimuth filter channels associated with the design of Figure 4, system synchronization and memory readout control will be a significant processing task. Therefore, a dedicated microprocessor (microprocessor 4) is included in Figure 9 to achieve this function.

CONCLUSIONS

Range and azimuth correlation in the time domain using current state-of-the-art LSI CCD technology provides a potentially practical means of achieving real-time pipeline processing of SAR images for spacecraft SAR missions. However, numerous complex computations must be continuously effected as a function of orbital geometry to derive and update the reference function coefficients and correction factors necessary to accomplish these correlations. Without LSI microprocessor technology, the controller implementation required for future on-board spacecraft processing applications would be extremely difficult if not impractical.

ACKNOWLEDGMENTS

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