DEFINITION OF A FULLY COMPLIANT IRIG RECORDING SYSTEM FOR TELEMETRY

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ABSTRACT

Alliant Techsystems' Advanced Technology Applications organization incorporates the latest IRIG standards for range equipment and operation. Over the past five years, our objective has been to assure interoperability among diverse data recording users while achieving technical excellence for our ADARIO(**A**nalog **D**igital **A**daptable **I**nput **O**utput) family of products. In this paper, we summarize 25 years of ADARIO development; technical challenges, risks and processes; as well as our five-year effort to modify and develop our recording system products to meet the evolutionary standards of technical excellence.

KEY WORDS

ADARIO, IRIG, Multiplex/Demultiplex

INTRODUCTION AND BACKGROUND

The Inter Range Instrumentation Group (IRIG) provides the criteria for range equipment and operation. These standards are published by the Range Commanders Council (RCC), an assemblage of Government with representations from the Army (5), Navy (5), Air Force (6) and NASA. Standards are updated to be consistent with state-of-the-art technologies. Compliance to these standards assures reliability in operations as well as interoperability among many users with different cost effective technologies. As an added value, these standards can be easily applied across many diverse telemetry applications to enhance flexibility among users.

IRIG Compliance for Data Recording

Two major parameters, *Data Format* and *Tape Format,* are the compliance drivers for IRIG in the digital recording industry. Both *Data Format* and *Tape Format* requirements must be adhered to for full IRIG compliance. We define these format requirements as:

- *How data enters the tape recorder* Data Format Compliance
- *How data is stored on tape* Tape Format Compliance

Since 1993, the requirements for both formats have evolved systematically as summarized in Table 1. They were developed from customer technical needs; selected from non-proprietary technologies based upon completeness and suitability and then refined. Tape format compliance started with 19mm large format tape to now including S-VHS cassettes.

Table 1. IRIG Compliance Parameters-Evolution of Technical Excellence

Data Format Compliance

- ADARIO Multiplex/Demultiplex Standard for Multiple Data Channel Recording IRIG 106-93 ADARIO Paragraph 6.14
- IRIG 106-96 ADARIO Paragraph 6.15 Modified Appendix G Modified)

Tape Format Compliance

- IRIG 106-93 Paragraph 6.13
- 19mm Digital Cassette Helical Scan Recording Standards
- IRIG 106-96 Paragraph 6.16 Added
- 1/2-Inch Digital Cassette (S-VHS) Helical Scan Recording

Data Format Selection

Data Format selection for an IRIG compliant product presents significant ***challenges***. The selected format must:

- *Have general applications for a broad base of users*
- *Have growth capabilities for future related products*
- *Be scaleable to be implementable with current and future technology*
- *Be non-trivial to minimize early entrance of competition.*

The IRIG **A**nalog/**D**igital **A**daptive **R**ecorder **I**nput/**O**utput system (ADARIO) *Data Format*s meet all of the above criteria. The *Data Format* is for general analog and digital

signals recorded on a single channel digital recorder, therefore; it applies to all telemetry signals. *The customer base is currently using analog recorders that have limited channels and limited dynamic range*.

The format provides growth capability from low-rate signals such as voice and low-rate data that can be recorded on any media to high-rate signals that are yet to be implemented in telemetry (over 1 Gbps channel rates), and beyond the current capability of any recording media (3.1 Gbps aggregate). The format based products can be scaled from low-end software based formatters/de-formatters using any low-cost computer peripheral for storage with aggregate rates of less than 5 Mbps. *Medium range* products are based on hardware assisted formatting/de-formatting and instrumentation adapted digital video recorders with rates up to 120 Mbps. *High-end* products are based on all hardware implementation using ECL and high-speed CMOS with high-end instrumentation recorders up to 512 Mbps. *Current technology using high-speed FPGAs and GAS logic permits future products based on the format to achieve over 1 Gbps aggregate and channel rates*. Also, the analog front-end requirements are scaleable from a simple successive approximation A/D to high-end flash converters at 130 Mega samples per second and high resolution providing wide dynamic range that was not possible with analog recorder technology.

Data Format compactness (less than 3% overhead), which permits complete time coherent reconstruction of the original signals with no prior knowledge, presents significant design and implementation challenges. The format overhead provides all information pertaining to the recorded data and essential dynamic variables that relate the phase and frequency of each channel, in a compact packed binary form, and require innovative digital and analog implementation to reconstruct the recorded, *packetized*, data with the desired correlation. This makes the format non-trivial that requires high-resource commitment for competitive products. Also the compactness and time de-coupling of the input processing from the output process by the *Data Format* permits the same ADARIO *packetized* data to be transmitted via ATM links with real time reconstruction at the destination which the standard Time Division Multiplexing can not accomplish.

Consequently, meeting *Data Format* compliance requirements, realized in IRIG-106-96, extrapolated to its maximum, poses no limitations to data acquisition only challenges. The current maximum *Data Format* specifications are:

- Maximum Aggregate Rate **3.144 Gbps**
- Maximum Channel Bit Rate **3.144 Gbps**
- Maximum Channel Bandwidth **52.4MHz**
- Maximum Sample Size **24 Bits**
- Phase Coherency **8 Nanoseconds**
- Maximum Channel Count **256**

ADARIO Development

Development of the initial ADARIO product represents over 25 man-years of effort. The development started with formation of a very close technical team and partitioning of the concept based on the format into functional modules. Simultaneously, an extensive ***current technology capability*** study began with the goal of defining sufficiently mature components that may be applicable to the product such as the:

- *Highest speed A/D*
- *D/A*
- *Programmable Logic Devices (PLDs) in the high-speed CMOS and ECL families*
- *ASICs*

and controlled impedance large form factor printed circuit board capabilities and connectors. The initial partitioning estimates for each card resulted in approximate complexity of over 1 million gates, 1K to 2K circuit nodes, and required system clock rates of 100 MHz and the system consisting of at least 5 card types. Technology study indicated that the highest speed parts consist of less than 2K gates (ECL PLD 20EV8) and ASIC of 20K to 30K gate complexity were applicable. *This resulted in high design risk due to human error, and high cost of ASIC design iterations.*

Solution to the risk was to rely heavily on CAD with schematic capture and extensive logic and timing simulation capability. The simulation resulted in significant design error reduction and yielded high complexity cards with minimal errors. However, over reliance on simulation resulted in attempts to simulate the complete system of over 8 million gates including analog phase locked loops, which resulted in few hundred hour simulation runs with minimal returns. Actual system tests, accomplished in a few hours, were more efficient in locating system level problems. The key lesson learned is to know when you are reaching the limits of the tools.

The schedule (3-year) and complexity (over 20 man-years) of design mandated *concurrent engineering*. *Concurrent engineering* was successful because of top-down design approach and close communication between team members forced by the proximity of the CAD work stations with complete sharing of design files and location of the design team in one large room. This resulted in immediate resolution of interface issues and free interchange of ideas without extensive revisions of formal ICDs. Waiting for new revisions. ICDs were completed at design completion for reviews and future modifications. *These may be old concepts but they resulted in an excellent product that exceeded original expectations with long future and further technology challenges.*

The challenges for future ADARIO products is to:

- *Incorporate capability to record or play other formats*
- *Reduce cost and size with new technology while enhancing reliability due to lower component count*
- *Reach the ultimate limits of the Data Format which places a **technical challenge** on the recorder capability.*

ADARIO Family of Products

A chronology of ADARIO products, Figure 2, shows the evolution from a Basic ADARIO 400 in 1990, *(developed with a heavy application base in instrumentation)* to our full modular ADARIO 512 in 1997 *(modified to meet the latest compliance to IRIG 106-96).* Our near future release ADARIO 1000 will extend data rates beyond 1Gbps and broaden applications into Asynchronous Transfer Mode (ATM) applications.

Figure 1. ADARIO Family Chronology

As detailed in Figure 1 above, our products have evolved to meet the following IRIG 106-96 characteristics:

- 512 Mbps
- 76 Channel Capability
- Multiple Recorder Outputs
- High Efficiency Data Formatting 2.34%
- Adaptable Clock Rate
- Max IRIG Compliant
- Flexible System Control
- Dynamic Channel Allocation
- 10 Nanoseconds Channel-to-Channel Coherency

The adaptable clock rate allows ADARIO to work efficiency with buffered recorders by adjusting recording clocking rate coincident with changes in data aggregate. Dynamic channel allocation allows users to activate/deactivate data channel as needed during a record session. In terms of systems control, ADARIO provides integrated control for both ADARIO and recorder(s). It has extensive on-line bit and fault isolation. Control interfaces include IEEE-488, TCP/IP (Ethernet) and RS-232/RS-422. In addition to Graphic User Interface (GUI), our systems control easily extends for simultaneous control of multiple ADARIO/Recorder Systems. Table 2 lists the current recorders that ADARIO supports and those exhibiting IRIG compliance:

"Ensure interoperability between ranges and compatibility of range users' equipment with the ranges."

Table 2. Recorders Supported by ADARIO

ADARIO Card Designator		Recorder	Rate	IRIG Tape Compliance
GRIC	DRIC			
	*	Schlumberger	480 Mbps	(ID-1)
*	*	Datatape LP 200	200 Mbps	(ID-1)
	*	Datatape LP 400	400 Mbps	(ID-1)
*	*	Sony DIR 1000L	64 Mbps	(ID-1)
*	*	Sony DIR 1000M	128 Mbps	(ID-1)
*	*	Sony DIR 1000	256 Mbps	(ID-1)
	*	Sony DIR 1000H	512 Mbps	(ID-1)
*	*	AMPEX DCRSI	107Mbps/240 Mbps	
*	*	AMPEX DIS 120	120 Mbps	
*	*	AMPEX DIS 160	160 Mbps	
*	*	Metrum 32 VLDS	32 Mbps	VLDS
*	*	Metrum 64 Mbps	64 Mbps	VLDS
*		Sony DTF	120 Mbps	
*		Exabyte		
*		Manmoth		

Our future ADARIO 1000 release is a representative of continuous improvements throughout the evolutionary IRIG compliance cycles.

REQUIREMENTS VS. PERFORMANCE SUMMARY

Alliant Techsystems recently integrated a fully compliant IRIG system for an Air Force range application. Table 3 lists the requirements for that system versus the achieved performance using IRIG 106-96 compliant equipment.

Table 3. Requirements vs. Performance

Mux and System

Requirements: IRIG Compatible	Performance: ADARIO 256B
• 16 Digital PCM Channels	• 16 PCM Channels
• 2 Time Code Channels	• Dual Analog Channels
• 1 Analog Channel (Up to 2MHz)	• 400 KHz Analog Channel
• Autoranging Input (0-25 Mbps)	• Autoranging Input (0-26 Mbps)
• Autoaggregate Output (0-64 Mbps)	• Autoaggregate Output (0-256 Mbps)
• Low Overhead	• Overhead <2%
• Timescale 8:1	• Timescale 16:1
• PC GUI-Based Control	• Labview GUI on Windows 95/NT
• Phase-Coherent Multiple channel Playback	• IRIG Compliant:19-Channel Playback
• Tape Dubbing	• Tape Dubbing With Playback (Simultaneous Data processing During Dubbing)
• Unlimited Record Time	• Ping-Pong (Dual Interface Capability)

Recorder

Requirements	Current Performance
• IRIG Compatible	• Metrum VLDS
• Continuously Variable Record/Playback	• Buffered
• Low Error Rate	• 1×10^{-11} Bit BER
• Quick Change of Tape	• Cassette
• Inexpensive Media	• SVHS Cassettes
• Search Capabilities	• Fast Search by PBN
• Remote Control	• RS-232

FUTURE ENHANCEMENTS UNDER DEVELOPMENT

As stated previously, our future ADARIO 1000, is a representative of continuous improvements throughout the evolutionary IRIG compliance cycles. In addition to Sun compatibility for control, we are now incorporating:

- Seamless Playback — *The ability to playback completely autonomous record session with equipment reset, reconfiguration or loss of sync*
- Positive Record Feedback — *The ability to emulate via software control **Read after Write** verification (Simuplay) for those recorders that are **Write Only** and **Read Only** machines*
- Time Code Search — *The ability to search/position tape based upon stored time code (Present capability utilizes PBN (Principal Block Number).)*