LSI DEVICES FOR FAULT-TOLERANT SPACEBORNE COMPUTER

Charles Bennett
LSI Development Manager
Fault-Tolerant Spaceborne Computer Program
Equipment Division, Raytheon Company
Sudbury, Massachusetts 01776

ABSTRACT

In order to meet the requirements for future satellite applications, a brassboard of an extremely reliable fault-tolerant spaceborne computer (FTSC) has been developed by Raytheon Co., Sudbury, MA., under the sponsorship of the USAF/SAMSO[*]. The requirements for the FTSC were high reliability, high speed, low power, high density and tolerance to space radiation environments. The reliability requirements were realized through several unique system and circuit concepts while the remaining requirements could only be realized through use of large-scale-integrated (LSI) circuit technology. An assessment of possible candidates for the LSI requirements for the FTSC was performed on available and emerging technologies. Once the candidate LSI technology was selected, a "proof-of-technology" program was instituted. The program included the development of a test chip to prove the operational characteristics of the technology and its producibility. Development of flyable prototypes of the FTSC using LSI devices is the final program goal.

INTRODUCTION

Standard requirements for satellite electronics are high reliability, low power, low weight, and (depending on mission requirements) high speed and radiation tolerance. For future satellite programs, an emphasis will be placed on the ability of the on-board computer to autonomously control the vehicle with a high probability of successful operation for extended periods of time. One of the most likely candidates to fulfill such a requirement is the Fault-Tolerant Spaceborne Computer (FTSC). Key features in the architecture of the FTSC are its modular redundancies, its subelement redundancies and its heavy reliance on large-scale-integrated (LSI) devices to obtain ultra-high reliability.

The theme of this paper concerns the steps involved in the LSI development for the FTSC. Substantial use of LSI devices is required to meet the FTSC reliability goals (95% probability of successful operation after 5 years in orbit). The plans for development of the FTSC LSI devices will be discussed with respect to the FTSC requirements. Characteristics of various candidate LSI technologies, methods of proving the capabilities of the technology and methods of proving the technology in various system environments will also be considered.

I. REQUIREMENTS FOR FAULT-TOLERANT SPACEBORNE COMPUTER

Satellite computers of the future will require a high probability of successful opration after extended on-orbit space missions. Previous NASA[1] and SAMSO[2] studies performed at Raytheon Co., Sudbury, MA., have evolved a computer architecture that satisfies these requirements. This concept involves the use of modular redundant computer elements, as well as subelement redundancies to satisfy reliability models[3] that effectively lead to systems that can have a 95% probability of successful on-orbit operation over a five-year space mission.

A. HIGH RELIABILITY REQUIREMENTS

Redundancy techniques developed in these cited studies lend themselves exceptionally well to the repetitive nature of some areas of computer architecture. The designation and management of spare elements of the computer are key factors for obtaining extremely high reliability computers. Computer memory is an area which is most readily adaptable to an effective sparing philosophy. All storage elements or bits of the memory are electrically identical. A failure in any one bit, therefore, can make the entire memory useless. If spare bits are included and a fail-safe switching technique employed to replace failed bits with these spare bits, the cited references infer that such a memory architecture will be considerably more reliable[1,2]. Such techniques when applied to spare blocks of memory, spare central processing areas, or in the sparing of bit lines in the buses that interconnect all portions of a computer can significantly improve the reliability. It should be noticed, however, that the switching required for the introduction of spare elements (such as an additional memory block) or of subelements (such as a bit line within a memory block) in themselves create an increase in system unreliability. However, with the extensive use of large-scale-integrated electronics, there will actually be less overall system components and, therefore, the reliability can again be made to increase.

B. HIGH SPEED REQUIREMENTS

In the FTSC, speed is an important factor because of the increase in logic levels involved in the special spare element switching. Increased bus loading, caused by sparing on the

memory block level, is also a factor. The FTSC prototype development specifications require the system to have a throughput of 200,000 operations per second for a particular defined instruction mix. This leads to an average gate propagation delay in the 5 to 10 nanosecond range.

C. LOW POWER REQUIREMENTS

As in all satellite applications, power is of primary concern. For the FTSC, there is an apparent increase in power due to additional circuits required for the fault tolerance of the system. With the choice of an optimum LSI technology, power can be reduced through the use of more on-chip circuitry with less parasitic capacitance. The FTSC system requirement is that it dissipate 35 watts or less. This is an extremely stringent requirement that dictates the use of an extremely low power LSI technology.

D. HIGH DENSITY REQUIREMENT

Another extremely important aspect of spaceborne electronics is that they require high packing density. An LSI device technology can reduce the quantity of packaged die in a system since more circuitry can be put on each die. With less die per system module, the modules can be made smaller leading to a smaller overall system. The overall FTSC requirements call for a system size of one cubic foot or less and a weight of 50 pounds or less. Again, the only effective means for achieving those goals is through extensive use of LSI throughout the system.

E. RADIATION HARDNESS REQUIREMENT

For specific space missions the requirement that the system electronics survive and operate through particular radiation environments must be imposed. Radiation hardness goals set for the FTSC involve transient radiation as well as long term cumulative radiation dosages.

F. SYSTEM DESIGN GROUND RULES, SYSTEM COMPLEXITY AND PARTITIONING

For the design of the FTSC, certain design ground rules had to be followed:

- LSI devices are used throughout the digital design. The least number of circuit devices are utilized to increase system reliability, increase system speed, decrease system size and weight.

- The quantity of inputs per gate is limited to three. This is required for use of Complementary Metal Oxide Semiconductor (CMOS) technology. The limitation of

three inputs is caused by the increase in threshold voltage in stacked p-channel transistors of a NOR gate after exposure to radiation.

- A family of circuit "cells" will be used to develop the LSI devices. These cells need be designed only once and their data stored in a computer data base to be called up as needed in the logic design and layout for a particular device design.

- LSI devices must utilize a maximum of 750 equivalent logic gates under normal circumstances. This is to force the LSI chips to maintain a size that is commensurate with a reasonable yield at wafer probe testing. An equivalent gate is considered a two-input gate. Device complexities of greater than 750 can be tolerated providing the device logic is highly regular leading to an inherently more dense layout.

- LSI devices are to be a product of the system partitioning and utilize no more than 84 input/output pins. This requirement allows for a standard LSI package to be utilized while maintaining an optimum density for the average LSI device partitioning.

G. SPECIAL FTSC REQUIREMENTS

Certain peculiarities of the FTSC architecture require special circuit considerations. Because of the system modularity requirements, the busing requirements are very stringent. Tied to the main system bus is a complement of up to 24 memory modules, four Central Processor Units, four Direct Memory Access Units, and two Serial Interface Units for a total of 34. This represents a very heavy capacitive load, especially for CMOS circuits, and special consideration must be given to the design of the bus drivers. Since the switching of spare elements and subelements is one main feature of the FTSC, a considerable number of transmission gates must be used.

II. LSI TECHNOLOGY COMPARISONS, ASSESSMENTS AND REQUIREMENTS

In order to satisfy reliability, speed, power, density and radiation hardness requirements for the FTSC system, an in-depth comparison had to be made of the available and emerging LSI technologies as they relate to FTSC system requirements. Restating the requirements--

(1) Reliability   95% probability of success after 5 years in orbit

(2) Speed   Gate delays of 5-10 nsec for fan-outs of 2-3

(3) Gate Density   750 gates (3000 devices) per chip; 84 pin-outs allowed

(4) Total Dose   Allowance for 30% parameter degradation
     Hardness

(5) Transient   Mission dependent
     Hardness

(6) Power   Static power (post-rad) small compared with dynamic power

(7) Producibility   Capable of demonstrating repeatability of processing

In assessing technologies that could meet these requirements, it became immediately apparent that to meet the reliability goals, a relatively small number of devices must be used to define the FTSC system. With the additional logic involved in fault-tolerant circuit techniques, high density LSI devices became a necessity. With high density and low static power as requirements, the use of the high power consuming, low density, relatively radiation intolerant technologies such as TTL and ECL were eliminated. Since Complementary Metal Oxide Semiconductor (CMOS) technology devices exhibit the lowest static power dissipation, relatively high packing densities and good tolerance to radiation environments, the assessment was quickly limited to the several CMOS technologies; namely,

Bulk silicon CMOS metal gate
Bulk silicon CMOS silicon gate
Silicon-on-Sapphire (SOS) CMOS metal gate
Silicon-on-Sapphire (SOS) CMOS silicon gate

A. LSI TECHNOLOGY SPEED CONSIDERATIONS

The speed or propagation delays of electronic circuits are dependent on the equivalent impedance of the driving source and the capacitive component of the load. For technologies such as T^2L, source impedance is small (usually 50 ohms or less) while impedance of the next stage is usually more resistive than capacitive thus a small R-C time constant leading to small gate propagation delays. For CMOS devices, the source impedance is fairly large (usually in the 1000 to 10,000 ohm range) while the load impedance is essentially capacitive due to the oxide insulated gate of subsequent stages. This leads to large gate propagation delays. Table 1 shows the levels of device capacitances, the relative inverse gain factor and the average gate delay for the various CMOS technologies. The relative inverse gain factor is a weighting factor[4] which considers lower mobility in SOS transistors when compared to bulk silicon. The discrepancy in drive capability, or on-resistance, between SOS and bulk CMOS could be as much as a factor of two as is evident from the table. The effective capacitance of each

CMOS technology is the product of the inverse gain factor and the total capacitance. The gate delay times are related to the effective capacitance for the CMOS technologies with fan-outs of 2 to 3.

Node capacitance is 60% to 70% higher in bulk silicon gate CMOS with respect to the SOS Si-gate due to the drain to body capacitance. This is virtually absent in SOS. The interconnect capacitance in bulk silicon gate is assumed equal to the node capacitance just as in the case of bulk metal gate. Comparing the node capacitance of SOS silicon gate to SOS metal gate shows a larger value of capacitance for SOS metal gate caused by the non self-aligned nature of the metal gate. The inverse gain factor for the SOS metal gate accounts for the additional reduction in n-channel mobility due to increased doping required to achieve the same pre-rad threshold in metal gate SOS as in silicon gate SOS. It becomes apparent from Table 1 that silicon-gate CMOS/SOS has a distinct speed advantage over the other CMOS technologies.

B. LSI TECHNOLOGY POWER CONSIDERATIONS

An FTSC requirement, as previously stated, is: static power consumption after total dose should be small compared to dynamic power consumption. The following simple formula is commonly used to estimate dynamic power consumption per gate:

$$P = CfV^2$$

where P is power in watts; C is capacitance in farads; f is frequency, and V is voltage. For SOS silicon gate, on-chip capacitance from Table 1 is in the 0.75 to 1.5 pf range. If C = 1 pf, f = 2.5 MHz (the projected FTSC clock rate) and V = 10 volts,

$$p = 1 \times 10^{-12} \times 2.5 \times 10^6 \times (10)^2 = 2.5 \times 10^{-4} \text{ watts or } 250 \text{ }\mu W.$$

This is a representative dynamic power consumption value per gate in SOS silicon gate at the maximum FTSC clock rate. From Table 1 it is obvious that dynamic power consumption of other CMOS technologies is greater due to the larger capacitance per gate. It has been shown[5] that post radiation leakage per mil of transistor width can be kept to less than 0.1 μA. An LSI device containing an average of 500 gates (or 2000 transistors) yields a total of 2000 mils of transistor width and the total leakage would be 200 μA or 2 mW dissipation at 10 V bias. This power consumption is 1/6 the average power consumption at 2.5 MHz for 500 gates with 10% usage or 12.5 mW. On a per-gate basis, assuming 4 linear mils per gate, post-rad leakage would then be only 0.1 x 4 x 10 = 4 μW per gate compared to the previously calculated 250 μW of dynamic power consumption per gate at 2.5 MHz (the maximum projected FTSC clock rate).

C. LSI TECHNOLOGY DENSITY CONSIDERATIONS

A comparison of the average area in mils^2/device for the four CMOS technologies with respect to various developers standard cell families is as follows:

Bulk silicon CMOS metal gate:	40-50 mils^2/device
Bulk silicon CMOS silicon gate:	15-25 mils^2/device
CMOS/SOS metal gate:	10-20 mils^2/device
CMOS/SOS silicon gate:	7.5-15 mils^2/device

For the FTSC requirements that LSI devices contain up to 750 equivalent gates (or 3000 transistors), a 220 x 220 mil chip would require an area of 16 mils^2/device. The 220 x 220 mil chip area will support the 84-pin requirement with adequate margins. From the above table, it becomes apparent that bulk CMOS technologies exhibit marginal to poor device areas while CMOS/SOS technologies exhibit adequate device areas. It is a well known fact that increasing the area of a die lowers the yield of acceptable die thus increasing device costs.

D. LSI TECHNOLOGY RADIATION CONSIDERATIONS

Hardness capabilities of the four CMOS technologies are listed in Table 2. It may be seen that total dose hardness is highest for metal gate bulk CMOS. More experience has been applied to hardening this CMOS technology. However, the learning curve for hardening of silicon gate technology is expected to be steeper. One main difference in the hardness of different CMOS technologies lies in gate oxide processing. The radiation-induced charge builds up in the gate oxide causing a shift in voltage threshold levels of p- and n-channel transistors of complementary transistor pairs. The basic problem in hardening the gate oxide of silicon-gate CMOS devices is the growth of oxide near the beginning of the processing cycle whereas the oxide of metal gate technologies is grown near the end of the process steps. Any high temperature process steps, beyond gate oxidation, tend to anneal out the oxide hardness. Examples of high temperature steps are the diffusion of sources and drains and the doping of polysilicon gates. Ion implantation techniques and/or low temperature diffusions alleviate the problem.

Speed degradation is another adverse condition brought about by radiation. A measure of degradation can be determined by p-channel threshold shift[6]. Assuming that the on-resistance of the device is proportional to $(V_{DD}-V_{TP})^{-1}$ and that the delay is proportional to that on-resistance, the increase in device delay can be determined. If the p-channel pre-rad threshold is 1.0 V and the post-rad threshold has shifted an additional 2.0 V and V_{DD} = 10V, the change in device delay would be $(10-1.0)/(.10-3.0)$ = 1.29 times the original delay.

E. LSI TECHNOLOGY SELECTION FOR THE FTSC

When comparisons of the various CMOS technologies are factored against defined FTSC requirements, it becomes evident that the advantages of speed, power and density favor selection of CMOS/SOS silicon gate technology. Transient radiation hardness favors both SOS technologies because of the isolation properties of the sapphire substrate for individual devices. Total dose hardness favors both metal gate technologies because of the experience level in their processing. Silicon gate total dose hardness is just at a point where it satisfies the present FTSC hardness goal. Thus, it has been determined that CMOS/SOS silicon gate technology will be developed to satisfy FTSC requirements for an LSI technology.

F. LSI TECHNOLOGY DEVELOPMENT

Aside from the special fault-tolerant architecture employed in the FTSC system design, the most important other factor that will assure required FTSC reliability levels is extensive LSI usage throughout the system. In order to assure timely development of the FTSC system, it was decided to have dual sources for LSI devices. An optimum situation would occur if the two developers could process devices from each other's mask sets. Because of the similarity and compatibility of design and processing techniques, Hughes Aircraft Co. and RCA were the two developers selected. The personnel, experience and facilities of these two organizations are excellent.

III. PROOF OF LSI TECHNOLOGY

During the period from May 1975 to December 1976, the Brassboard Fault-Tolerant Spaceborne Computer (BFTSC) was successfully designed, fabricated and debugged at Raytheon Co., Sudbury, MA., under a contract with the USAF/SAMSO. The objective of the BFTSC was to prove the fault-tolerant concepts as originated in the cited architectural studies[1,2]. The BFTSC was fabricated utilizing the Fairchild 34000 family of CMOS logic and consists of 11,000 integrated circuits. The program has successfully proved the architectural and operational feasibility of fault-tolerant concepts. That phase of the program will be followed by a prototype phase. The goal of the prototype phase will be to redesign and develop the FTSC in final form, fit and function as a flyable, developmental prototype model. In progressing from brassboard to developmental prototype phase, the use of LSI devices is planned in place of the small-scale-integrated (SSI) devices. It has been shown how the technology assessment pointed towards CMOS/SOS silicon-gate technology to satisfy all FTSC requirements. However, the selected technology was not considered of sufficient maturity to allow development of the prototype without further characteristics studies. SAMSO decided that a proof-of-technology program should be instituted in parallel with the prototype system design activities.

A. INTERIM TEST CHIP DEVELOPMENT PROGRAM

The proof-of-technology program was instituted through development of a test chip utilizing CMOS/SOS silicon-gate hardened LSI technology. The test chip[7] was specified by Raytheon with inputs from SAMSO, SAMSO's advisors and the eventual test chip developers (Hughes Aircraft and RCA). The test chip was to be designed with three main functional areas: An 8-bit ALU test area, a cell-family test area, a physics devices test area. The 8-bit ALU area was to prove the capability of utilizing a family of cells in its design while projecting eventual FTSC chip densities. The cell-family area was to prove the operability of cells peculiar to the FTSC design requirements. The physics devices area was to provide data on key parameters of CMOS/SOS silicon-gate technology. The overall goal of the interim test chip development program was to prove the hardened CMOS/SOS silicon-gate technology capabilities to the point where further design and development could be used in the FTSC.

B. PROOF OF TECHNOLOGY DENSITY

An 8-bit ALU was chosen to prove the density of the selected LSI technology. This selection was made because the layout and cell interconnections of an ALU lie somewhere between the high density of a highly-ordered register-file type circuit and the low density of the relative disarray of random logic circuits. The actual ALU was implemented by Hughes and RCA with approximately 1100 transistors. The active area involved was approximately 100 x 110 mils or approximately 10 mils^2 per transistor. This is well within the requirement of 7.5-15 mils^2 per device.

C. PROOF OF TECHNOLOGY CHARACTERISTICS

To prove the actual characteristics of the LSI technology, a representative complement of cells that would be used on actual FTSC LSI device designs were placed on the test chip. Separately powered chip areas were to be tested as a specific fault-tolerant requirement. Timing strings of loaded and unloaded NAND's and NOR'S were included to prove the requirement of gate delays to be in the 5 to 10 nsec. range. Physics-type experiments were also included. P- and n-channel transistor pairs with different channel lengths were placed on the test chip. These test transistors were used to determine threshold voltages, drive current capabilities and leakage currents for both pre- and post-irradiated conditions. Metal and polysilicon interconnection experiments were included to perform resistive measurements and for visual examinations of vias and step coverage integrity. A large capacitor was included for determining the properties of the hardened gate oxide as created by normal processing techniques.

D. PROOF OF FTSC SPECIAL CELLS

Part of the test chip was devoted to circuits that are peculiar to the FTSC design requirements. Among these were the three-input separately powered voter and the bus transceiver with large capacitive drive capability.

E. PROOF OF TECHNOLOGY PRODUCIBILITY

One major reason for the interim FTSC test chip development program is to prove the producibility of the LSI technology. Part of that proof is the capability of the selected device developers (Hughes and RCA) to design, process and test a specific device and measure the characteristics of the resultant devices from a minimum of two wafer lots. As previously mentioned, the test chip has an 8-bit ALU was well as cells/physics devices (each area being accessible via 40 I/O pads). Three test configurations have been specified for packaging:

- 40-pin ALU configuration
- 40-pin cells/physics configuration
- 84-pin composite configuration

The composite configuration brings out all 80 pads from the entire test chip onto 80 pins of a specially developed 84-pin flat package.

F. PROOF OF TECHNOLOGY TEST PROGRAM

A test program[8] has been developed for performing functional, static, dynamic and parametric testing of the several test chip configurations. The overall objectives of the test program on the test chip are to prove the characteristics (operational, environmental and radiation) and producibility (multiple wafer lots) of CMOS/SOS silicon-gate technology at the various device developers.

IV. PROOF OF FTSC SYSTEM DESIGNS

The Brassboard FTSC was designed with SSI CMOS devices. System functional modules were partitioned into a quantity of circuit cards, each of which represented one eventual LSI device. The brassboard involved 220 circuit cards, each containing 50 integrated circuits for a total of 11,000 integrated circuits. There are presently 20 LSI device types (less memory devices) into which the FTSC has been partitioned. These devices vary between 160 and 1250 gate complexity. The 160 gate device is a buffer-driver interface that contains few equivalent gates with most of the chip area taken up by large bus drivers. On the other extreme, the 1250 gate device is the bit rippler that contains 24 highly

repetitive and dense elements. Analysis of the bit rippler design has shown that it can be designed onto a chip of approximtely 160 x 240 mils. The Brassboard FTSC successfully proved the fault-tolerant concepts for which it was built. Since then, some redesign has occurred along with several important system enhancements. Another SSI computer is being built to prove the newly identified improvements. This improved design is designated as the Engineering Test Model (ETM).

The ETM is to be designed, fabricated and utilized in a manner similar to the original Brassboard FTSC. Each circuit card will represent one eventual LSI device. One role of the ETM, that differs from the original BFTSC, is for it to have a companion circuit card for each unique representation of an LSI device. That circuit card is to accept one LSI device. The card will be plugged into the ETM system substituting for the original SSI representation of the LSI function, thereby testing the overall correctness of the actual LSI device. Once the "proof-of-design" LSI device has been proven to operate as expected in the system configuration, it can then be released for the next level of development.

Following the ETM development, an Engineering Development Model (EDM) is to be built. This model will be a form, fit and functional model of the final prototype FTSC. It also acts as the test bed in which the LSI devices will be given their operational testing prior to final release. In this EDM, the LSI devices will be given an effective dynamic as well as functional test. Once the LSI devices have been successfully tested, they will be "released" for final quantity processing for use in the prototype FTSC.

CONCLUSIONS

Reliability modeling and LSI technology analyses and trade-offs have proven that LSI devices are a must in meeting the goals of the FTSC. The program involving development of CMOS/SOS silicon-gate technology will allow the FTSC to meet its stringent reliability, speed, power, weight, size and hardness goals.

REFERENCES

1. Modular Spacecraft Computer Study, SAMSO Contract F04701-71-C-0362, 6/71-12/71.
2. Data Management System Study, SAMSO Contract F04701-71-C-0362, 1/72-7/72.
3. Reliability Model Derivation of a Fault-Tolerant Computer Configuration, NASA Contract NAS-12668, 6/73-3/74.
4. Seavey, M.H., "LSI Technology Assessment for FTSC," Internal Raytheon memo, EM76-0647, p. 25.
5. Ibid. p 45.
6. Ibid. p 36.

7. "Design Specification Interim FTSC Test Chip Hardened Si-Gate CMOS/SOS," Raytheon Spec. 978951, Rev. A. 20 October 1977.
8. "FTSC Test Chip Test Plan," Raytheon Spec. 978952, Rev. A, 5/15/78.

TABLE 1

CMOS LSI DEVICES -- CAPACITANCE AND DELAY INFORMATION

Type of Gate	Node Cap.(pf)	Interconn. Cap. (pf)	Total Cap. (Pf)	Relative Inverse Gain Factor	Effective Cap. (pf)	Gate Delay (ns)
Bulk Metal	4 - 6	4 - 6	8 - 12	1	8 - 12	27-40
SOS Metal	1.5 - 2.5	<0.1	1.5 - 2.5	3	4.5 - 7.5	15-25
Bulk Silicon	1.5 - 2.5	1.5 - 2.5	3 - 5	1	3 - 5	10-17
SOS Silicon	0.75 - 1.5	<0.1	0.75 - 1.5	2	1.5 - 3	5-10

TABLE 2

CMOS RADIATION HARDNESS LEVELS

Type of Gate	Neutron Hardness (n/cm^2)	Total Dose Hardness (Rads)	Dose Rate Hardness (Rads/Sec.)
Bulk Metal	$>10^{15}$	$(0.5 - 5) \times 10^6$	$10^8 - 10^{10}$
SOS Metal	$>10^{15}$	$(0.5 - 5) \times 10^6$	$10^{10} - 10^{11}$
Bulk Silicon	$>10^{15}$	$(0.5 - 5) \times 10^5$	$10^8 - 10^{10}$
SOS Silicon	$>10^{15}$	$(0.5 - 5) \times 10^5$	$10^{10} - 10^{11}$