ABSTRACT

A Fault Tolerant Spaceborne Computer is being developed for long duration military space missions. The user requirements, the architecture, the computational characteristics, the LSI microcircuit technology selected and the program’s present status are described.

SUMMARY

The Fault Tolerant Spaceborne Computer (FTSC) is being developed by the U.S. Air Force Space and Missile Systems Organization (SAMSO) in support of long-duration space missions. The overall objectives of this program are to define, develop, and flight test a general purpose, highly reliable spaceborne computer that will have the computing capability required to meet on-board requirements of future Air Force space programs; the reliability, survivability and autonomy characteristics required to support the overall mission requirements in these areas; and a power, volume, and weight requirement significantly below those required by conventional computer architectures. Following study and simulation phases, a brassboard (a packaged and transportable breadboard) was completed in late 1976 by Raytheon Company. The program is now ready to enter the flight prototype phase.

The FTSC uses redundancy at three levels to achieve the desired reliability (95 per cent probability of surviving at least five years): Triple Modular Redundancy, Spare Module Redundancy, and Subelement Redundancy. Two primary considerations influenced the levels at which redundancy was applied in the FTSC: the need to minimize the power, weight, and volume penalties associated with the redundant elements and the desire to eliminate all single point failures. The program objective of autonomous recovery from faults was meet by distributing the fault detection logic throughout the logic, providing a hardware configuration control unit to reassemble a minimal system after a fault is signaled, and using software recovery of the full system and the user program environment.
Computationally, the FTSC provides 32-bit integer and floating point data formats, 60K words of user memory, eight general purpose registers, eight addressing modes, and 95 instructions. It executes a typical navigation-oriented instruction mix at 200,000 operations per second.

The FTSC is being implemented using complimentary metal oxide semiconductor - silicon on sapphire (CMOS/SOS) technology because of its transient and total dose radiation hardness and because of the speed and power constraints. The FTSC design uses 21 types of custom CMOS/SOS microcircuits of the 700-1200 gates per chip level of complexity.