EXPERIMENTAL 2 GBPS MM WAVE SYSTEM AND 4 GBPS QASK MODULATOR

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ABSTRACT

A 2 GBPS QPSK modulator and demodulator were developed and BER performance was evaluated over a millimeter wave data channel. The error rate measurements taken with the breadboard equipment showed system performance to be less than 2 dB from theoretical at an error rate of 10^{-5}. Additionally, a second QPSK modulator was constructed and combined with the first to generate 4 GBPS QASK data for future evaluation.

INTRODUCTION

The continuing demand for communication satellites to provide data channels at increased rates has prompted an experimental program investigating multigigabit communications technology. The initial program objectives were to develop a broadband millimeter wave satellite channel, a 2 GBPS QPSK modem, and to evaluate the bit error rate performance of the resulting system.

The satellite channel included a low conversion loss millimeter wave to Ku band mixer, a Ku band parametric preamplifier and field effect transistor (FET) amplifiers, as well as channel filters. The modulator was formed from two bi-phase modulators, each consisting of an FET switch and a circulator. The two modulator channels were each driven with 1-GBPS data generated by multiplexing and latching the outputs of 500 MBPS shift register sequence generators. The demodulator included both carrier and clock recovery phase locked loops. Extensive use was made of Gallium Arsenide microwave integrated circuit technology in both the modem logic elements, and in the channel amplifiers.

Following evaluation of the 2 GBPS system, a second QPSK modulator was constructed and combined with the first to form a 4 GBPS QASK modulator. The next phase of this continuing program will be to develop the receiver circuits for demodulation and evaluation with 4 GBPS QASK operation.

SYSTEM CONFIGURATION

A block diagram of the system is shown in Figure 1. It includes a QPSK modulator operating at a 15 GHz carrier frequency, and an up converter which translates the signal to the millimeter (MM) wave region where it is passed through a single conversion transponder. The transponder translates the signal back down to 15 GHz and provides filtering and amplification. Following the transponder, noise is added to the signal before it is phase detected, filtered and latched in the demodulator. The recovered data is processed in error detectors to provide system bit error rate evaluation.

QPSK MODULATOR & DATA SOURCES

Two 1 GBPS data sources drive a quadrature pair of FET bi-phase modulators which operate on a 15 GHz carrier oscillator to form a 2 GBPS QPSK modulated signal at 15 GHz. The 1 GBPS data sources are each formed by multiplexing and latching the outputs of 500 MBPS PRN sequence generators.

The 500 MBPS PRN sequence generators are mechanized using Fairchild 11CO6 “D” flip flops. Each generator produces a maximum length sequence of 511 bits and generates two suitable phases of the word which are multiplexed to generate the original 511 bit word at twice the bit rate, or 1 GBPS.

The multiplexers are mechanized using two dual transistors, each having a common emitter connection. The 500 MHz clock signal and one 500 Mbps data stream are coupled to the respective base connections of the second dual-transistor. This mechanization produces a low logic level at the single ended output of each dual transistor only when its input clock signal is high and its input data signal is low.

Effective multiplexing of the two 500 MBPS data streams is obtained by wire “anding” the output collectors of the two dual transistors so that a low output level from either differential pair is produced at a common output.

The 1 Gbps data from each multiplexer is latched in order to improve the data waveform. The latch improves the normalization of high and low data states and of the data transition times.

The latch is mechanized using three dual transistors. One dual transistor forms the memory element of the latch, which is mechanized as a cross-coupled bistable multi-vibrator. The other two dual transistors function to set and reset the bistable circuit. The set and reset circuits each operate in a manner similar to that of half of the multiplexer

described above. The set and reset pulses are each injected through a Schottky diode to the appropriate base df the bistable multivibrator. A single transistor buffers the latch output.

The outputs of the latches each drive an FET bi-phase modulator. The modulators each use a GaAs FET to switch the length of a waveguide stub in the signal path. The modulator switch and stub are coupled to the transmission path using a circulator. The use of an FET switch to apply the modulation provides a high quality modulated signal because of the low AM/PM limiting of the input data provided by the FET switch. Other advantages of the FET waveguide modulator configuration are its low DC power consumption, its inherent isolation between input data and output RF provided by the waveguide in the output signal path, and its potential for even higher data rates on MM wave carriers. The multiplexer latch and modulator are packaged in one compact assembly to minimize reflections between circuits. A photograph of the assembly is shown in Figure 2. A photograph of the combined QPSK modulator is shown in Figure 3.

TRANSPONDER

The 15 GRz modulated signal is up converted to the MM wave region to provide an input for the breadboard single conversion transponder. The transponder consists of a low conversion loss mixer which downconverts the signal to 15 GHz, followed by a parametric preamplifier, FET amplifiers, and channel filter. The transponder provided a noise figure of 7.6 dB (6 dB mixer conversion loss followed by a system noise figure of 1.6 dB), a gain of 44 dB, and a 1 dB channel bandwidth of 2 GHz.

DEMODULATOR

The input signal to the demodulator is divided into three paths. One path goes to the carrier recovery loop. The other two paths drive a quadrature pair of Airtech double balanced mixers which operate as phase detectors. Following the phase detectors the signals are passed through data filter amplifiers which increase the signal level, and provide post correlation data filtering. The output of each amplifier is sampled by a latch similar to the multiplexer latch which drives the modulator. This latch is driven by a clock operating at one eighth the symbol rate, so that the reconstructed data emerges at 125 MBPS from each latch. This technique of undersampling the PRN data sequence allows BER evaluation using a conventional low speed BER test set.

Block diagrams of the carrier and clock recovery loops are shown in Figures 4 and 5. The carrier recovery circuit is an IQ loop, and the clock circuit consists of an edge detector followed by a phase locked loop. The clock circuit diagram illustrates the implementation of the one eighth rate clock to the latch. A photograph of the carrier and clock loops is shown in Figure 6.

PERFORMANCE EVALUATION

The high quality of the signals generated in the 2 Gbps system is demonstrated from waveform and spectrum photographs, as well as from a BER evaluation.

Figure 7 shows time and frequency domain displays of the waveforms which drive one of the biphase modulators. The first photograph shows a segment of the PN data sequence. Note the single bit pulses of 1 nanosecond duration (print through at the 1 GHz clock rate can also be seen as ripple on longer sequences of zeros or ones).

The second photograph is of the same waveform but with the time base expanded and the oscilloscope synchronized to the word clock rather than to the word pattern itself. This photograph shows the rise time to be approximately 200 psec. The last photograph is a frequency domain response of the same waveform and illustrates the near ideal (sin x)/x shape.

Figure 8 is a similar set of photographs, but taken at the demodulator phase detector output. This particular set of waveform responses was taken with the single conversion transponder bypassed. Once again, it illustrates the high quality of the waveforms encountered. The low AM/PM limiting of the FET modulator is demonstrated by a comparison of Figure 7 and 8. The waveforms of Figure 7 contain a substantial amount of clock rate ripple which is limited, but not converted to phase ripple, by the FET switch. The result is that the detected waveform of Figure 7 has substantially reduced clock rate ripple.

In addition to the circuits described above, a second multiplexer/latch assembly has been constructed using all gallium arsenide components. The GaAs multiplexer is mechanized using three FET chips. Two FETs perform the basic multiplexing operation while a third FET amplifies the output signal to a level suitable for driving a latch consisting of Hughes GaAs logic gates. This configuration offers the potential of operating to even higher data rates. A photograph of the GaAs multiplexer, latch and modulator assembly is shown in Figure 9. Multiplexer and latch output waveforms for the gallium arsenide circuits are shown in Figure 10. This figure can be compared to Figure 7 for the current system and illustrates even higher quality waveforms.

Bit error rate performance for the system is shown in Figure 11. The system was evaluated with the transponder bypassed (back to back) and with the transponder included. The measurements were taken with a strong signal into the transponder so that the preamplifier noise was negligible compared to the noise source (strong uplink, weak downlink). Degradation is approximately 2 dB with the transponder included. With the transponder bypassed, the degradation is slightly less.

4 GBPS QASK MODULATOR

A second word generator and FET modulator was constructed and integrated with the all GaAs multiplexer/latch assembly. This modulator and the original were driven with coherent carriers and their outputs were combined in a hybrid to form a 16 signal QASK modulator.[1] A block diagram of the configuration, along with a vector construction of the signal set, is shown in Figure 12. A photograph of the hardware is shown in Figure 13.

The QASK set of 16 signals has advantages in a high rate system because it provides twice the data rate without a bandwidth increase when compared with QPSK. Another advantage is that baseband circuits need only operate at half the speed required for QPSK. The disadvantages are that the signal set is approximately 4 dB less power efficient than QPSK, that more hardware complexity is required, particularly in the receiving circuits, and that AM on the signal requires a linear, and, therefore, less efficient transmitter. An alternative to a linear transmitter is to locate saturating power amplifiers at the output of each QPSK modulator prior to the power combining hybrid. However, the required termination on the fourth port of the hybrid results in a 3 dB power loss. Regardless of these difficulties, the bandwidth efficiency of this technique provides advantages for systems operating at the highest data rates.

The output of the 4 GBPS modulator was compared in phase to the carrier, and the resulting eye pattern for one of the quadrature channels, the “I” channel, is shown in Figure 14. The figure shows the eye pattern with input data modulation on both the “I” & “Q” channels, as well as with input modulation on the “I” channel only. A comparison provides a qualitative assessment of the channel crosstalk.

At present, the receiver multiple threshold latching circuits are being configured to demodulate the signal and allow bit error rate evaluation.

CONCLUSION

The experimental 2 Gbps MM wave system has demonstrated the capability of current technology to provide high quality data transmission at rates to 2 Gbps. In addition, the QASK modulator has indicated a capability of very high data rates in band limited applications.

REFERENCES

1. M. Washio, T. Katoh, E. Itaya, Experimental Study on a New 1.6 GBPS 16-Level APSK Modem, National Telecommunications Conference, (NTC), Dec. 1977.

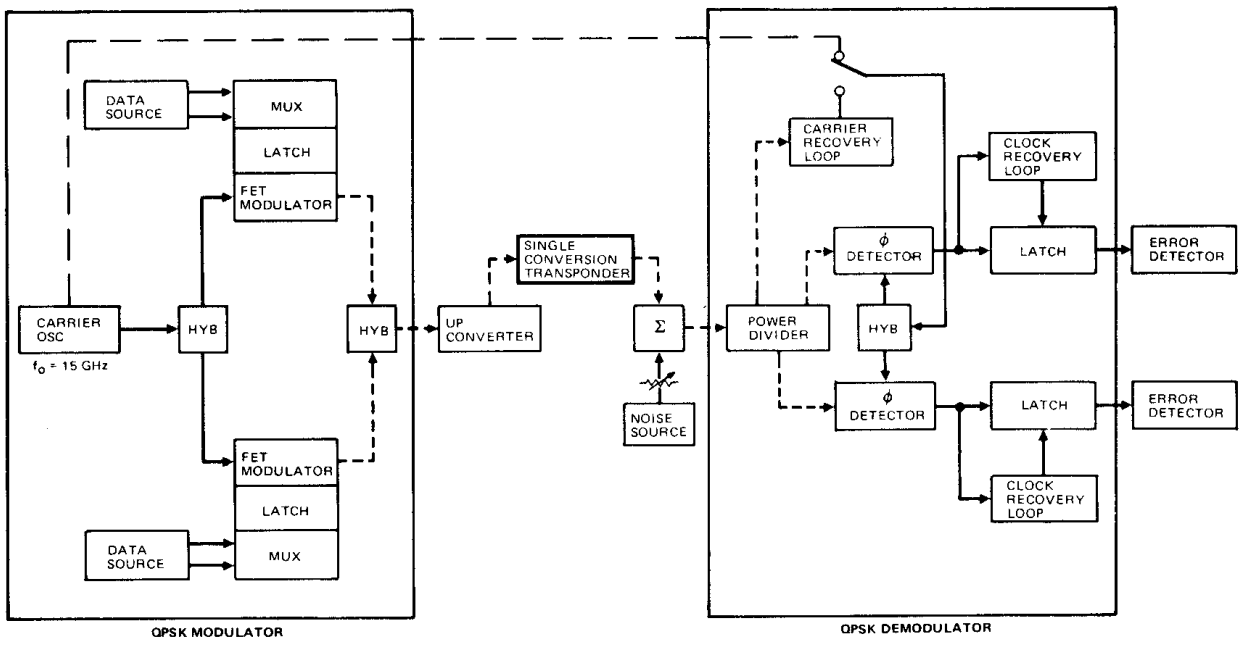

FIGURE 1. 2 Gbs MODEM AND DATA CHANNEL

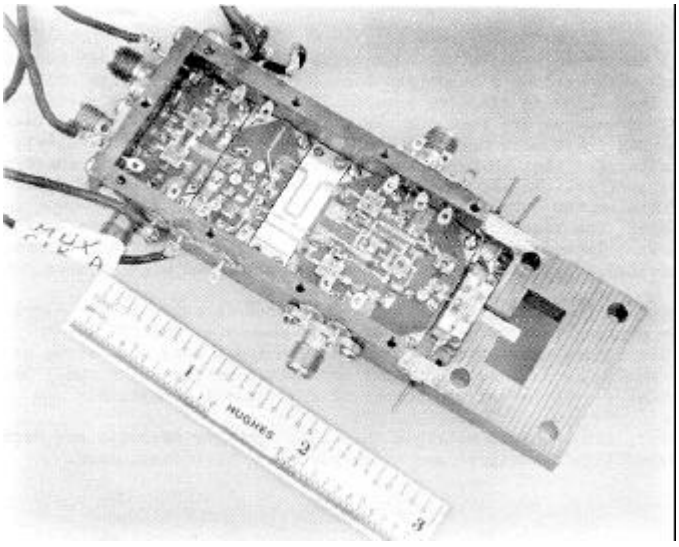

Figure 2 - Multiplexer - Latch - Modulator Assembly

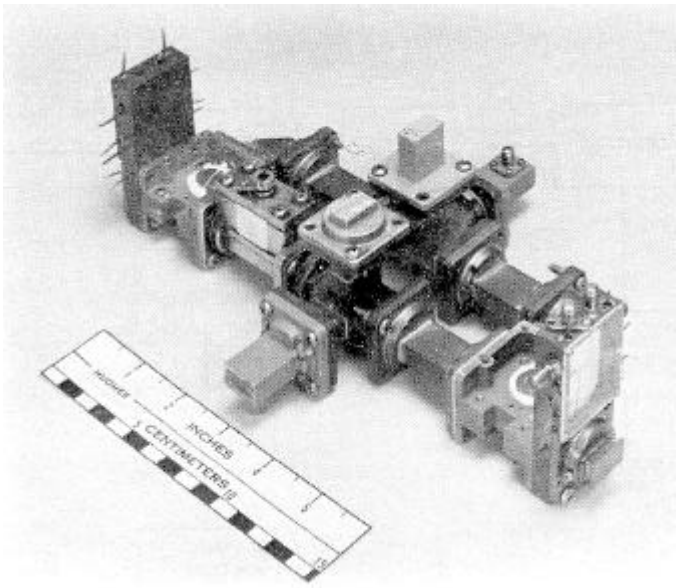

Figure 3 - QPSK Modulator

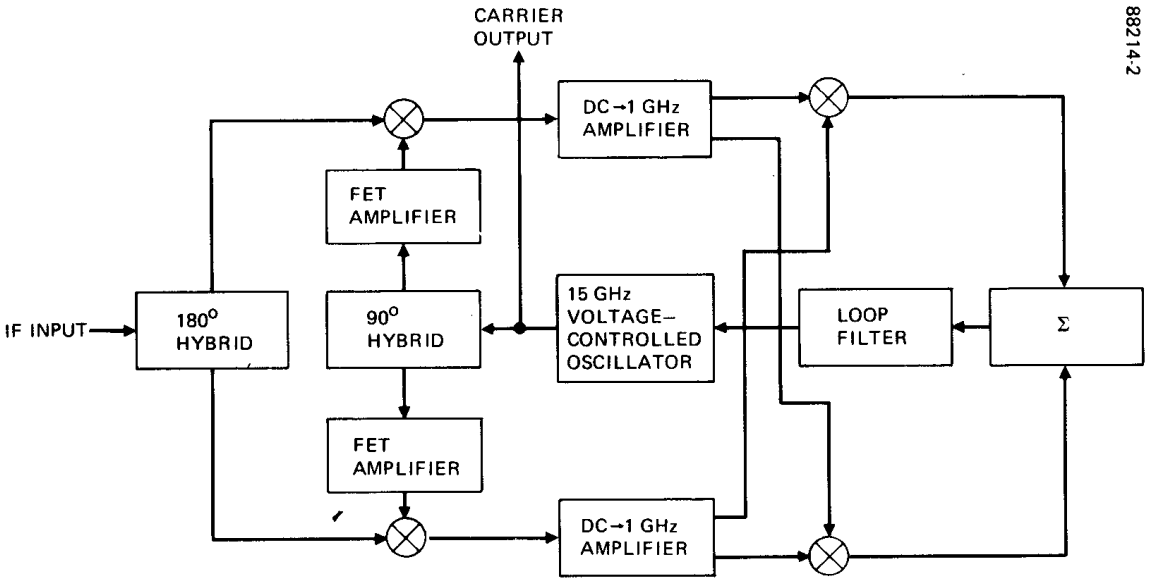

Figure 4 - 2 GB PS QPSK Carrier Recovery Loop

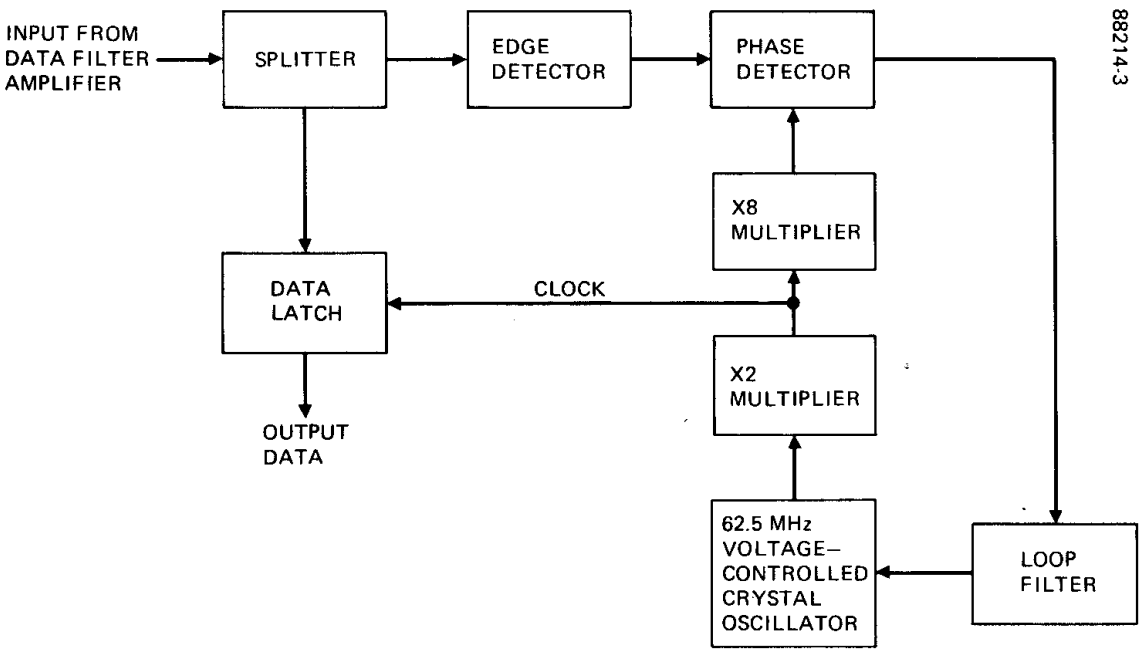

Figure 5 - 2 GB PS QPSK Clock Recovery Loop

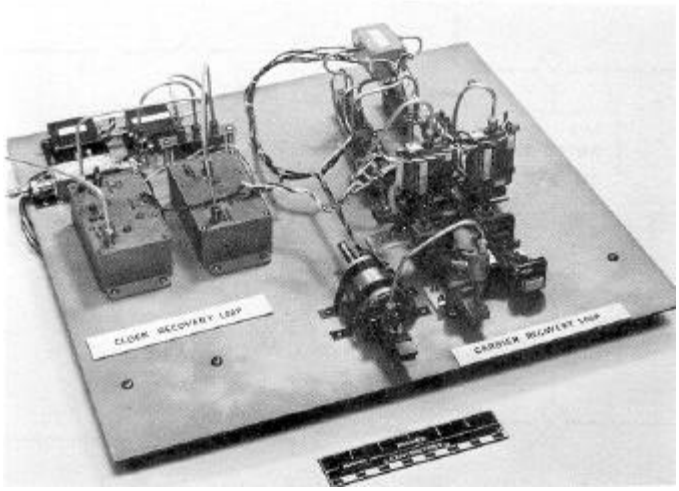

Figure 6 - Carrier and Clock Recovery Loops

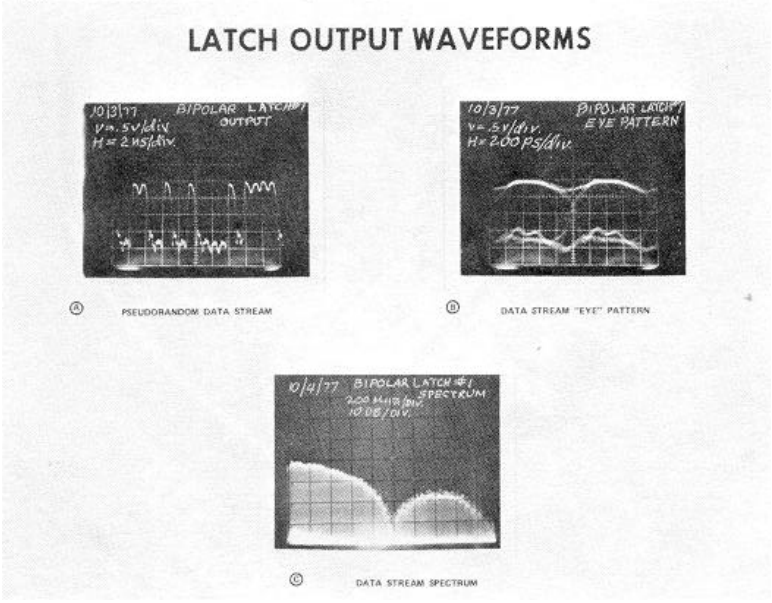

Figure 7 - Time and Frequency Domain Displays of Modular Input (Latch Output)

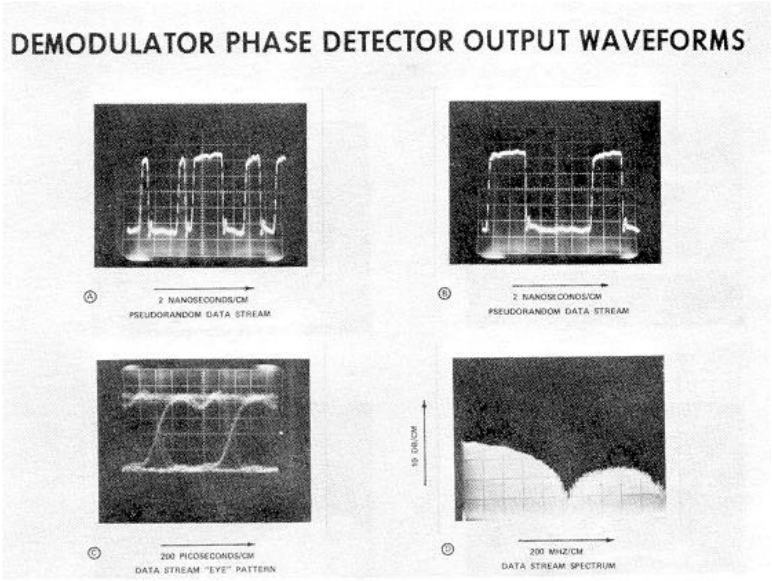

Figure 8 - Time and Frequency Domain Displays of Demodulator Output

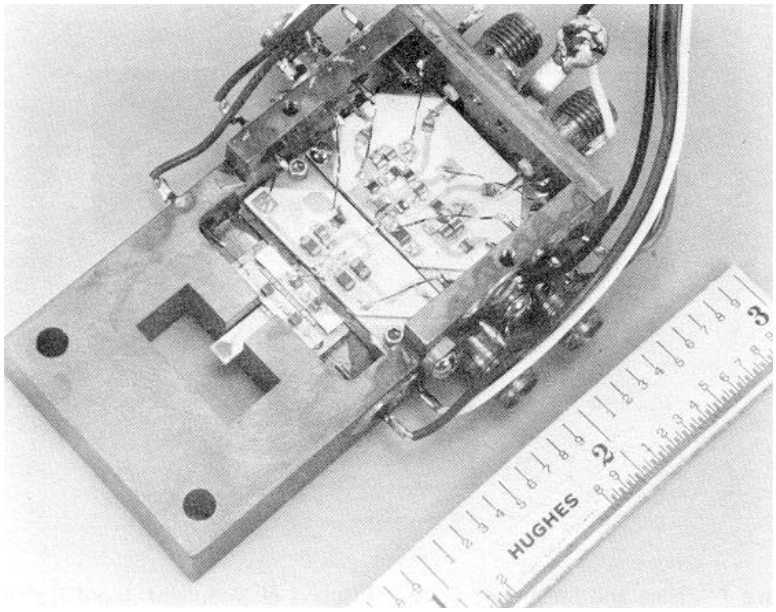

Figure 9 - G_aA_s Multiplexer - Latch - Modulator Assembly

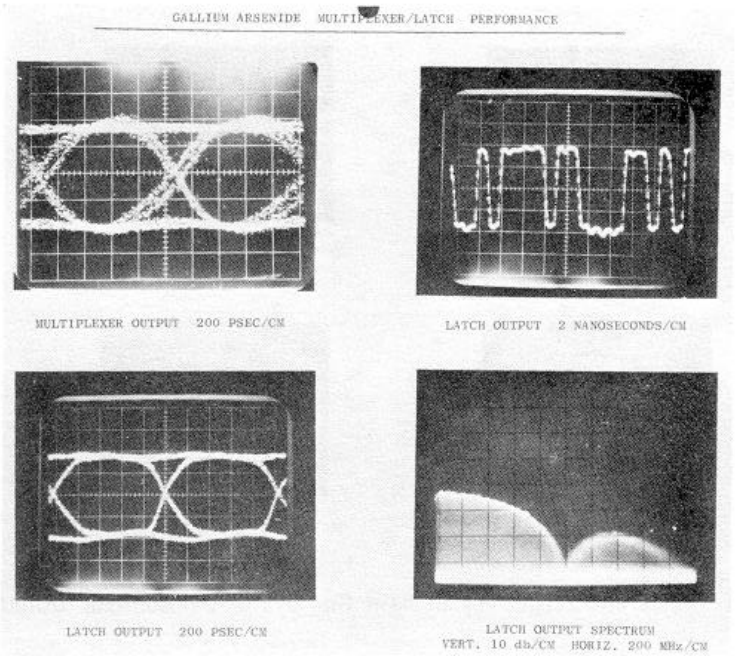

Figure 10 - Time and Frequency Domain Displays of Modulator Input (G_aA_s Latch Output)

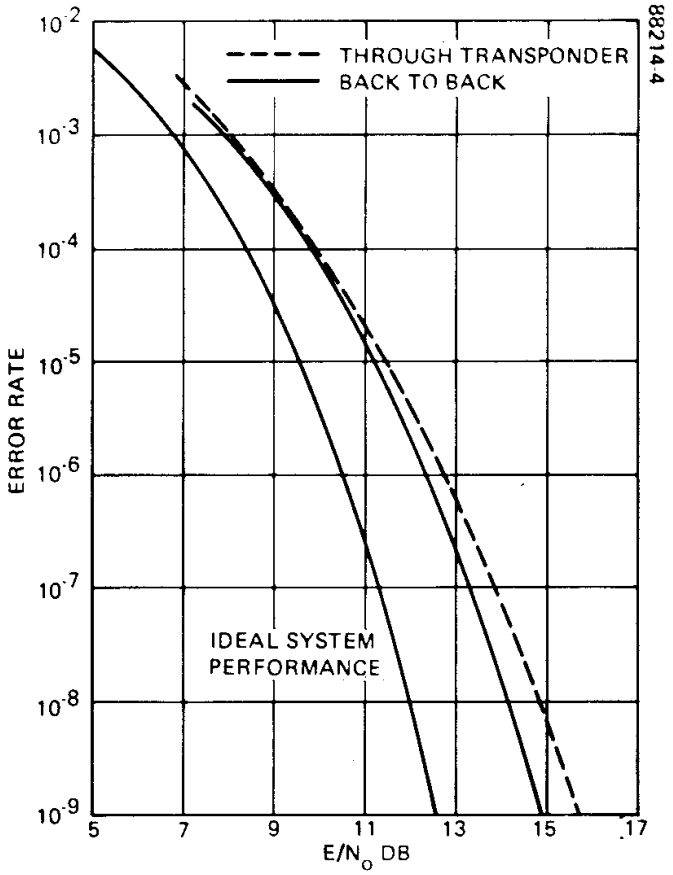

Figure 11 - 2 GB IT System Ber Performance

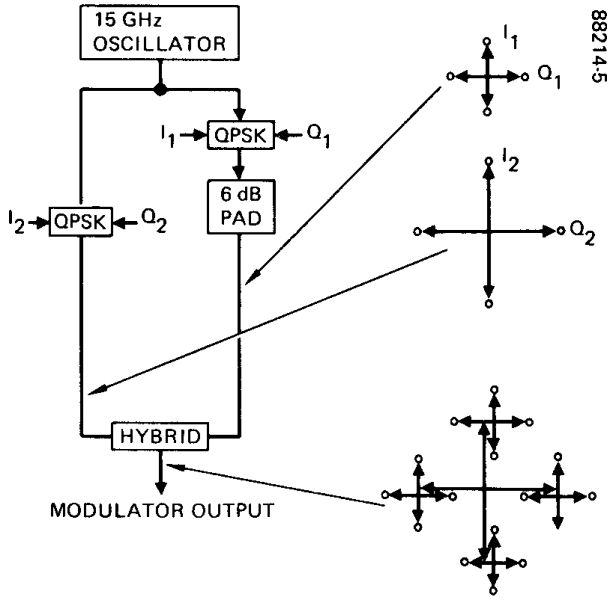

Figure 12 - 4 GB PS QASK Block Diagram and Vector Construction

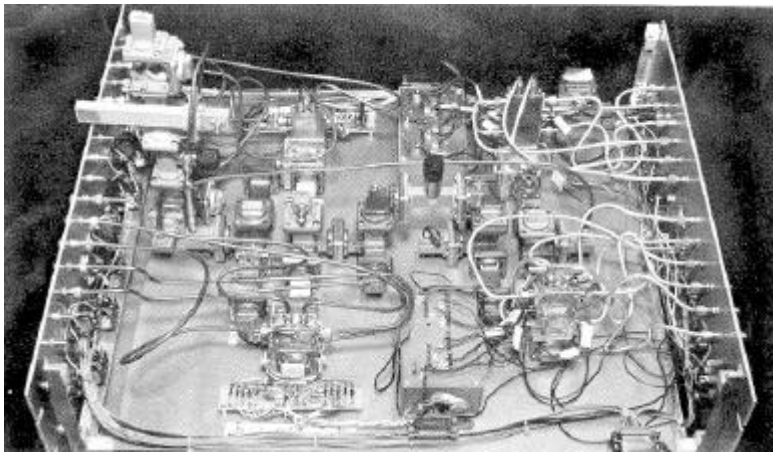

Figure 13 - QASK Modulator

4 GBPS QASK EYE PATTERNS

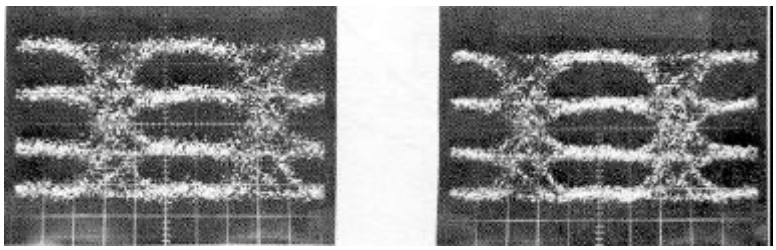

Figure 14 - G