ACQUISTION PROCESSING FOR THE TDRSS SIMULATOR

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INTRODUCTION

The TDRSS simulator forward link acqusition process requires that the epoch and frequency of the spreading code be acquired, and that the incoming carrier be phase locked. The time required for these two acquisitions must meet a specification of 20 seconds for S band and 4 seconds for K band operation. Calculations for the time required to acquire the carrier show that with the allowable sweep rates and frequency uncertainties the acquisition time specifications cannot be met with conventional sweep lock circuitry. Parallel processing is possible, but the requirements on local frequency control become difficult, and the additional circuits required make this approach unattractive.

Because of these considerations, a frequency control strategy was developed which reduces the carrier acquisition time to fractions of a second. The specified acquisition time can then be allotted almost entirely to the spreading code acquisition process. This strategy is described in detail, including an experimental verification of the technique. The technique has an additional advantage of eliminating false lock to data sidebands in the carrier loop.

ACQUISITION OVERVIEW

The acquisition strategy is based on the fact that the spreading code clock and the incoming carrier frequencies are related by a fixed ratio. Because of this, once the spreading code has been acquired its frequency can be multiplied by the fixed ratio and used to steer the carrier VCXO to the correct frequency for extremely rapid carrier acquisition.

Frequency acquisition is performed in a series of steps. In the initial step, the despreading code VCXO is phase locked to a signal which is derived from the carrier VCXO by an exact frequency ratio, and the carrier VCXO is phase locked to a stable reference at the nominal VCXO frequency. During this step, the spreading code is advanced in phase until correct epoch is detected. When epoch is detected the phase

control of the carrier VCXO (from which the despreading code clock is derived) is transferred from the stable reference to a tau-dither code tracking phase detector.

At this step in the acquisition process, the code VCXO is tracking the incoming clock frequency, and the carrier VCXO is tracking at the fixed ratio times the clock frequency. Hence, the carrier VCXO has been steered to the precise received carrier frequency.

The final step in the process is to transfer control of the carrier VCXO from the Tau-dither phase detector to the carrier loop phase detector, and to transfer control of the code VCXO directly to the Tau-dither phase detector. This complete the acquisition process.

ACQUISITION DESCRIPTION

The spreading code clock frequency and the incoming carrier frequency are related, very nearly, by fixed ratios given as follows:

$$\text{S Band } f_{code} = \frac{31}{96 \times 221} f_{carrier} \tag{1a}$$

$$\text{K Band } f_{code} = \frac{31}{96 \times 1469} f_{carrier} \tag{1b}$$

The acquisition procedure involves acquiring the code clock frequency first, as its doppler uncertainty range is much smaller (by the above ratios) than that of the carrier. Having acquired the clock, the carrier frequency is known within the accuracy that the above ratios are known. This latter is specified to be one part in $3(10^9)$, i.e., 0.01 Hz uncertainty in the code frequency (3 MHz) given a precisely known carrier. In the acquisition procedure, the uncertainty reflects in the opposite direction, i.e., from a precisely known code to a carrier frequency uncertainty. At S band, for example, the uncertainty is

$$2070 \text{ MHz} \times 3(10^{-9}) \approx 7 \text{ Hz}.$$

The following describes the frequency acquisition procedure and shows how frequency control loop bandwidths are determined by system stability and SNR specifications. The steps in the acquisition procedure are summarized in Table 1.

The frequency control circuitry for S band is illustrated in Figure 1. K band is functionally the same, differing only in carrier frequency and the ratio (1b) between code and carrier frequencies.

There are two separate VCXOs. The carrier VCXO governs IF phase while the code VCXO clocks the code generator. During frequency acquisition, the control signals for these VCXOs switch from one source to another. Each switch over marks the transition from one step in the acquisition sequence to the next.

At the start of a frequency acquisition sequence, the carrier VCXO is slaved to a stable 370 MHz source, receiving its control voltage from point A. The local code during this time is stepped in small increments searching for a time match with the incoming code. When such a match occurs, a signal appears on the line marked “despread IF,” producing a beat note of frequency $d_i - d_\ell$ at point C. Here, d_i and d_ℓ represent incoming and locally-estimated doppler shifts.

If the beat frequency were low enough, control of the carrier VCXO could be switched over to point C immediately and the loop would lock. Specification values are such, however, that pull-in would not be possible in a reasonable time: the worst-case beat frequency is too large relative to permissible loop bandwidth. Therefore, an intermediate step is employed wherein control is first switched to point B. This intermediate step makes use of the fact that absolute doppler is much less on the code than on the carrier. Because of the much lower doppler, the “beat note” or rate of slip between local and incoming codes is well within the ability of the control loop to pull in.

Figure 2 illustrates the operation of the frequency control system. It shows the propagation of phase through the circuitry under locked conditions, that is, when phase errors are small. Figure 2b is a simplified version of Figure 2a concentrating only an steps B and C.

In Figure 2b the system reduces to two loops, only one or the other of which is closed at a given time. The lower loop corresponding to acquisition step B is a tau-dither loop. Prior to lockup, the loop input is a phase ramp, i.e., a (quasi) constant frequency offset or chip slip rate due to uncompensated doppler. This slip rate equals the difference $d_i - d_\ell$ divided by the ratio between carrier and code clock rate. This latter ratio is denoted N_c in Figure 2 and is the inverse of the ratios (1a) and (1b). That is, for S band:

$$N_c = \frac{(96)(221)}{31} \tag{2}$$

The tau-dither loop is known to be able, in a noise-free environment, to lock to a slipping input sequence if the slip rate in chips/sec does not exceed the loop noise bandwidth in Hz. In symbols, lock will occur if

$$\frac{d_i - d_\ell}{N_c} < B_L \tag{3}$$

Per specification, $d_i - d_\ell$ is 1100 Hz, maximum. Thus, from Equations 2 and 3, a requirement on the tau-dither loop noise bandwidth is

$$B_L > \frac{(1100)(31)}{(96)(221)} = 1.6 \text{ Hz} \tag{4}$$

Near noise-free performance may be expected if loop SNR exceeds 15 dB, or 32. Loop SNR in turn is given by $C/2N_oB_L$. Thus,

$$\frac{C}{2N_oB_L} > 32 \text{ or } B_L < \frac{C/N_o}{64} \tag{5}$$

Minimum specified C/N_o is 33 dB Hz or 2000 Hz. Used in Equation 5:

$$B_L < 31 \text{ Hz} \tag{6}$$

To recapitulate, acquisition considerations determine a lower bound, Equation 4, for B_L, while noise dictates an upper bound, Equation 6. Any value in between 1.6 and 31 Hz will give satisfactory performance.

Locking the lower loop in Figure 2b would reduce frequency error to zero in both upper and lower loops. Actually, however, specifications allow for a slight discrepancy between incoming and local values of N_c, which as mentioned earlier are enough to allow the S band signal (upper loop) to be up to 7 Hz off. The final acquisition step is to throw the switch to position C in Figure 2b. The PLL bandwidth must be great enough to accommodate the 7 Hz frequency error that could exist, implying a loop noise bandwidth B_L of the order of 7 Hz or more.

An upper bound again is set by noise. The input C/N_o of 33.4 dB Hz will be degraded somewhat by losses in the despreader and carrier recovery loop. These losses are estimated at up to 4 dB, for an effective C/N_o of 29.4 dB Hz. To achieve 15 dB SNR, for basically noise-free acquisition behavior, single sided loop noise bandwidth should be limited to 14 Hz. Thus, a B_L between 7 and 14 Hz is indicated.

During the first two acquisition steps (A and B), it can be seen (Figure 2a) that the code VCXO is slaved to the carrier VCXO. The circuitry operates essentially as a one-oscillator system. Because of the small discrepancy which might exist in the countdown ratio (1a and b), it is necessary finally to uncouple these two VCXOs and allow the code VCXO to be tied to the actual incoming code rate. This switching is performed simultaneously with the transfer of the carrier VCXO control from B to C.

There is little if any phase error at the moment of switching as the carrier VCXO loop has just reduced this error to zero. The code VCXO loop bandwidth selection thus is not contingent on pull-in considerations but is set by residual PN jitter requirements:

$$\phi_{RMS} = \left(\frac{N_o B_L}{C}\right)^{1/2} \tag{7}$$

For example, with C/N_o = 33 dB Hz, a 10 Hz B_L would result ideally in phase jitter ϕ_{RMS} of 0.07 radian or just over 1 percent of a chip.

BREADBOARD VERIFICATION

A breadboard test was run to verify certain aspects of the proposed acquisition sequence. In particular, the test demonstrated that a loop can be aided in acquisition by a second loop operating at a lower frequency obtained by coherent division, and that such aiding can be used to prevent the loop from locking to data sidebands.

In the proposed acquisition sequence, the tau-dither tracking loop is first locked using as its clock a signal which is derived by direct multiplication from the carrier VCXO. This output is also coherently related to the frequency to which the simulator receiver is tuned. Hence, with the tau-dither loop tracking, the carrier VCXO (also the tau-dither VCXO during this phase of the sequence) is tuned to the precise frequency for locking to the received carrier (to the extent that the incoming clock and carrier are coherently related). At this time, loop control can be shifted to the carrier tracking loop phase detector and the carrier loop will track, without the need for sweeping and without the danger of locking to a data sideband. In order for this sequence to be acceptable, transfer of loop control from the low frequency code to the carrier loop must take place reliably, even in the presence of noise. The breadboard test was designed to verify that reliable transfer does take place.

A block diagram illustrating the sequence just described is shown in Figure 3 and the test simulation in Figure 4. In the simulation, a direct frequency synthesizer provides 500 MHz and 1 MHz outputs, which play the roles of the incoming carrier and the coherently related code clock. Noise is added to both of these outputs. A 1 MHz VCXO simulates the system VCXO, and is multiplied in a direct frequency synthesizer to 500 MHz for phase detection with the incoming 500 MHz “received carrier.” The two 1 MHz signals are compared in a second phase detector which plays the role of the tau-dither loop. Loop parameters have been selected so that both loops are second order, with B_L = 100 Hz, and damping of 0.7.

A schematic of the loop filter is shown in Figure 5. The difference in gain between the loops is made up by the difference in input resistor values. Note that control is transferred

at the input to the loop filter and that the filter capacitor is not disturbed. The 1 MHz VCXO rest frequencies are set to be 20 Hz apart, so that the initial frequency difference at 500 MHz is 10 KHz. The noise levels were set to provide a C/KT of 35 dB Hz, for a signal to noise ratio of 15 dB in the loop bandwidth. Spectrum analyzer photographs of the input 1 and 500 MHz signals are shown in Figure 6. The problem, then, is to lock the 500 MHz loop.

When the loop was closed around the 500 MHz phase detector at this time, there was no acquisition, which is to be expected because of the 10 KHz initial offset. However, when the 1 MHz loop was also closed, it snapped in immediately. The very rapid acquisition of this loop is to be expected, since the initial frequency offset was less than the loop bandwidth. We are now simulating tracking through the tau-dither loop. At this time, the frequency offset of the 500 MHz loop is reduced to zero because of the coherent relationship between the 1 MHz and 500 MHz signals. When the 1 MHz loop was now opened, returning control to the 500 MHz loop, the 500 MHz loop continued to track. The experiment was repeated with the frequency synthesizer mistuned by 10 Hz to provide a 500 MHz input with an imperfect coherency ratio, and simulate imperfect coherence between received carrier and code clock frequencies. The results were the same. The 1 MHz loop acquired immediately and reduced the initial offset in the 500 MHz loop, not to zero, but to 10 Hz. Again, the 500 MHz loop acquired immediately and tracked when control was retuned to it.

Transfer of control from the 1 MHz to the 500 MHz loop was found to be noncritical, with a precision switch not required. In fact, with both loops closed, the 1 MHz loop provided almost all of the steering and it was not even necessary to open the 500 MHz loop. This is because of the nonlinear phase detector characteristic. Consider a small phase offset, θ_e, between the two 1 MHz oscillators. This will result in an offset of 500 θ_e as detected by the 500 MHz phase detector. So long as 500 θ_e is small compared to a radian, both phase detectors will be operating in their linear range and will have equal effect if both are controlling a loop. However, as θ_e becomes larger, the 500 MHz phase detector will saturate and its loop gain will be reduced. This is not true, however, for the 1 MHz phase detector, which is still operating linearly and which is coupled into the high gain input of the loop filter. This is illustrated in Figure 7 which shows equivalent phase detector characteristics for a 500 MHz phase detector with a low gain loop filter and for a 1 MHz phase detector with a high gain loop filter. Note that in the linear region, both are identical.

A breadboard test was also run to demonstrate that with the proposed acquisition sequence there is no danger of acquiring to a data sideband on the incoming carrier. The simulated incoming carrier signal at 500 MHz was phase modulated at a 5 KHz rate to produce sidebands 10 dB larger than the carrier and at a 5 KHz separation. A spectrum

analyzer photograph of this input is shown in Figure 6. When this input was swept for acquisition the 500 MHz loop would acquire and track on a sideband. However, when the 1 MHz loop was used to aid acquisition, the loop was steered to and would acquire and track the reduced amplitude carrier immediately.

CONCLUSION

The difficult acquisition time requirements on the TDRSS simulator have resulted in a design which makes use of the coherency relationship between spreading code and carrier frequencies to aid in carrier acquisition. This acquisition aid technique has been verified by a breadboard test which demonstrated that there is no difficulty in transferring VCXO control from the code to the carrier loop, and that with such aiding, false lock to data sidebands will not occur.

TABLE 1. ACQUISITION STEPS

Step	Description	Carrier VCXO Control	Acquisition Circuit	Code, Tau Dither Loop	Carrier Loop
A_1	Just prior to begin of acquisition	Phase locked to stable reference	Searching: clocked by carrier VCXO via phase locked frequency multiplier	Waiting: clocked by carrier VCXO via phase locked frequency multiplier	Waiting
A_2	Forward code search	Phase locked to stable reference	Search for forward code apoch	Waiting: clocked by carrier VCXO via phase locked frequency multiplier	Waiting
B_1	Forward code epoch detect	Switch to (B): now locked to forward code tau dither loop	Forward code epoch detect	Error signal output to (B): locked with carrier VCXO	Frequency error reduced to 7 Hz (S band), not locked
B_2	Verify	Switch to (B): now locked to forward code tau dither loop	Verify true detection and tracking	Error signal output to (B): locked with carrier VCXO	Frequency error reduced to 7 Hz (S band), not locked

C_1	Acquire carrier	Switch to (C): now locked to carrier	Finished	Clocked by incoming carrier via frequency multiplier 0.01 Hz error	Locked to incoming carrier
C_2	Switch code loop to code clock	Switch to (C): now locked to carrier	Finished	Switch 2 to (C) phase locked to acquired code frequency	Locked to incoming carrier

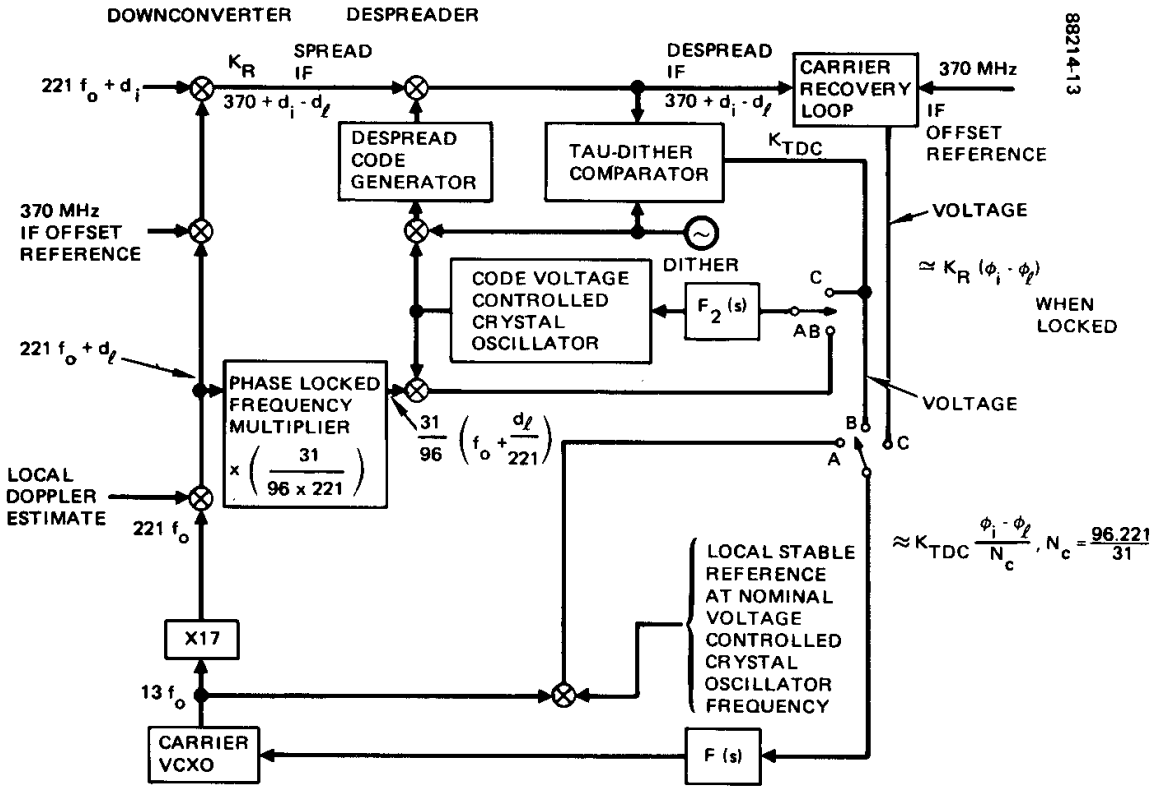

Figure 1 - Frequency Control Circuits

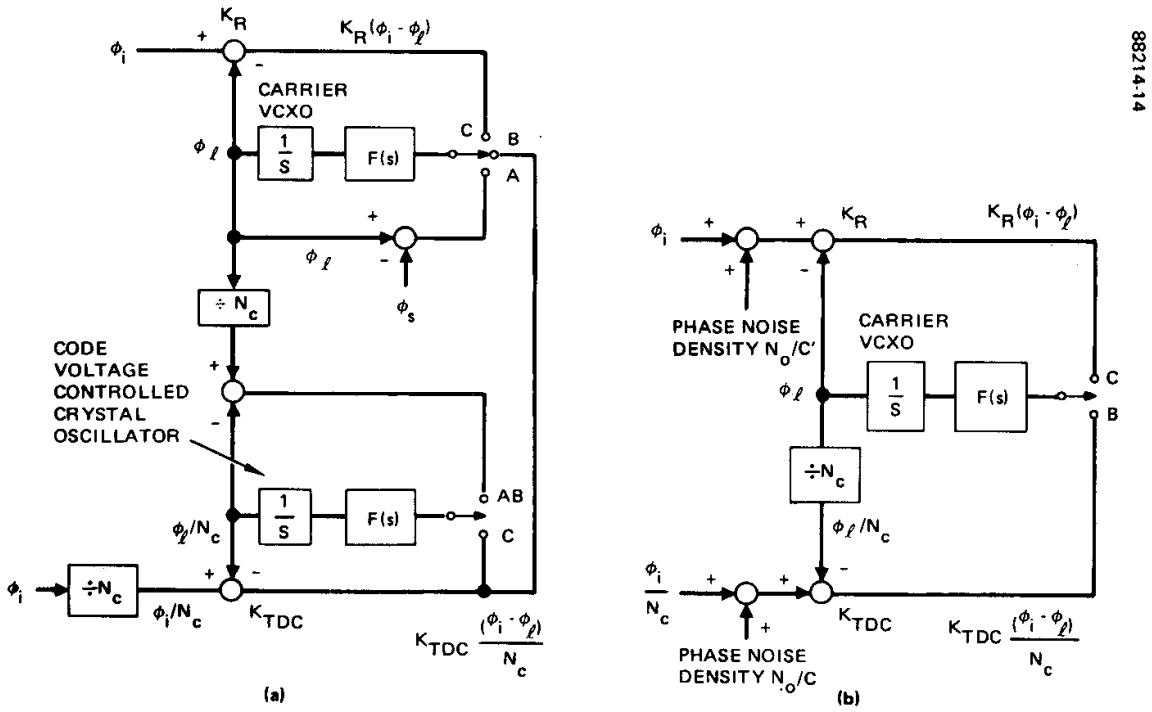

Figure 2 - Frequency Control Circuitry Phase Propagation

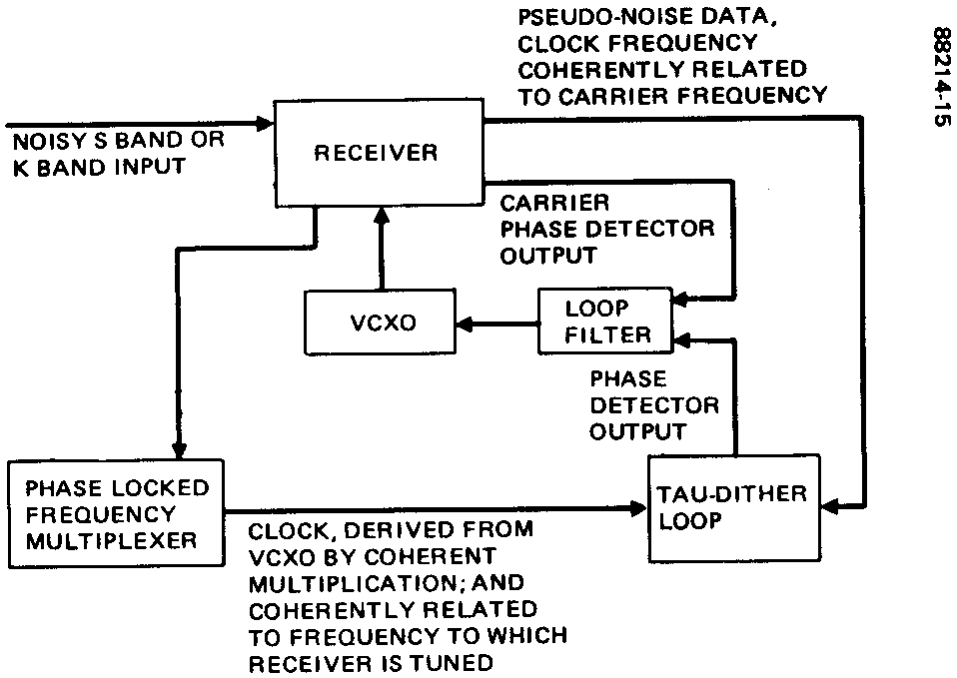

Figure 3 - Acquisition Sequence Diagram

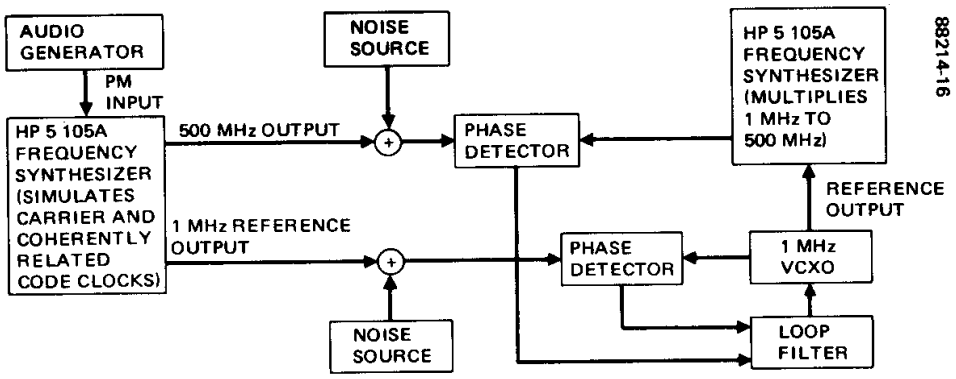

Figure 4 - Acquisition Test Block Diagram

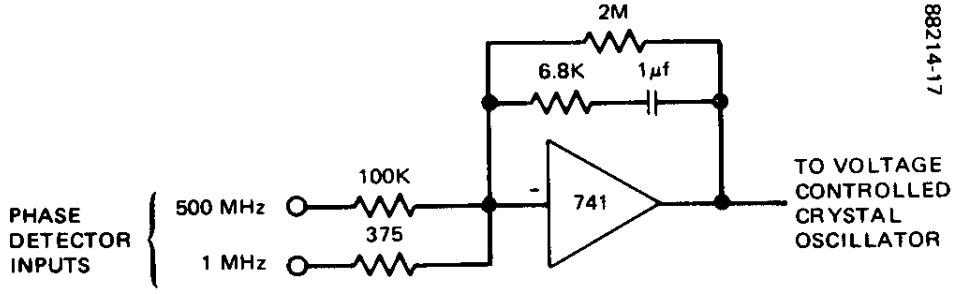

Figure 5 - Acquisition Test Loop Filter

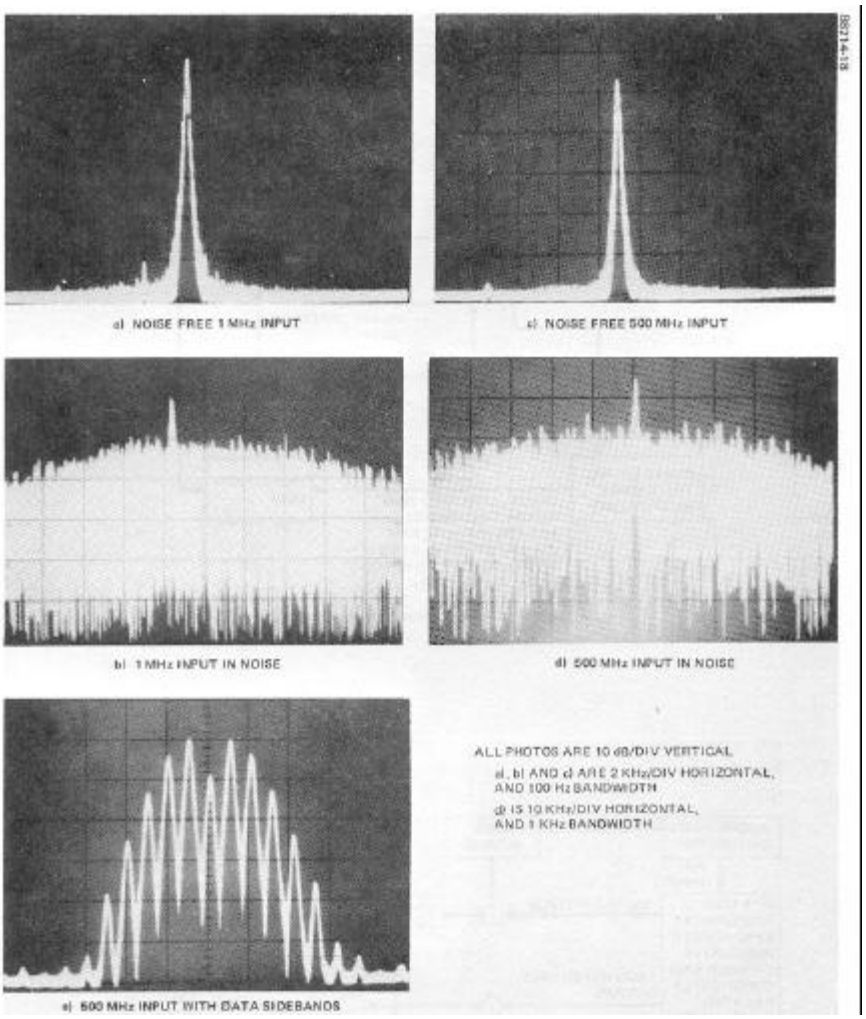

Figure 6 - Analyzer Photographs of Incoming Signals

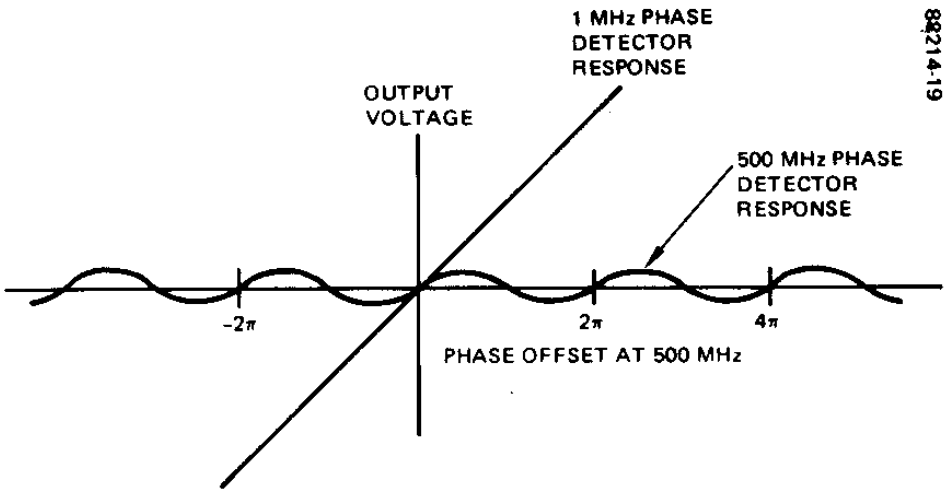

Figure 7 - Phase Detector Responses