

# **A CLASS OF PROGRAMMABLE SATELLITE RECEIVERS**

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## **ABSTRACT**

The currently developed theory of optimal demodulation and synchronization systems for digital data has been applied to the design of a class of programmable satellite receivers. The primary purpose is to provide flexibility in application through digital control of the important functions of the receiver. This permits the acquisition and demodulation of medium to very low data rates in widely varying communications environments and over a broad range of modulation schemes. The receiver peripherals are controlled by a digital processor which can accept external commands to reconfigure to any of a preprogrammed set of algorithms.

## **INTRODUCTION**

The first application of the programmable concept is in the high reliability, low-power NASA Standard Command Detector Unit (CDU). Designed to meet the rigid performance requirements of various outer planet communication links, this CDU retains its mission adaptability in spite of structural and functional economy. With a command-selectable range of nine data rates (8-2000 bps) in a binary phaseshift keyed (BPSK) modulation format or as nonreturn to zero (NRZ) baseband data, and an easily modified memory-resident set of demodulation algorithms, this CDU achieves its performance margin using the power and weight saving approach of custom complementary metal oxide semiconductor (CMOS) large-scale integration (LSI).

A second programmable receiver has been designed and breadboarded for the Jupiter Orbiter Probe (JOP) or Galileo mission. This receiver uses an acquisition algorithm and demodulation scheme tailored for the Jovian environment. Its implementation permits its use in a wide range of applications. It is commendable to permit reconfiguration during separate mission phases as well as programmable to permit its use for varying demodulation techniques, data rates, acquisition algorithms, etc., to meet the demands of the communication medium expected for each specific mission. The receiver is

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channelized to permit command selection of any of several carrier frequencies at channel separations determined by the particular mission. Its spare processing capacity may be utilized in radio science experiments with the results presented to the telemetry interface as required.

Both of these applications are discussed in this paper as well as general capabilities and extensions which are envisioned.

## DIGITAL COMMAND DETECTOR

The NASA Standard CDU is a coherent demodulator for BPSK message spectra or NRZ data. The CDU combines hardware simplicity with a flexible approach for implementing specific data demodulation algorithms. It is programmed to operate on BPSK signals where the subcarrier frequency is 16 kHz. Its programming allows nine selectable data rates to be demodulated. For the Tracking and Data Relay Satellite System (TDRSS) application where NRZ data is to be detected, a 16 kHz chopping signal is provided to the transponder to modulate the data. These functions, as well as other ancillary functions performed by the CDU, are listed in Table 1.

**Table 1. CDU Functional Capabilities**

Design compatible with the NASA Standard Near Earth or Deep Space Transponders and the NASA Standard TDRSS Transponder.	Operates at 4 different data rates in the NRZ mode ranging from 125 to 1000 bps.
Operates in either of two modes: PSK or NRZ.	Detects whether or not the CDU is synchronized or in lock with the received command signal.
In the PSK mode (Standard or TDRSS) the CDU demodulates the 16 kHz subcarrier frequency and detects the command data bits.	Provides detected command data, bit timing, and lock status to redundant command decoders.
In the NRZ mode (TDRSS only) the CDU provides a 16 kHz signal for modulating the NRZ data.	Provides signals defining the operational condition of the CDU to an external unit for insertion into the spacecraft down link telemetry data.
Operates at 9 externally programmable data rates in the NRZ mode ranging from 7.8125 to 2000 bps.	Provides direct access test point signals to monitor the CDU performance in the subsystem and spacecraft test configuration.

The functional architecture of the CDU is shown in the block diagram of Figure 1. The unit employs a universal design and is included as an integral part of three NASA Standard Transponder designs: the NASA Standard Near Earth, the Deep Space, and the TDRSS User Transponders.

Functionally, the CDU consists of a data-coherent automatic gain control (AGC) system, a sample-and-hold (S/H) circuit, an analog-to-digital converter (ADC), a second-order data-

aided subcarrier tracking loop, a data-transition tracking symbol synchronization loop, and a lock detector. Structurally, the CDU consists of the signal-conditioning assemblies (AGC, S/H, ADC), read-only memory (ROM), random-access memory (RAM), and a digital processor (instruction decoder, program sequencer, data bus and interfaces, arithmetic logic units, timing oscillator, I/O buffers, etc.) employing a custom LSI approach and metal-gate CMOS technology. Using custom LSI, 30 circuit boards with 390 small scale and medium scale integration functions were reduced to a single board as shown in Figure 2. Appropriate modifications to the signal conditioning circuitry would enable this digital processor to demodulate various modulation formats, (such as differentially encoded PSK (DEPSK), quadriphase PSK (QPSK), and frequency shift keying (FSK)), and data rates.

The data-coherent AGC system consists of logarithmic-linear digitally controlled attenuation with a dynamic range in excess of 40 dB. The AGC loop performance (i. e. , noise jitter, settling time, etc. is determined by the AGC loop algorithm and coefficients stored in ROM, allowing greater ease in matching mission-particular AGC requirements and performance.

Upon receipt of the appropriate command from the digital processor, the S/H circuit freezes the analog input to the eight-bit ADC and maintains the input constant over ADC conversion time.

Because of the stability of digital circuitry and the ease with which it can be integrated, the foremost design goal was to digitize the signal as soon in the processing as possible. This goal led to the selection of a sampled data approach wherein the demodulation was effected through coherent sampling.<sup>1</sup> This approach removes the subcarrier, translating the input sequences to baseband. By sampling in quadrature, one sequence represents the inphase, or data sequence, and the other the quadrature, or error sequence. From the data sequence, bit synchronization and data detection are performed, while the error sequence is used to maintain subcarrier synchronism.

In order to obtain the best performance, a data-aided subcarrier tracking loop was selected. Because Doppler offsets are expected, the loop is a perfect second-order loop. Thus, the subcarrier loop can be designed considering the expected worst-case input signal-to-noise ratio (SNR) and Doppler offset. The superior performance achievable using the data-aided approach, compared to previous techniques dictated its selection. The many advantages of the data-aided configuration have been well documented<sup>2,3</sup>. In the CDU the subcarrier tracking loop utilizes a quasi-continuous variable-phase correction updated at the end of each detected bit. This limits the amount of Doppler which can be tracked; however, for the expected offsets, no appreciable bit error rate degradation is expected. Improved Doppler tracking performance can be realized by correcting the subcarrier phase in

fractional bit intervals. However, due to the additional complexity and the small Doppler offsets expected, this approach was rejected. In contrast to the conventional data-aided receiver implementation (shown in Figure 3) which requires mixers, filters and ADCs in both inphase (I) and quadrature (Q) channels, the CDU implementation takes advantage of the digital implementation by effecting both the inphase and quadrature synchronization channels with appropriate dedicated sample accumulators within the digital processor (Figure 4). The requirement for data-rate dependent digital filtering in each (I and Q) leg is eliminated by maintaining a constant sample rate over all data rates, thus providing maximum design economy without compromising performance. The CDU utilizes a perfect integrator and a quasi-continuous variable-phase correction to implement a second-order subcarrier tracking loop. The demodulator algorithm is stored in ROM, with ROM-resident loop coefficients selected to minimize steady-state phase jitter while meeting all NASA specifications on acquisition time. The subcarrier loop resolution is 1/64 of a cycle with a maximum allowable single phase correction of 45 degrees.

Proper detection of the demodulated data stream requires the use of some form of matched filter. Implementation of this matched filter, in turn, requires the generation of accurate estimates of the end-of-bit epoch. It is the function of the bit synchronization loop to generate these end-of-bit estimates. The bit sync configuration, a digital data-transition tracking loop (DTTL), consists of two parallel branches which are strobed by a timing generator driven by an error signal formed from the product of the branch outputs. The inphase branch monitors the polarity of the actual transitions of the input data and the midphase branch obtains a measure of the lack of synchronization. The performance of this loop has been the subject of extensive analysis,<sup>4,5,6</sup> at NASA's Jet Propulsion Laboratory.

The DTTL symbol synchronizer, implemented as indicated in Figure 4, derives its estimates of the proper end-of-bit epoch through the polarity of  $I_k$  times the quantity  $M_k$  which is a measure of the symbol timing error. The CDU design takes advantage of coherence between the subcarrier and the data so that the bit sync loop resolution need only be accurate to within a subcarrier cycle to provide effective bit sync resolution of 1/64 of a subcarrier cycle. Thus, at the lowest data rate (8 bps), the effective bit sync resolution is approximately 8 millionths of a data bit. The maximum allowable phase correction is 0.25 of a bit interval with a correction made after eight data transitions.

The lock detection algorithm is also ROM-resident, with coefficients chosen to exceed the NASA specifications for probability of acquisition and deacquisition. Again, all coefficients and the algorithm itself are completely ROM-resident, providing complete flexibility in optimally tailoring the demodulator to meet mission-specific performance requirements.

The CDU algorithms and implementation were designed and developed through the use of state space simulation techniques. Such support software allows significant reductions in the time required for both hardware and software development. With the aid of simulation, the design iterations quickly converge to quantitatively present the available and significant system performance tradeoffs. This system software package includes a CDU assembler to facilitate the ROM programming of algorithms and coefficients by providing the interface between a high-level processor language and the generation of the required bit patterns. Also included is a simulator which accepts the ROM program and verifies operational integrity at the hardware level.

Test results indicate the CDU is operating approximately 0.5 to 1.0 dB from theoretical BPSK performance at all nine data rates. The secondary power consumption is approximately 2.1 watts. A set of CDU test data is shown in Figure 5 at a data rate,  $R$ , of 2000 bps.

## **DIGITAL RECEIVER**

The digital receiver design for the JOP mission was highly influenced by stringent performance requirements of the communications medium and mission constraints. The large Doppler offsets expected during initial acquisition led to the development of a novel acquisition technique. This technique, the Hilbert Acquisition Aid (HAA) has been demonstrated to provide a frequency acquisition characteristic which permits rapid acquisition ( $\approx 5$  seconds) for low signal-to-noise densities ( $S/N \geq 24$  dB-Hz) and frequency uncertainties on the order of  $\pm 80$  kHz. For the demodulation technique, the implementation losses have been shown to be on the order of 0.5 dB from theoretical bit error probability performance.

The receiver functional block diagram is shown in Figure 6. The current design uses a carrier frequency of 1 GHz with two down conversions prior to the baseband demodulation. The hardware in the RF portion of the receiver is derived from NASA Standard Transponders and the TDRSS User Transponder. The baseband processor is derived from the NASA Standard CDU and provides the receiver with its software control capability and programmable demodulation and acquisition capabilities. As shown in Figure 6, the baseband processor accepts I and Q channel inputs from the RF portion of the receiver and controls the frequency channel selection, receiver gain through the AGC, and frequency and phase of the baseband inputs through the numerically-controlled oscillator (NCO) output. All external interfaces are controlled by the baseband processor with telemetry outputs and command inputs provided as well as lock indication, demodulated data, and clock. Other outputs and inputs can be accommodated as determined in the definition phase of a specific mission.

The circuitry in the receiver will be capable of withstanding radiation doses in excess of  $3 \times 10^5$  rad (Si) with the RF circuitry comprised entirely of bipolar circuitry. The baseband processor will be implemented in hardened CMOS as well as bipolar circuits. The custom LSI circuits used in the baseband processor will be constructed with a hardened, low-power, high-speed silicon-gate CMOS process with proven capability.

This receiver is intended to be a highly flexible, channelized design which can acquire and demodulate medium to very low data rates in widely varying communications environments and over a broad range of modulation schemes. This design goal is realized through software control of the important functions of the receiver. Thus, through programs designed specifically for each application, acquisition and demodulation strategies can be tailored for optimal performance. Modulation formats for which algorithms can be developed include: phase shift keyed (PSK), differentially encoded PSK (DEPSK), differentially encoded/detected PSK, (DEDPSK), quadriphase PSK (QPSK), and staggered QPSK (SQPSK). For the JOP mission PSK and DEDPSK are under consideration.

The foremost design goal was to digitize the signal as soon in the processing as possible. A secondary goal was to develop an acquisition technique compatible with low SNRs and large frequency offsets. For demodulation the ADC could operate at the IF using coherent sampling. However, for ease of implementation and performance the acquisition strategy required a baseband I-Q channel pair. This requirement, coupled with a need to minimize circuitry, led to the decision to demodulate the received signal at baseband. This approach does not compromise the receiver flexibility in any way; however, additional analog circuitry is required.

The basic requirements for the JOP mission are given in Table 2. Significant parameters are the minimum  $ST/N_0$  of 4.5 dB and the acquisition probability of 0.995 for a total frequency uncertainty of 160 kHz. Thus, while sufficient attention must be devoted to demodulation of the signal within 1 dB of theory, a much more difficult problem is reliable frequency acquisition. A new acquisition strategy, the HAA, has been developed to meet these requirements.

The baseband processor is shown in Figure 7. This processor makes use of the custom microprocessor chips designed for the NASA Standard CDU. The CDU, minus its analog interfaces, has been used as the digital processor in this design with the primary external interfaces compromising one of its functions. While the software algorithms must respond to the command inputs, simultaneous acquisition and demodulation are achieved through separate algorithms controlling carrier acquisition and tracking, data detection, AGC adjustments, and input channel selection. The input frequency offset and phase are controlled through the NCO interface. Acquisition and tracking inputs are obtained through

**Table 2. Receiver Performance Parameters**

<b>Signal Characteristics</b>	
• Frequency	999-1009 MHz
• Maximum frequency uncertainty	$\pm 80$ kHz
• Maximum Doppler rate	$\pm 50$ Hz/sec
• Minimum signal	-146 dBm
• Maximum signal	-116 dBm
• Minimum $ST/N_o$	4.5 dB
• Modulation	DPSK
• Data rates (commendable)	125, 250, 500, 1000 bps
<b>Acquisition Requirements</b>	
• Acquisition probability (50 sec)	0.995
• False acquisition probability (50 sec)	$1 \times 10^{-4}$
<b>Tracking Requirements</b>	
• Bit error probability	$< 1$ dB from theory $0.1 < PE < 1 \times 10^{-5}$
<b>Radio Science Requirements</b>	
• Signal power measurement	$< 0.1$ dB resolution
• Frequency measurement variance	$< 1$ Hz rms (1 sec)

two separate I-Q channel pairs. One pair is wideband for acquisition of large frequency uncertainties while the other is maintained at a bandwidth greater than or equal to three times the selected data rate.

Digitization of these signals is performed as close to the final mixers as is practical to avoid the problems of drift and dc offsets associated with the analog circuits.

The microprocessor used in the digital subsystem is structured as shown in Figure 8. In order to optimize data handling operations, the system is configured using a 10-bit address bus, a 16-bit instruction bus, and a 16-bit data bus. By keeping these three buses separate, the system is capable of performing data fetches or executing instructions in a single system clock cycle.

The estimated physical characteristics of the design are shown in Table 3. Through the use of LSI and low power RF designs, the size, power, and weight have been minimized. With a power consumption of 7.3 watts, a weight of 2050 grams, and volume of 2100 cubic

centimeters, this receiver represents a refined state-of-the-art digital receiver with a flexibility to meet the requirements of widely varied missions through software changes.

**Table 3. Estimated Receiver Physical Characteristics**

	Size (cm)	Volume (cm <sup>3</sup> )	Weight (gm)	Power (W)
Baseband	14 x 20 x 3	840	250	3.0
Power Converter	14 x 6 x 1.5	126	600	1.8
RF	14 x 20 x 3	840	1200	2.5
Spare Volume	14 x 14 x 1.5	294		
JOP Receiver	14 x 20 x 7.5	2100	2050	7.3

The demodulation algorithm was selected to maximize the bit error probability performance of the receiver at the expense of processing complexity. Because the communication environment for the JOP mission is difficult and the transmitter power is constrained, the margin from theoretical performance allocated to the receiver must be kept at a minimum. The processing power of the circuits developed for the NASA Standard CDU is more than adequate for this task. Coupled with an ADC, an NCO, and preaccumulators, the processor can perform the demodulation of signals with a minimum of degradation from theoretical performance.

The JOP receiver uses a baseband sampling scheme to implement a second-order, suppressed-carrier, data-aided loop. The carrier tracking algorithm is shown schematically in Figure 9. The inphase samples ( $I_i$ ) and the quadrature samples ( $Q_i$ ) are summed in integrate-and-dump accumulators. With nominally 160 samples per bit interval and 8-bit quantization in the ADC, these accumulators can be considered to approximate perfect reset integrators. The outputs of these accumulators are applied to an arctangent mapping ROM with a resolution of  $2\pi/1024$  radians. This estimate of the phase error is applied to the loop filter which drives the phase of an NCO to achieve synchronization. The ADC sample instants are determined by the ultrastable oscillator (USO) frequency and phase, while the NCO translates the input frequency and shifts the input phase to effect tracking.

This algorithm offers the advantage of coherent tracking performance when the channel phase characteristic is approximately constant over a bit interval. Where the channel phase characteristic is approximately constant over two bit intervals the differential detection

scheme shown in the figure can be shown to be the optimum a posteriori receiver of differentially encoded data.<sup>3</sup>

The receiver was tested using the algorithms illustrated in Figure 9. Because the carrier tracking was essentially coherent, the results approached very closely the theoretical performance for differentially encoded coherent PSK (DEPSK). The data taken is shown in Figure 10. The data pattern transmitted was a 15 bit maximal length code.

The development of the HAA was necessitated by what were considered undesirable properties of the sequential-detection-based acquisition strategies. Whereas sequential detection requires a somewhat complex set of thresholds and dismiss times, the HAA requires only a loop noise-bandwidth setting established by the particular design point selected by the mission. The HAA has a gradual degradation in acquisition time as the input SNR drops below the design point and acquires dramatically faster as the SNR is improved. A functional block diagram of the HAA is shown in Figure 11.

A noiseless analysis of this scheme was undertaken to determine the effects of dc offsets, quadrature error, amplitude imbalance, and limiters in the cross-terms.

For the case where the SGN operators were ignored (i.e., no limiting) the resulting control signal [  $\langle H(t) \rangle$  ] is

$$\langle H(t) \rangle = 2 D_i D_q - A_i A_q \sin (\psi + \beta) \quad (1)$$

where

$$\begin{aligned} D_i \text{ and } D_q &= \text{I and Q channel dc offsets} \\ A_i \text{ and } A_q &= \text{I and Q channel amplitudes} \\ \beta &= \text{quadrature error} \\ \psi &= \alpha_i(\omega) - \alpha_q(\omega) \end{aligned}$$

In arriving at this result it was assumed that the control signal was averaged for a period of time which is large with respect to the offset frequency,  $(\Delta\omega)^{-1}$ . As seen in (1), the dc offsets ( $D_i$  and  $D_q$ ) are not affected by data modulation or reference phase and must be controlled to avoid significant error. However, if an adequate transition density exists in the data modulation, or if there are periodic software controlled phase inversions, capacitive coupling is permitted, allowing the offsets to be reduced to only two elements in the actual implementation - one buffer amplifier and an ADC. Again, from (1) it is seen that quadrature errors ( $\beta$ ), if not controlled adequately, can produce significant degradation. With reasonable care  $\beta$  can be reduced to negligible proportions and then only the I-Q phase difference becomes important.

An all-pass network has been designed which permits the I-Q phase difference ( $\psi$ ) to be controlled over a wide range of frequencies with a characteristic which approximates a Hilbert transform from which this technique derives its name. A typical characteristic of  $\psi(\omega)$  is shown in Figure 12. The purpose of the HAA is to resolve the frequency within a sufficiently narrow band in order that a coherent phase-tracking algorithm can acquire it. Thus, a characteristic as shown in Figure 13 would be used for loop bandwidths ( $B_L$ ) on the order of 10 Hz.

Because the receiver design is primarily digital with the maximum use of software control, the use of limiters permits the digitization of the I and Q acquisition channels prior to the multiplication with only sign inversions for multipliers. Thus the requirement for an 8 bit x 8 bit multiplier and its associated high power consumption is removed. Therefore, the technique with the limiters has become the primary alternative. The analysis of this scheme has been undertaken with the same conditions as were previously assumed for no limiters. The resulting control signal  $\langle H(t) \rangle$  is

$$\langle H(t) \rangle = -\frac{2}{\pi} \left[ D_i \phi_q(2p-1) + D_q \phi_i(2p-1) + A_i \cos \phi_q \sin(\psi + \beta) + A_q \cos \phi_i \sin(\psi + \beta) \right] \quad (2)$$

$$\begin{aligned} |D_i| &< |A_i| \\ |D_q| &< |A_q| \end{aligned}$$

$$= D_i \text{SGN}(D_q) + D_q \text{SGN}(D_i) \quad (3)$$

$$\begin{aligned} |D_i| &\geq |A_i| \\ |D_q| &\geq |A_q| \end{aligned}$$

where

$$\phi_i = \sin^{-1} \left( \frac{D_i}{A_i} \right); \phi_q = \sin^{-1} \left( \frac{D_q}{A_q} \right); \psi = \alpha_i(\omega) - \alpha_q(\omega)$$

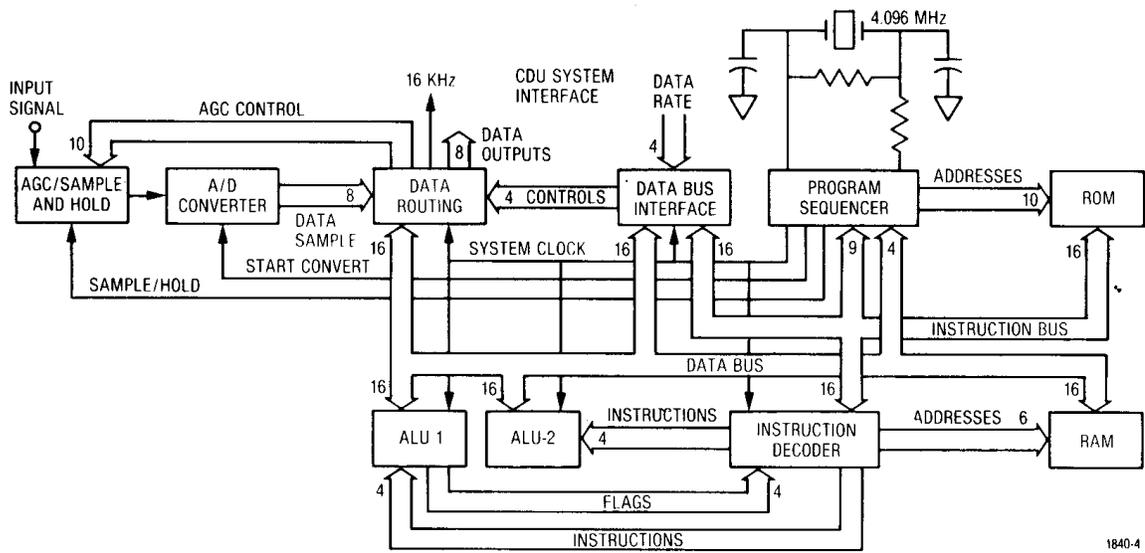
$$p = \text{Prob } m(t) = 1.$$

For dc offsets less than the signal amplitude (the only case of any practical interest) the error signal is not changed markedly from (1). For negligible offsets, quadrature errors and amplitude imbalance, the characteristic is seen to be proportional to the signal amplitude for the limited case and proportional to the signal power for the true multiplier case. Similar problems exist with  $D_i$  and  $D_q$  and quadrature Imbalance. However, as with the previous case, with the assumption of adequate transition density or with reference phase inversions, capacitive coupling renders the offsets negligible and the quadrature error can be controlled to insignificant levels. This implementation does not suffer from any significant hardware degradations since the circuits can be designed with insignificant dc offsets, quadrature errors, and amplitude imbalances.

Testing and continued development are currently underway. Using the current design concept, the HAA rapidly reduces the frequency uncertainty and is disabled or much reduced in gain after the signal is detected in the narrow tracking bandwidth. Test results indicate reliable acquisition is achievable in the order of 5 seconds at  $S/N_o = 24$  dB-Hz and  $\Delta f \leq 80$  kHz. Further testing is required to adequately characterize the performance of the HAA in an operating digital receiver.

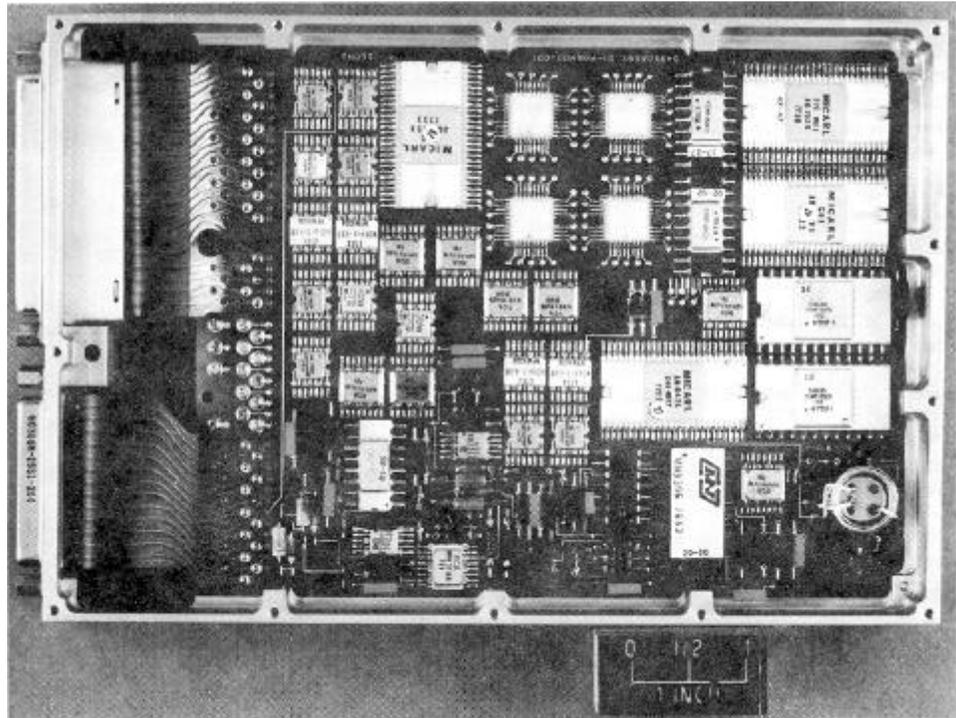
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- 6 Simon, M. K., "Optimization of the Performance of a Digital-Data-Transition Tracking Loop", IEEE Transactions on Communication Technology, October 1970, pp. 686-689.

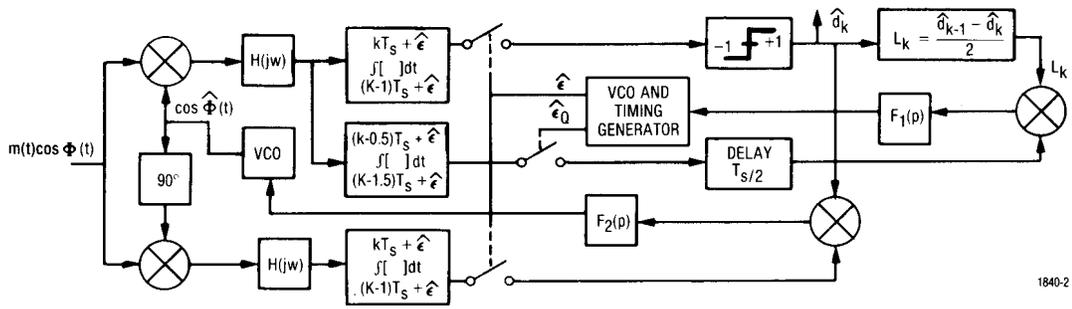


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**Fig. 1 - Command Detector Unit Block Diagram.**

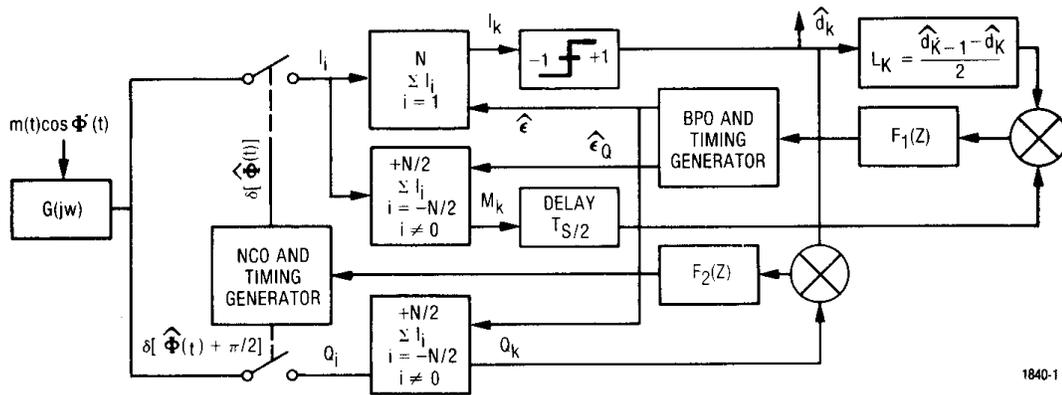


**Fig. 2 - CDU Prototype.**



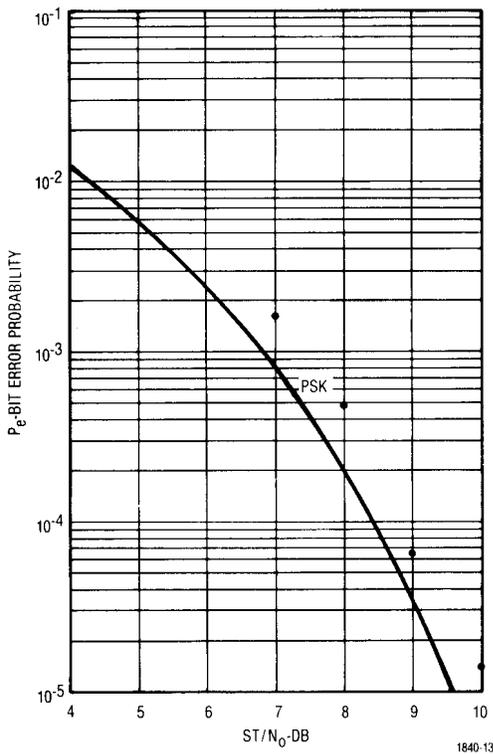
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**Fig. 3 - Classical Data-aided Receiver with DTTL Symbol Synchronizer.**



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**Fig. 4 - Sampled Data-aided Receiver with DTTL Symbol Synchronizer.**



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**Fig. 5 - CDU Test Data.**

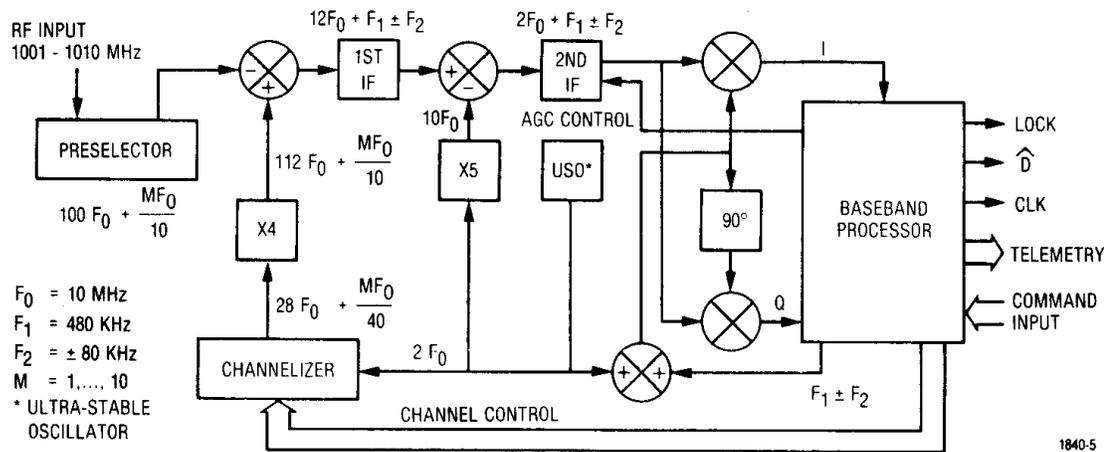


Fig. 6 - Receiver Functional Block Diagram.

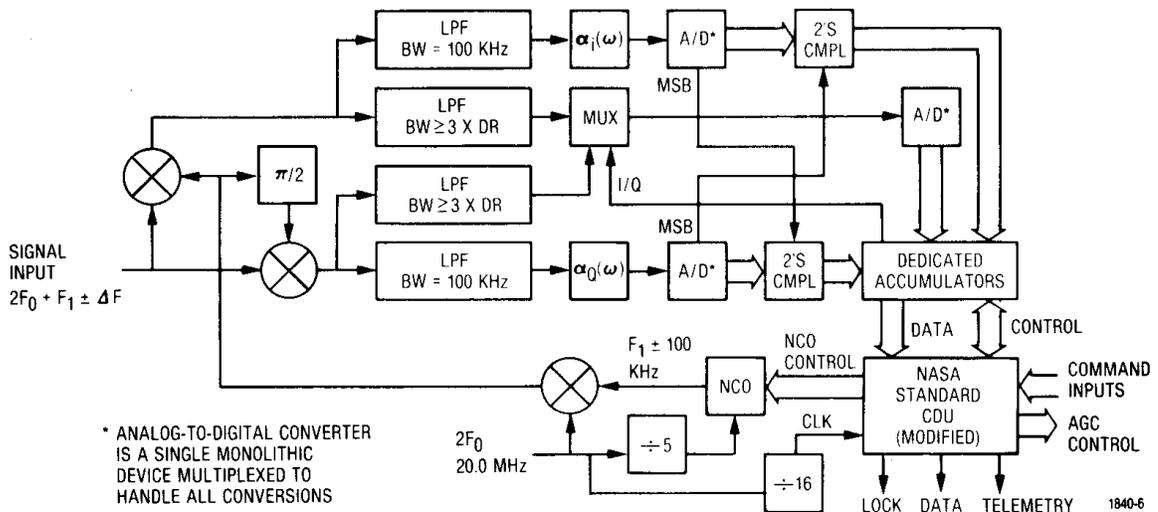


Fig. 7 - Receiver Baseband Processor.

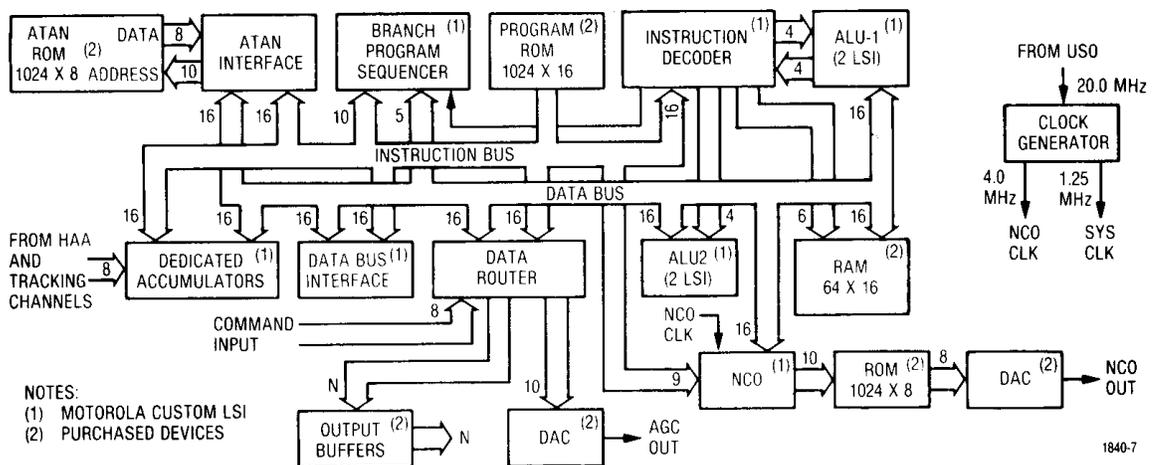
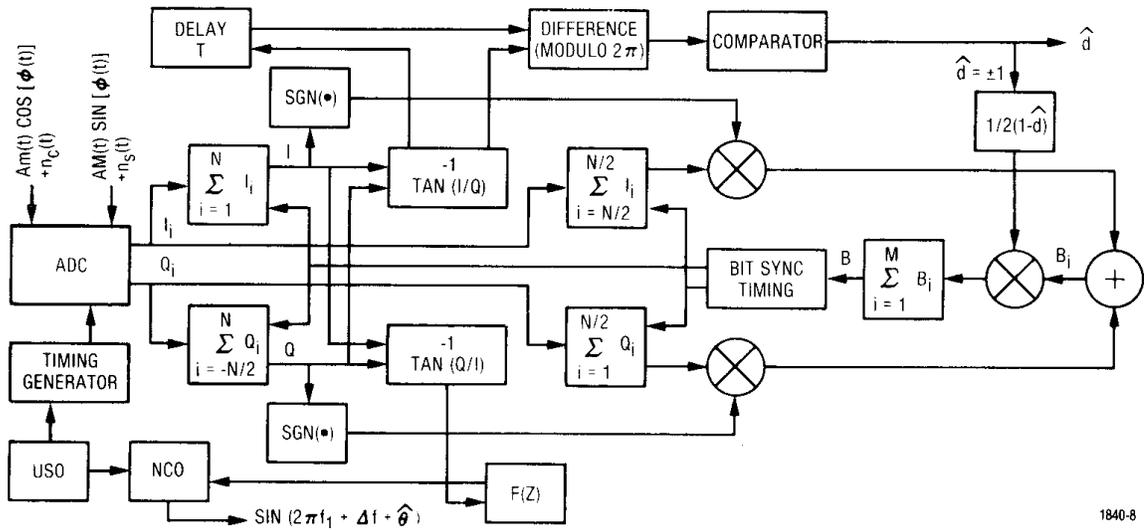
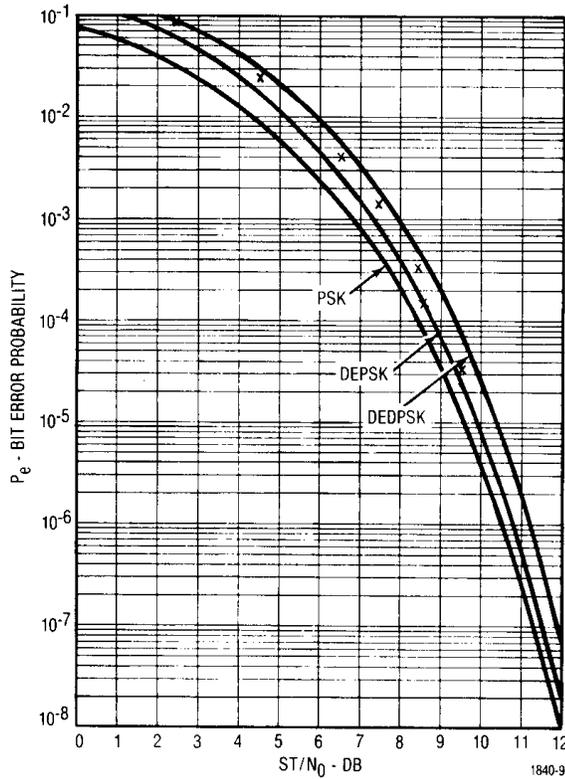


Fig. 8 - Receiver Digital Subsystem.



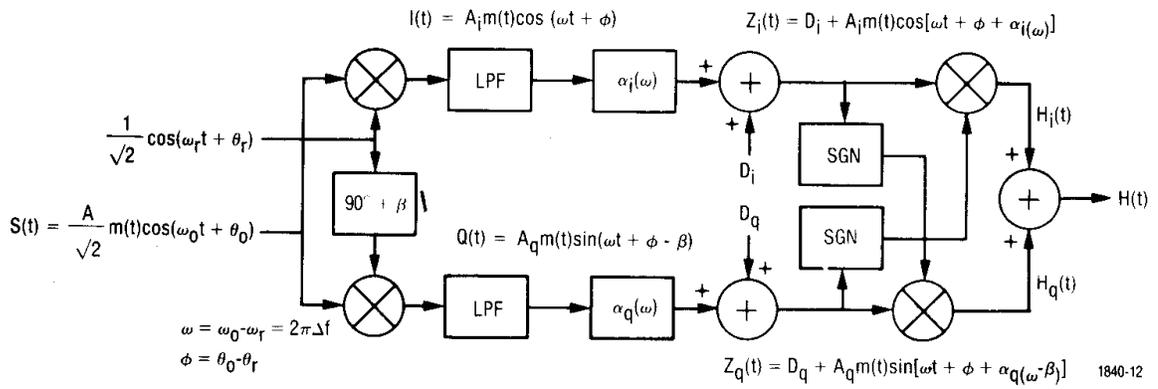
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**Fig. 9 - Differentially Coherent Demodulator For Differentially Encoded BPSK.**

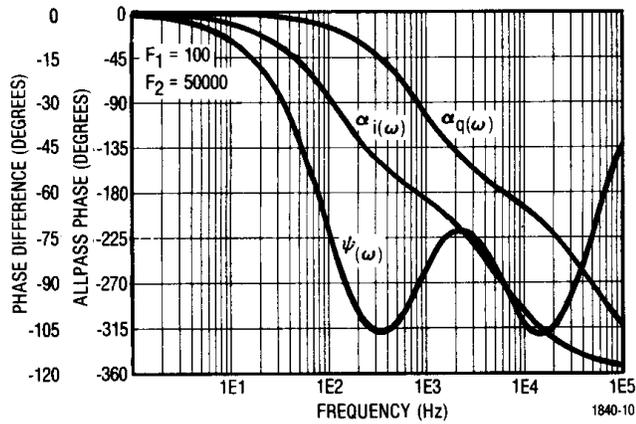


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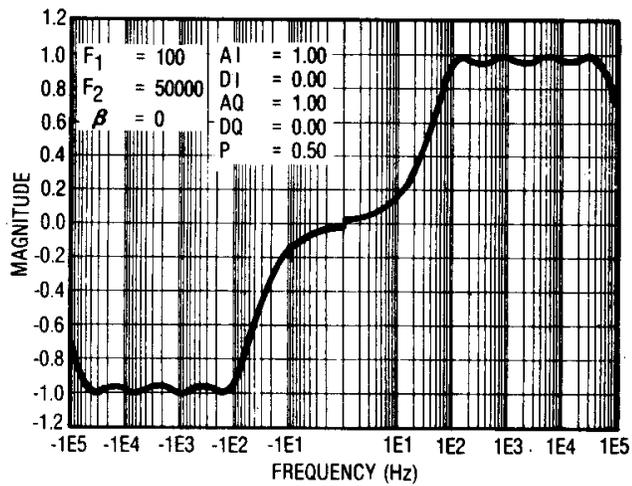
**Fig. 10 - Bit Error Probability Performance**



**Fig. 11 - Hilbert Acquisition Aid.**



**Fig. 12 - HAA Phase Angle Versus Frequency.**



**Fig. 13 - HAA Voltage Versus Frequency.**