A SEASAT SYNTHETIC APERTURE RADAR PREPROCESSOR (SARP)

Edward L. Waltz
Bendix Aerospace Systems Division
Ann Arbor, Michigan 48107

ABSTRACT

A Synthetic Aperture Radar Preprocessor (SARP) for the SEASAT radar is described. The SARP system permits playback of Synthetic Aperture Radar (SAR) data for digital processing into ocean imagery. The system includes a High Data Rate Recorder, SAR Digital Preprocessing (SDP), array processor, mass storage disc, and host computer. Data tapes are played back at reduced rates and the SDP performs the functions of frame synchronization, decommutation of time and status data, presummation of adjacent azimuth returns and correction of gain as a function of range. The data are formatted into presumed range returns and are transferred to the array processor for buffering and subsequent storage on the mass disc. This preprocessing operation loads a 100 x 100 km swath of data on the disc for subsequent range and azimuth correlation to convert the SAR data to imagery.

The SAR Data Preprocessor equipment is described and the implementation of the 35 Mbps frame synchronizer and presum arithmetic logic are detailed. A SAR Test Pattern Generator for simulation of SAR and other image data formats is also described. The test generator permits simulation of a wide range of digital data formats (including NASA and IRIG standards) and includes a programmable data pattern capability.

INTRODUCTION

The SEASAT-A spacecraft, launched on June 26, 1978 includes an L-band Synthetic Aperture Radar (SAR). The SAR is an imaging radar designed to provide data on ocean waves, sea ice, and coastal regions. The instrument images a 100 km wide swath and is designed to achieve a 25 meter resolution by processing the data in both range and azimuth to convert the radar echo into an image. This two dimensional processing effectively creates the synthetic aperture by compressing the dispersed return using correlation techniques.
The major elements of the SAR data path are shown in Figure 1. The radar antenna illuminates a 100 km swath which is offset to the side of the spacecraft ground track by approximately 300 km. The radar pulse repetition frequency may be selected to achieve four returns as the spacecraft nadir moves 25 meters in the along-track (azimuth) direction. The coherent returns are translated into S-band and transmitted downlink. The data are received at ground stations and digitized into sequences of 13,680 data samples within each range gate. The sample sequences are formatted into major frames (pulse return sequence) and minor frames (smaller fixed-size data blocks including time and status information.) The resulting serial data sequence is recorded on a High Data Rate Recorder (HDRR). The digitizing operation may be selected to provide 1, 2, 3, 4 or 5 bits per data sample, and provides 5 bit rates for recording: 23.5, 47.0, 70.5, 94.0 and 117.5 Mbps.

Spacecraft tracking and telemetry data may be used to compute orbital and spacecraft attitude information, respectively, to support image reconstruction. This data and ground calibration measurements are used to apply corrections for doppler frequency and range drifts due to orbit perturbations, spacecraft motion, altitude deviations, earth rotation, and other sensor-target motion effects.

The high density tape is subsequently processed by the SARP in two steps. The preprocessing step includes playback at a reduced data rate to unpack the SAR data, apply amplitude corrections and store a 100 x 100 km strip of raw data (with overlap) on a mass disc. The second step includes the exhaustive two-dimensional reconstruction of the returns into an image by performing range and azimuth correlation. The attitude and orbital data are used to apply geometric corrections in the correlations to reduce spatial distortions. As an additional capability, the SARP can accept density tapes of other image sensors and transfer the raw data (without SAR preprocessing) to the mass disc. This requires a flexible frame synchronizer to accommodate standard IRIG formats, and NASA Goddard Space Flight Center HDT formats in addition to the SAR format. A SAR/HDT Test Patter Generator (STPG) is used to simulate the wide range of data formats, with selectable image data content.

**SARP SYSTEM DESCRIPTION**

The configuration of the SARP system is shown in Figure 2. The major components of the system that are used for the preprocessing function are:

1. High Data Rate Recorder (HD RR) - The Martin-Marietta recorder is capable of data rates up to 120 Mbps with playback reductions of up to 1/32. The 42-track unit includes synchronization, multiplexing, deskewing and PRN randomizing logic to distribute and reassemble the serial data stream on the multiple tracks.
2. SAR/HDT Test Pattern Generator (STPG) - A Bendix generator simulates SAR data formats to permit equipment diagnostics, test tape generation and operational testing.

3. SAR Data Preprocessor (SDP) - The Bendix preprocessor accepts the playback data and performs the synchronization, decommutation and arithmetic processing functions under control of the host computer.

4. Array Processor - A Floating Point Systems AP-120B array processor is used to perform range and azimuth correlation processing. In the preprocessing mode, it controls the transfer of data onto the mass disc. The AP-120B includes a 38-bit Input/Output Processor, a Programmed I/O Processor, and 64K words (38-bit) of main data memory.

5. Mass Storage Disc - A Systems Industries mass disc storage system with 300 Mbyte storage capacity is used to store the SAR data during the multiple processing operations.

6. Host Computer - A Data General Nova digital computer controls all processing activities and provides support computations. In addition, the host computer system includes peripherals and image displays to provide computer tapes and quick-look displays of processed imagery.

The preprocessing function includes the playback of data to extract a selected swath of data (approximately 100 x 100 km) and transfer the data to the mass disc. The major functions performed in the preprocessing mode are:

1. HDDR Playback - The HDDR reproduces the SAR data at rates between 1/4 and 1/32 real-time and provides a serial data stream to the SDP.

2. Synchronization - The SDP synchronizes to the minor frame format and automatically acquires word and frame count. Minor frame count is used to achieve major frame synchronization.

3. Demultiplex - The SDP demultiples the header, data, and fill information from the format. Header data (status/time) are transferred to the host computer, and certain time and status parameters are displayed on the front panel. This demultiplexing is performed over the entire range of format parameters (e.g. bits/sample, minor frames/major frame, etc.) The image and fill data samples are demultiplexed and transferred to the SDP arithmetic processor. The SDP interrupts the host computer each major frame and transfers synchronization status and header data.

4. Presummation - Multiple-look returns may be presumed with a weighting function applied to each unique return. The summation may occur over 1 to 32 returns, and an error
correction capability is provided to insert best estimate values for lost minor frames. The weighting function values are provided by the host computer.

5. Offset and Range Gain Correction - A geometric offset for the beginning pixel (representing start of track on the Earth’s surface) is provided by the host computer to indicate the first sample element (in a return) to be transferred to disc. In addition, a gain correction function may be applied across the range to compensate for the SAR Sensitivity Time Control (STC) gain function. This gain is provided by the host computer as a continuous sampled function with a gain value for each range element.

6. Transfer to Array Processor - The SDP transfers preprocessed (or raw decommutated data directly from the demultiplexer) to the array processor via an IOP 38 (I/O Processor) interface. Transfers occur as 16 bit, two’s complement samples packed into 38 bit double words. The IOP directs the data to the main data (MD) memory of the array processor.

7. Array Processor Buffering - The array processor buffers the incoming data and assembles blocks for transfer to the mass disc via the Programmed I/O Processor (PIOP). The PIOP formats the preprocessed blocks for subsequent retrieval during the range/azimuth correlation process.

The host computer controls the input operation and selects the desired data swath by monitoring the time code provided by the SDP. The operator inserts the starting time of data into the host computer for comparison with the time information transferred from the SDP. Upon detection of the correct starting and ending times, the computer will command the loading of data onto the disc.

SAR/HDT DATA FORMATS

The major elements of the data formats accommodated by the SARP are: (1) Major Frame - this includes a sequence of minor frames and typically represents a single radar return or scan line. (2) Minor Frame - a fixed-length block of bits which includes frame synchronization, header data and a subset of the major frame data sequence, (3) Frame Sync Pattern - a unique code pattern of up to 32 bits which identifies the beginning of each minor frame, (4) Header - a sequence of bits which include minor frame number, time code, sensor status and other ancillary data, and (5) Data - a fixed-length sequence of words representing sequential data samples.

The SDP will accommodate a wide range of image data formats, including IRIG formats, SEASAT SAR and the NASA GSFC High Density Tape - Production (HDTp) formats. The SAR format provides for variable number of minor frames per major frame to permit
addition of “fill frames” at the end of each major frame. These frames are inserted in the digitizing-formatting operation to eliminate timing drifts between the incoming PRF and outgoing serial data rate. The SAR data format includes a fill flag and minor frame count to permit unique identification of the minor frames containing data.

SERIAL DATA PREPROCESSOR (SDP)

The SDP is a hardware digital processor which includes both ECL and TTL logic. The major elements of the unit are shown in Figure 3. Serial digital data are input from the HDRR or STPG to the frame synchronizer which acquires lock with the minor frame format. Decommutated header data are displayed on the front panel and transferred to the computer interface. The data samples are decommutated and parallel transferred to the digital preprocessor for presuming, double buffering and gain correction. The digital preprocessor accumulates complete presumed SAR returns (13,680 words) and passes the blocks to the array processor interface. Non-SAR data decommutated from HDT formats are packed and directly transferred to the interface. The computer interface communicates with a host computer direct memory access (DMA) to transfer status and header data to the computer. In addition, the computer can transfer blocks of presum and gain coefficients to the SDP via this interface. The following paragraphs provide a functional description of these SDP elements.

1. Frame Synchronizer - Serial data at rates up to 35 Mbps are accepted and a three-state synchronization strategy is employed to acquire lock with the minor frame format. Figure 4 is the state transition diagram for the synchronizer. The three states have programmable error tolerances ($e_1, e_2, e_3, W, N_1, N_2$ and $N_3$) and permit optimization of the mean time to acquire frame sync and probability of retaining true lock. The definition of each state is as follows:

   Search - A bit-by-bit search is conducted for any pattern within with $e_1$ error tolerance. When the criterion is met, the synchronizer advances to the check state and an expected sync window is established.

   Check - The bit-by-bit search is continued in the event a better pattern is detected (within the $e_2$ tolerance and smaller than the earlier pattern) and, if found, the expected sync window is reset. If the word within the sync window plus slip aperture, $W$, does not meet the $e_2$ criterion, the synchronizer reverts to the search mode. If, however, $N_2$ consecutive windows meet the tolerance criteria, the synchronizer advances to the lock state.

   Lock - The lock state is retained until $N_3$ consecutive frame syncs cannot be found within the $e_3$ and $W$ error criteria. If this occurs, the synchronizer returns to the search state.
Figure 5 shows the arrangement of the synchronizer logic. The incoming NRZ data is shifted into a 32-bit shift register and the parallel output enters a comparison network. The network includes a 32-bit mask and exclusive-or gating. The 32 comparisons enter a unitary adder to convert the sum-of-errors to a binary value for comparison with the error tolerance, $e$. The adder is a 4-stage, pipelined architecture employing programed read only memories (PROM) to perform the addition. The sum-of-errors value is compared at each bit interval with the error tolerance for the current state ($e_1$, $e_2$, or $e_3$) and with the previous best pattern to generate the “sync detect” and “better pattern” signals. The sync state control function is performed by a sequential state machine which employs a PROM to generate next state decisions based on five inputs: 1) current sync state, 2) sync detect, 3) better pattern detect, 4) sync aperture, and 5) consecutive word criteria overflow. The control PROM implements the state diagram (Figure 4) and controls the state of three elements: 1) the bit/word and word/frame counters are reset and enabled to synchronize their counts with the incoming data, 2) a test counter, $N$, is incremented to count consecutive frame events for comparison with the $N_1$, $N_2$, and $N_3$ criteria, and 3) the state flip-flops are controlled to make the necessary state transitions. Once in the LOCK state, the bit/word and word/ frame counters provide the necessary clocking to decommutate the minor frame format.

2. Format Demultiplexer - The header and SAR data are independently stripped from the data format in the lock mode. The first eight bits following the sync word (minor frame count) are used to direct the following eight bits (time/status) to appropriate locations in a scratch pad memory. The time/status words for the first ten minor frames are stored for subsequent transfer to the host computer, and are decoded for display on the SDP front panel. Since the SDP accommodates data word formats between 1-5 bits/word for SAR and 4-16 bits for HDT data, the demultiplexer must accommodate 1-16 bit words. SAR data are formatted into 8-bit words for transfer to the arithmetic logic. HDT data are packed into 16-bit words for direct transfer to the array processor.

3. Digital Preprocessor - The digital preprocessor is a hardwired arithmetic processor which performs three primary functions: 1) Non-coherent presumming of adjacent (azimuth) returns to provide a weighted summation of multiple-look data, 2) double buffering of presummed returns to buffer the asynchronous input/output operations, and 3) application of a gain function to permit precision correction of SAR range-gain effects.

Figure 6 shows the data flow in the preprocessor logic. Incoming SAR returns are sequences of 13,680 8-bit data samples. While in the LOCK mode, the sequence is stored in the D memory (Delay) and input to the presum logic through the input multiplexer. In the event of a loss-of-sync, the D memory is switched to the read mode and the input multiplexer enables this (previous azimuth) return to be substituted in the presum until sync is reacquired. The data sequence from the input multiplexer is multiplied by a coefficient,
W_n, prior to accumulation with previous returns. The presum can be defined as a vector operation on 13,680 element vectors:

\[ \bar{S} = \sum_{n=1}^{L} W_n \bar{X}_n \]

where:
- \( \bar{S} \) = Weighted vector sum of L returns (13,680 elements)
- \( L \) = Number of adjacent returns to be summed
- \( W_n \) = Scalar weighting coefficient for the Nth return
- \( \bar{X}_n \) = Nth Vector return

The accumulation of the weighted sequences is performed by a recirculating memory which operates in the read-modify-write mode. The system accommodates up to \( L = 32 \) looks and a scaling network is provided after weighting to maintain proper dynamic range in the accumulated data. The recirculating memory is implemented as two 64-bit wide, double buffered memories to achieve the required processing speed. The two memories alternate in the input/output modes each time the mod L counter indicates that a group of L returns have been summed. Upon readout, the presumed return is vector multiplied by a gain vector which is stored in the G x memory:

\[ Y = G_x \bar{S} \]

where:
- \( Y \) = Gain corrected return vector (13,680 elements)
- \( G_x \) = Gain vector (Gain as a function of ranger
- \( \bar{S} \) = Weighted vector sum of L returns

The 32-bit product is scaled to 16 bits and is output to the array processor interface.

4. Array Processor Interface - The preprocessed data sequences are transferred to the array processor under DMA control by the IOP-38. The 16 bit SAR and HDT words are packed into 38 bit words for the block transfers. The IOP-38 acts as the master during the transfer and provides the pointer addresses for both the SDP and array processor memories while maintaining word count.

5. Host Computer Interface - A direct memory access interface permits the host computer to perform five transfer functions to control the SDP: 1) read status of SDP synchronizer, 2) read contents of the header scratch pad memory, 3) issue reset-start command to SDP, 4) load presum coefficients \( W_n \) into the presum memory, 5) load gain
coefficients into the G memory. The SDP provides an interrupt at the beginning of each major frame and at minor frame number 9 when the header data is ready for transfer.

6. Operator Panel - The front panel (Figure 7) provides a display of time and status from the header data and indicates the frame synchronizer state. The frame synchronizer format and sync strategy parameters are entered via thumbwheel switches. Additional displays of the interface status and control of the preprocessor scaling are provided on the panel.

DISC LOADING OPERATIONS

The array processor acts as a buffer-formatter between the SDP and the mass storage disc, and controls the input (IOP-38) and output (PIOP) devices which block transfer the data to and from main data memory. The array processor control microprogram causes the incoming data blocks (preprocessed returns) to be sequentially loaded onto the disc at an aggregate throughput rate of approximately 400K samples per second. The characteristics of the transfer strategy which achieves this rate are:

1. Format - Each 13,680-sample return (16-bit samples after preprocessing) occupies 54 sectors. This requires the use of two tracks with 64 total available sectors. The residual ten sectors (256 bits each) are not used to provide timing margin between returns and to start all returns on track boundaries. The cylinder-cylinder head movement is caused to occur between returns by using an even number of tracks down the cylinder.

2. Capacity - The total disc capacity that can be achieved is 9 records per cylinder times 823 cylinders. This capacity of 7407 records (returns) corresponds to a 185 km downtrack distance (azimuth) if four-look presumming (L = 4) has been performed.

3. Timing - The 400K sample per second sustained transfer rate is achieved by performing triple buffering in the array processor and formatting the data to assure that the loss of a disc revolution occurs only on cylinder changes. The maximum sustained transfer rate is 388K samples per second while the peak transfer rate is 605K samples per second.

SYSTEM THROUGHPUT

The system throughput rate to load the mass disc is determined by data rate criteria of the SARP components. Four primary data rate criteria define the upper limits of the disc and SDP and the lower limit (playback reduction) of the HDRR:

1. The mass disc can sustain a 388K sample per second input transfer rate to fill to capacity.
2. The effective SDP output sample rate to the array processor is a function of incoming bit rate, bits/sample digitzation, and amount of presumming selected.

3. The SDP fame synchronizer can accept bit rates up to 35 Mbps and the presum memory has an effective input word rate of 6 Mwps.

4. The SAR data is recorded at bit rates between 117.5 and 23.5 Mbps and playback reductions of 1/2, 1/4, 1/8, 1/16 and 1/32 are permitted within the HDRR bit error rate criteria.

As a result of these criteria, the HDDR playback rate (for any given value of bits/sample and presum quantity) must be selected to maintain an SDP output rate which does not exceed the disc input transfer rate. The playback reductions range from 1/32 for the L = 1 case (no presum) to 1/4 for L = 32.

**SAR/HDT TEST PATTERN GENERATOR (STPG)**

The STPG provides a serial digital data stream suitable for recording on the HDRR or for simulating the playback of data from the HDRR. The test pattern data may be used for HDRR performance evaluation or to provide a stable, repetitive signal for equipment diagnostics. The SEASAT SAR data format is a subset of a wide range of selectable formats that may be generated by the STPG. The range of operator selectable format parameters are summarized below:

1. Bits/Word - 1 to 8 bits
2. Sync Pattern - 24 or 32 bits
3. Words/Minor Frame - 1 to 2048
4. Minor Frames/Major Frame - 1 to 2048
5. Major Frames Repeat - 1 to 16,384
6. Non-Fill Minor Frames - 0 to 2,048
7. Bit Rate - 8 bps - 40 Mbps

In addition, the data field may be selected to include one of three types of data:

1. Pseudorandom Code - 511 bit maximal length repeating sequence
2. Fixed Code - Fixed binary code as set in panel switches
3. Stored Program - One of four minor frame programs and one of two subcom programs may be selected. The test pattern programs are stored in PROM and generate the data word sequence.
The STPG is constructed with ECL logic and is packaged in an integral chassis with power supplies. Figure 8 emphasizes the major sections of logic. A frequency synthesizer provides a basic clock rate between 000.001 and 160.000 mHz which may be divided by 4, 8, 16, 32, 64 or 128 to provide the output data rate. The resulting bit rate clocks the cascaded timing counters: bits/word, words/minor frame, minor frames/major frame, and major frame count. The modulus of each of these counters is determined by front panel switches. The master timing logic utilizes the states of these counters to control the shifting of sync, header, and data words into the output stream. The contents of the word counter addresses the selected PROM to step through a data field program which can be up to 256 words in length. The PROM contains 4-bit instructions which control an 8-bit data generator. The instructions provide nine operations on the output value, \( x \): \( (x + 1) \), \( (x + 2) \), \( (x - 1) \), \( (x - 2) \), \( X \), 0, 1, NOP, or jump to subcom program. The two subcom programs include similar data operations and may be addressed by the minor frame or major frame counter. This flexible data generation capability permits the generation of ramps, steps, impulse functions, grids, and bar patterns which are useful in testing image processing systems.

The output logic includes individual shift registers for data generator words, sync code, pseudorandom code, and pseudorandom fill code. Each register is gated onto the output data stream by the master timing and the data multiplexer selects header or pattern data. The sync pattern register includes the capability to insert sync errors in all minor frames or in alternating frames to exercise the frame synchronizer.

**CONCLUSION**

The SARP system provides a flexible means of processing SAR data for development of reconstruction techniques. The mass disc for temporary data storage, programmable array processor and hardware preprocessor provide a cost-effective system for handling SAR data. While the throughput for this system is low, alternate multiple-array processor configurations with additional memory can achieve significantly increased processing speeds. The flexible input capability of the SDP permits the system to be used for a wide range of SAR and imaging sensors with the addition of post processing software.

**ACKNOWLEDGEMENTS**

This work was performed for the Naval Research Laboratory, Washington, D.C., under the direction of Dr. Alan Petty. I wish to express appreciation for the development of the SARP concept by Drs. Igor Jurkevich and Steven Mango of NRL under the direction of Dr. Petty.
FIGURE 1 - SYNTHETIC APERTURE RADAR DATA HANDLING AND PROCESSING FLOW

FIGURE 2 - SAR PREPROCESSOR SYSTEM CONFIGURATION
FIGURE 3 - SAR DATA PREPROCESSOR (SDP) BLOCK DIAGRAM

FIGURE 4 - SDP FRAME SYNCHRONIZER STATE DIAGRAM
FIGURE 5 - FRAME SYNCHRONIZER BLOCK DIAGRAM

FIGURE 6 - DIGITAL PREPROCESSOR ARCHITECTURE
FIGURE 7 - SDP FRONT PANEL CONFIGURATION

FIGURE 8 - SAR TEST PATTERN GENERATOR (STPG) BLOCK DIAGRAM