HIGH SPEED A/D CONVERTER TECHNOLOGY SURVEY

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ABSTRACT

Surveyed are current and future high speed A/D technologies with potential for a significant impact on future systems. Current bipolar silicon monolithic quantizers and hybrid sample-and-hold circuits are described. The gallium arsenide integrated circuit technology, including FETs and TEDs, provides speed increases from 10 to 100. Josephson Junction devices are discussed as a technology potentially offering radical increases in sample rates and reductions in power.

1. INTRODUCTION

In the past ten years, as systems have changed from analog to digital implementations, operational requirements have outpaced development high speed analog-to-digital A/D converters so that the A/D is often the limiting factor in system performance.

Development of high speed, small, reasonably priced avionics digital processors has permitted designers to greatly increase system performance. However, the limitations of high speed A/D converters has frequently required these new systems to be overly complex and expensive.

Modern electronic systems are required to process signals with bandwidths of up to 500 MHz and a dynamic range as high as 60 dB. This implies that the A/D converter-samples at a 1 Gsps rate with 8 to 10 bit resolution. In addition, for optimum signal detection and processing, it is necessary to keep the intermodulation products introduced by large signals or jammers as much as 60 dB below the signal of interest. The combination of high sampling rates, wide dynamic range, and excellent linearity presents a very difficult problem for the A/D designer.

Historically, A/D converters were designed utilizing conventional digital logic and linear devices such as the Motorola MC1650 voltage comparators and were packaged on one or more printed circuit boards. Although many current A/D converters still use this type of design it is evident that the desired sample rates and resolutions have extended

beyond those capable with these devices. Only through micro-miniaturization and hybridization can the input bandwidth and sample rate be increased.

The desire to simultaneously achieve high sample rates, high resolution, and good linearity leads to the development of monolithic LSI circuits for A/D converters. In the past five years a number of circuits have been introduced and are now beginning to be used in new systems. These circuits are most accurately described as quantizers, since most applications require a sample and hold and ancillary circuits to form a complete A/D converter. A quantizer consists of the circuitry (comparators, D/A converters, etc.) to convert an analog voltage to a digital word representing the analog signal value. As LSI circuit development has progressed, more circuitry has been incorporated into the chip. The ultimate goal is to develop a true single chip monolithic A/D converter that includes the sample and hold, reference circuits, and all timing and control logic.

This paper describes the current state of the art in monolithic quantizers and sample-and-hold circuits. It also projects future developments in these areas.

2. MONOLITHIC QUANTIZERS

BIPOLAR LSI PROCESS

All of the high speed quantizer circuits that have been developed or are in development use a silicon bipolar process similar to the ones used for emitter-coupled logic. Some commerical quantizers are available using a CMOS process; however, they are limited to a maximum sample rate of 1 Msps.

The bipolar processes produce microwave transistors with an f_T of up to 5 GHz with a yield compatible with LSI requirements. The transistors are well suited for the requirements of A/D converter circuitry and are useful for converters with accuracies of up to 12 bits and speeds of up to 500 Msps. Typical parameters for a high speed bipolar process are given in Table 1.

VOLTAGE COMPARATOR ARRAYS

The first monolithic quantizer was a voltage comparator array developed by TRW DSSG in 1972.[1] The circuit developed was a 2 bit quantizer (2BQ) containing four comparators and encoding logic. This circuit was designed for use in parallel and subranging A/D converters. Four voltage comparators have their positive inputs parallel and their negative inputs connected to taps on an external reference voltage divider. Comparator outputs go to encoding logic to translate the four line code into a two line

binary code. A packaged device is shown in Figure 1. This circuit was used in a 20 Msps 10 bit subranging A/D converter.[2]

By 1974 two 3 bit quantizers (8 comparators) had been developed: One by MIT, Lincoln Laboratory[3] and one developed by TRW DSSG. Both circuits included a thin film resistor-divider network to distribute the reference voltage to the comparator negative inputs.

The TRW circuit was used in a 400 Msps 5 bit parallel A/D converter developed in 1976. The A/D converter uses four 3BQs connected in parallel and a monolithic second level encoding circuit to combine the four 3 bit binary outputs into a 5 bit binary output and a monolithic timing logic circuit to generate all timing and control signals. The converter, in a 3 x 3 inch thin film hybrid (Figure 2), also contains the reference circuits and a hybrid sample and hold.

In 1976 Tektronic Inc. developed a 4BQ (16 comparators).[4] This circuit has sufficient accuracy for use in a 20 Msps 8 bit subranging A/D converter (Figure 3). The 4 MSBs are decided by the first 4BQ. The 4BQ output is stored in the 4 bit register that drives a 4 bit A/D with a 8 bit resolution. The D/A sets the reference voltage for the comparators in the second 4BQ, which then decides the four LSBs. The 8 bit result is then transferred to an 8 bit output register.

SUCCESSIVE APPROXIMATION QUANTIZERS

Although the 3 and 4 bit quantizers represent a significant advancement over previously available circuits, they still require multiple circuits for higher resolution and a significant amount of ancillary circuitry. The use of multiple monolithic circuits and hybrid fabrication techniques lead to higher power and cost. To eliminate these objections, single chip monolithic quantizers using a successive approximation algorithm were developed. This algorithm combines excellent linearity and high dynamic range.

A block diagram of a 10 bit quantizer is shown in Figure 4. The quantizer consists of a single comparator driven by a 10 bit D/A converter. The D/A is initially set to mid-scale (MSB ON) and the D/A output compared to the analog input. The comparator decision is stored in the D/A latch and, depending on the decision made by the comparator, the MSB either remains on or is turned off. The next most significant D/A bit is then set and a new decision made. This process continues until the least significant bit decision is made. At this time the D/A latches contain the binary representation of the analog input. The binary word is then transferred to the output latch and a new conversion started. Timing and control signals are provided by the shift register. This quantizer requires a conversion clock and a bit clock.

The first circuit introduced was a 10 bit 5 Msps device.[5] This quantizer requires only a sample and hold, reference circuit, and MSI timing logic to form a complete A/D converter. A photograph of a packaged device is shown in Figure 5. This circuit is being used in a 5 Msps 10 bit A/D converter for the APS 125 radar. The development of this circuit was followed by two other devices.

These devices represented the limit of the LSI process since it produced devices with an f_T of only 1.5 GHz. A higher performance process with a self-alignment technique that uses oxide wells for the alignment of several mask steps was used for subsequent developments. This process features transistors with an f_T of 5 GHz and achieves higher speeds with less power.

In 1976 two higher speed circuits were developed using the oxide aligned process. Both circuits incorporated an internal analog voltage reference that uses the bandgap voltage of silicon to generate a precise temperature independent voltage.[6] One circuit also includes logic to generate a sample-and-hold strobe. Inclusion of the internal reference and sample-and-hold strobe allows a complete A/D to be implemented with less additional circuitry. An avionics A/D converter using the 8 bit 12 Msps device is shown in Figure 6. This is a complete A/D including a hybrid sample and hold and all timing logic. This converter provides a high sample rate with high reliability and excellent linearity (0.1 percent of full scale).

The performance of some typical TRW successive approximation quantizers is summarized in Table 2. A 10 bit 10 Msps circuit represents a practical limit for quantizers using the successive approximation algorithm, because at this rate the D/A must settle to 10 bit accuracy and the comparator must make its decision in only 8 nsec. Even though subranging quantizers are more complex, they have a distinct speed advantage.

3. HIGH SPEED SAMPLE-AND-HOLD CIRCUITS

CURRENT TECHNOLOGY

The advancement of sample-and-hold technology has not been as rapid as that experienced in quantizer developments. While monolithic quantizers were being developed, the emphasis in high speed sample-and-hold technology has been with thin film hybrid circuits. This is primarily because the excellent linearity bandwidths of up to 1 GHz, and small aperture times are much easier to achieve with the inherent flexibility of a thin film hybrid. Although the use of hybrid technology represents a significant advance from the discrete components formerly used, they still result in circuits that are complex and costly.

HYBRID SAMPLE-AND-HOLD CIRCUITS

A typical high speed sample-and-hold hybrid circuit is shown in Figure 7. The hybrid package size is 1.75 x 1.3 inches. The deposited conductors, thin film resistors, chip transistors, and capacitors are constructed on a 25 mil alumina substrate. The power dissipation is approximately 0.8 watt. This circuit was designed for applications requiring 10 bit accuracy at a 25 Msps rate and is usable with parallel quantizers up to 50 MHz sample rates with no loss in performance (Table 3).

Figure 8 is a block diagram of the sample-and-hold circuit. When the SAMPLE signal input commands the sample and hold to track the analog input, the bridge drive output voltage turns on the hot-carrier diode bridge and connects the preamplifier output to the hold capacitor. The sudden charging of the hold capacitor distrubs the preamp output, but because of the low output impedance, this voltage transient does not disturb the analog signal source driving the sample-and-hold input.

After this transient period is over, the bridge drive output voltage reverses, the bridge switch opens, and the preamplifier is disconnected from the hold capacitor.

The postamplifier presents a high impedance to the hold capacitor and a low impedance output. A field effect transistor with a very low input current prevents excessive droop of the voltage at the hold capacitor. Excessive droop will cause quantizing errors during the conversion time.

A sample and hold designed for use in the 400 Msps 5 bit parallel quantizer discussed previously is shown in Figure 9. Because this circuit requires a wider bandwidth than the 50 Msps 10 bit application, the circuitry has been modified to achieve more bandwidth by giving up linearity. Instead of the complementary emitter-followers in the previous circuit, FET source followers and emitter-followers are used to obtain broadband performance at the expense of linearity.

MONOLITHIC SAMPLE-AND-HOLD CIRCUITS

Development of a monolithic sample and hold is crucial to the development of a single chip monolithic A/D converter. The key to this development is a monolithic circuit that combines high frequency response with excellent linearity. The currently available commercial monolithic sample-and-hold circuits achieve very good linearity by using feedback amplifiers. However, these circuits have poor frequency response and MOS FET switches which result in very poor sampling aperture times. These circuits are limited to sample rates of 1 Msps.

For the past year TRW has been engaged in the development of a monolithic sample-and-hold circuit. Several solutions for combining high speed and good linearity have been investigated. At this time a high speed monolithic sample and hold is practical, and development is continuing; the expected performance is shown in Table 4.

4. FUTURE DEVELOPMENTS

4.1 LSI Technologies

Several technologies offer potential for future LSI high speed A/D converters. The four most promising are silicon bipolar, gallium arsenide FETs, gallium arsenide TEDs, and Josephson Junctions. Silicon bipolar has the most near term use because of its maturity; however, gallium arsenide is being rapidly developed. Josephson Junctions are the least mature but may ultimately have greater performance.

SILICON BIPOLAR TECHNOLOGY

Although advances in bipolar technology will not be as dramatic as in the past it has not yet reached its full capability. Improvements in photolithography and the use of electron beam lithography will result in transistors with a f_T of 6 to 7 GHz and two to three times lower intrinsic capacitances. With this performance an LSI A/D converter with a 500 Msps 8 bit capability should be achievable in five years.

Development of a monolithic sample-and-hold circuit will occur within the next two years, leading to the development of single chip LSI A/D converters. It is probable that the first single chip converter will be introduced by 1980.

GALLIUM ARSENIDE FETs TECHNOLOGY

Monolithic gallium arsenide field effect transistors are high speed medium accuracy devices being used to fabricate experimental SSI and MSI logic circuits with speeds up to 1 GHz. The use of a semi-insulating substrate offers the advantage of circuit capacitances of 10 to 100 times less than those achievable with silicon bipolar-technology. Since, in an LSI circuit the speed is primarily limited by RC time constants, a gallium arsenide circuit can achieve higher speeds with less power. Additional process development will be required before LSI circuit developments move from the experimental to the production stage. The areas requiring further development are planar transistors and electron beam lighography.

The accuracy potential of gallium arsenide FETs does not appear to be as great as that of bipolar transistors. The threshold variations currently experienced need to be improved before converters with greater than 10 bits are practical.

Studies have shown that the application of gallium arsenide FET technology to A/D converter developments will be highly advantageous. Converters with sample rates of up to 2 GHz with 8 to 10 bit accuracy can be developed in the next three years. Projections of the achievable A/D converter performance are shown in Table 5. Since the gallium arsenide process has FETs and Schottky diodes available, the design of a monolithic sample and hold is relatively simple. Therefore, it is logical to assume that the monolithic A/D converters developed will include the sample and hold.

GALLIUM ARSENIDE TED TECHNOLOGY

Transferred electron devices (TEDs), also known as Gunn effect devices, are microwave devices which exhibit negative resistance with a dc bias is applied between cathode and anode such that their internal fields exceed a threshold level of about 3.15 kV/cm. If a Schottky barrier gate electrode is added near the cathode, the cathode-anode bias can be set near but below the threshold level, and a negative dc voltage, pulse, or RF signal can be applied to the gate to trigger the device into its negative resistance region. When the TED is biased into the negative resistance region it oscillates at a frequency determined by the gate to anode separation. If the input pulse is short (say less than one-half the period of the output frequency) the TED will produce a single (amplified) output pulse. If the input gate is split, the device can be made to function as an AND or OR gate, producing an output signal when either gate input is a negative pulse (for the OR gate) or when both gate inputs are negative pulses, depending on the cathode-anode bias.

The TED is basically a threshold device and with the proper selection of bias can be used as a comparator in an A/D converter. A monolithic single bit cell is a useful building block for higher accuracy converters. The expected performance of such a cell is given in Table 6. Several of these cells can be connected in series to form a higher speed A/D converter than GaAs FET A/Ds, but at lower accuracy and higher power.

JOSEPHSON JUNCTION TECHNOLOGY

Josephson Junction technology is furthest from maturity, has some very substantial problems yet to be solved, but offers the lowest power delay products of any known technology. Josephson Junction devices are expected to achieve switching times of 1.0 psec at a power of 10^{-8} watts for a power-delay product of 10^{-8} pj. Josephson Junction devices are formed by weakly linked superconductors and exhibit extremely broadband

(0 to 1000 GHz) negative resistance when cooled between 40K with the necessary supporting electronics will prove very difficult.

A Josephson Junction has two modes of operation: 1) in the current mode, the junction is a superconductor with zero junction voltage; 2) at higher junction currents, the device becomes resistive, with a voltage discontinuity of about 2 mV at the threshold point. The magnetic field near the junction affects the threshold current at which the device switches from the current state to the voltage state. Electronic circuitry using Josephson Junctions often uses this magnetic sensitivity to control the threshold of a junction with the magnetic field generated by current flowing in another part of the circuit.

Josephson Junctions currently exhibit switching speeds of less than 50 psec and power consumption of less than 10 μW per junction, resulting in a speed power product of less than a femtojoule. State-of-the-art threshold current matching monolithic Josephson Junction is about 10 percent, which implies that extensive development is required to achieve A/D accuracies greater than 4 bits. IBM has developed a 62.5 Msps, 4 bit A/D converter using Josephson Junctions, but the ultimate potential of the technology is believed to be as high as 50 Gsps at 8 bits.

5. TECHNOLOGY COMPARISON

A comparison of the ultimate performance of the technologies previously discussed is given in Table 7. Gallium arsenide FETs offer the greatest potential for near term high speed A/D converter developments, with TEDs and Josephson Junctions offering higher sampling rates and lower power in later developments. The table also presents the current state of the art in each A/D technology.

The 10 to 100 speed increases offered by gallium arsenide A/D converters are a revolutionary step which will have a dramatic effect on the configurations of future EW, radar, and communications systems. Sample rates of 10 GHz should result in very important new performance capabilities for these systems, including greatly enhanced radar resolution or increased communications capacity. Finally, the Josephson Junction technology, while perhaps 10 years from application to real systems, offers a radical advance in speed and reduced power. Successful future systems designs will almost certainly incorporate one of these advanced technologies.

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3. C.E. Woodward, K.H. Konkle, and M.L. Maiman, “A Monolithic Voltage Comparator Array for A/D Converters,” IEEE Journal of Solid State Circuits, Vol. SC10, pp. 392-399, December 1975.

4. R.A. Nordstrom, “High Speed Integrated A/D Converter,” ISSCC Digest of Technical Papers, pp. 150-151, February 1976.

5. D.R. Breuer and J.D. Hyde, “10 Bit 5 Megasample/Second Monolithic A/D Converter,” ISSCC Digest of Technical Papers, pp. 152-153, February 1976.

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Table 1. Bipolar LSI Process Parameters

- TRANSISTORS:
  - f_T = 3-5GHZ AT I_c = 2 MA
  - C_{CB} = 0.14 pf AT 0 VOLT
  - C_{CB} = 0.02 pf
  - β = 100-200
  - β_{MATCH} = 1 TO 2%
- RESISTORS:
  - CERMET THIN FILM 100 OHMS/SQ
  - PARASITIC CAPACITANCE<0.02-2Pf/MIL^2
  - TEMPERATURE COEFFICIENT <100 PPM/°C
  - MATCHING = 0.1 TO 0.5%
- INTERCONNECT:
  - TWO-LEVEL METAL INTERCONNECT

Table 2. Successive Approximation LSI Quantizers

SPEED (MSPS)	ACCURACY (BITS)	POWER (WATTS)
7	8	2.3
5	10	2.8
2	12	1.7
10	8	0.9
10	10	2.8
25	8	0.4

Table 3. 50 Msps 10 Bit Sample-and-Hold Performance

SAMPLING RATE	50 MSPS AT 10 BITS
ACQUISITION TIME	10 NSEC
SETTLING TIME	8 NSEC
POWER	1.2 WATTS
SIZE	1.75 X 1.3 INCHES
INPUT RANGE	±1.24 VOLTS
APERTURE TIME	>10 PSEC
LINEARITY	0.02%

Table 4. Monolithic Sample-and-Hold Performance

SAMPLING RATE	100 MSPS AT 10 BITS
LINEARITY	0.01%
ACQUISITION TIME	4 NSEC
SETTLING TIME	6 NSEC
APERTURE TIME	5 PSEC
BANDWIDTH	4 MHZ
POWER	0.7 WATT

Table 5. Projected Performance of Gallium Arsenide FET A/D Converters

A/D CONVERTER TYPE	SAMPLE	RESOLUTION	POWER	CHIP SIZE
SUCCESSIVE APPROXIMATION SUBRANGING (TWO STAGE) PARALLEL	70 MSPS 200 MSPS 2 GSPS	10 BITS 10 BITS 8 BITS	70W 300 MW 1W	60 X 60 MIL 110 X 110 MIL 200 X 200 MIL

Table 6. TED Bit Cell Performance

SAMPLE RATE	5 GSPS
APERTURE TIME	<5 PSEC
POWER	300 MW
CHIP SIZE	56 X 90 MILS

Table 7. Comparison of Four A/D Solid-State Technologies

TECHNOLOGY	ADVANTAGES	LIMITATIONS	POTENTIAL CAPABILITIES		STATE-OF-ART A/D CONVERTERS			COMMENTS
			SPEED AT 8 BITS	MAXIMUM ACCURACY (BITS)	MSPS	BITS	WATTS	
SILICON BIPOLAR TRANSISTORS	• HIGH ACCURACY (16 BITS) • HIGH SPEED (500 MSPS) • EXISTING LSI TECHNOLOGY	• MODERATE POWER • LSI SAMPLE AND HOLD DIFFICULT	500 MSPS	16	10 50 250 400	10 10 8 5	4 5 60 20	HIGHER SPEED A/D'S CAN BE MADE BY INTERLEAVING TWO OR MORE SLOWER UNITS, BUT THE REQUIRED TIME ALIGNMENT (0.36 DEGREE AT f IN MAXIMUM) USUALLY LIMITS ACCURACY, AND POWER CONSUMPTION IS OFTEN EXCESSIVE
GALLIUM ARSENIDE FET	• MEDIUM ACCURACY (10 BITS) • HIGH SPEED (1 TO 2 GSPS) • LOW POWER • MONOLITHIC SAMPLE AND HOLD	• TECHNOLOGY DEVELOPMENT REQUIRED	2 GSPS	10				BEST TECHNOLOGY FOR NEAR-TERM DEVELOPMENT (3 TO 5 YEARS) OF ADVANCED A/D CONVERTERS
GALLIUM ARSENIDE TED	• VERY HIGH SPEED (10 GSPS) • LOW POWER	• TECHNOLOGY DEVELOPMENT REQUIRED • LOW ACCURACY (6 TO 8 BITS)	10 GSPS	8	5000	1 (CASCADABLE CELL)	0.30	REQUIRED GaAs PROCESS THAT CAN PRODUCE FETs AND TEDs ON SAME LSI CHIP
JOSEPHSON JUNCTION	• VERY HIGH SPEED (50 GSPS) • LOWEST POWER • MONOLITHIC SAMPLE AND HOLD	• CRYOGENIC TEMPERATURES • TECHNOLOGY DEVELOPMENT REQUIRED	50 GSPS	8	62.5	4		NEEDS LIQUID HELIUM TEMPERATURE BUT OFFERS EXTREMELY LOW POWER LONG TERM DEVELOPMENT (10 TO 15 YEARS)

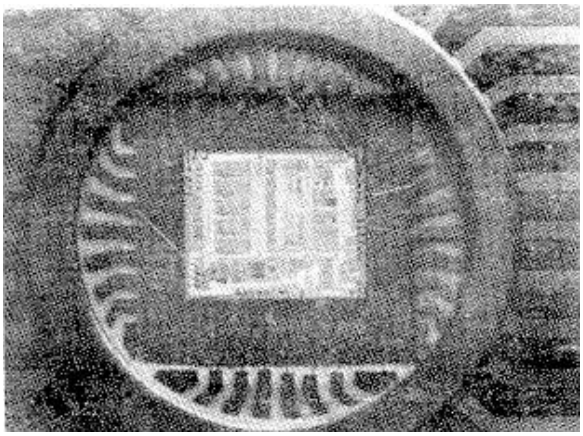


Figure 1. Packaged 2BQ Circuit

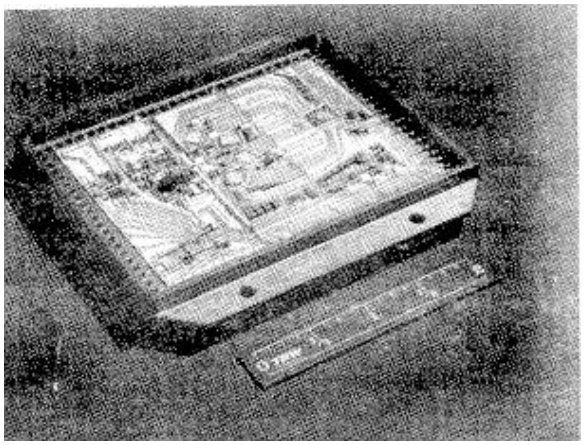


Figure 2. 400 Msps A/D Converter

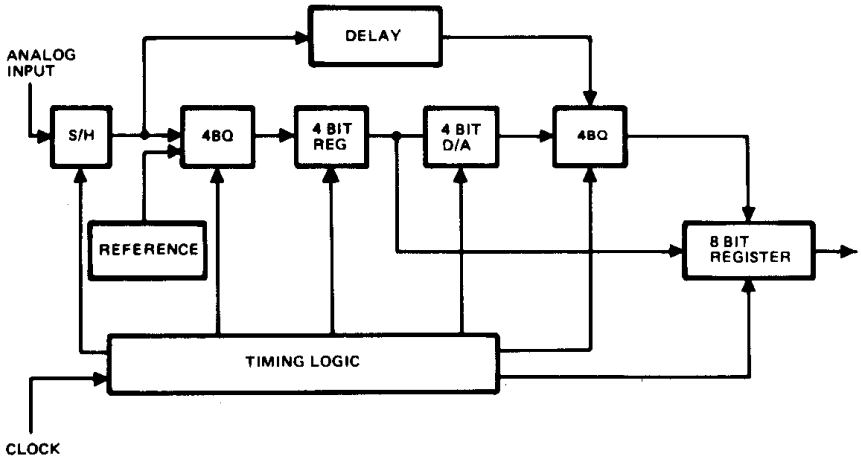


Figure 3. 8 Bit Subranging A/D Converter

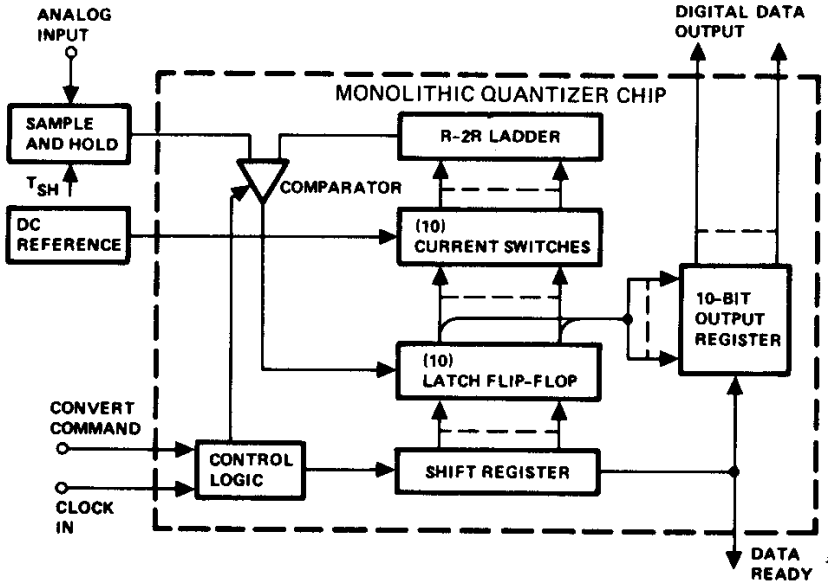


Figure 4 . Successive Approximation Quantizer Block Diagram

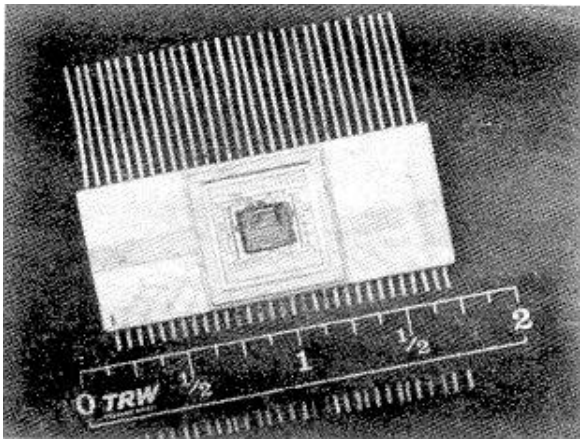


Figure 5. 10 Bit Monolithic Quantizer

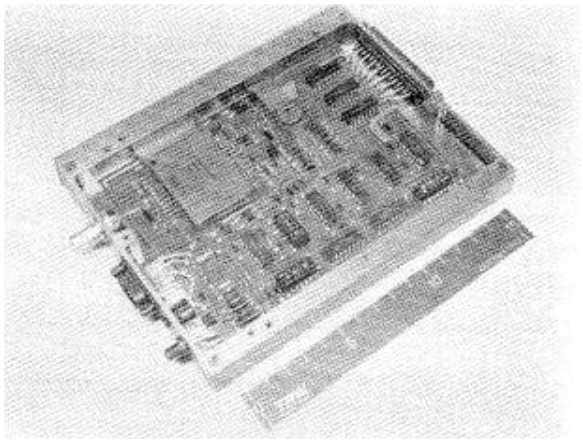


Figure 6 . 8 Bit Avionics A/D Converter

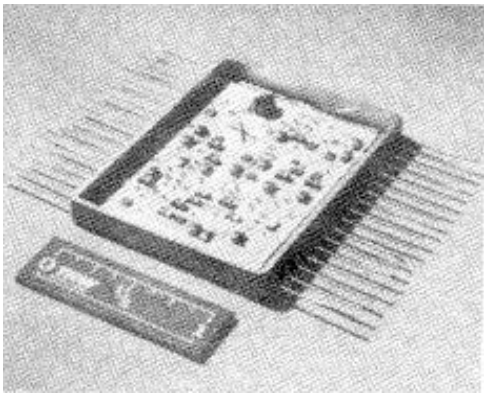
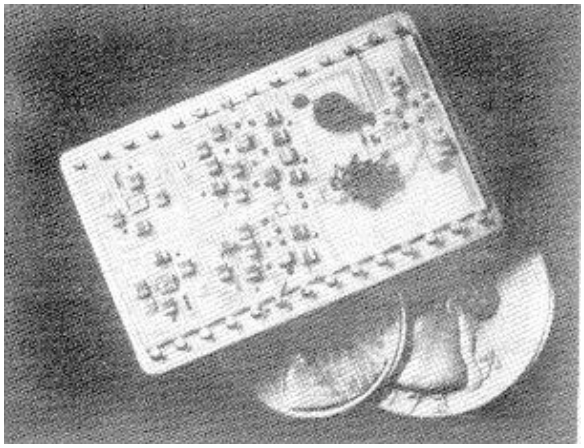


Figure 7. 50 Msps 10 Bit Hybrid Sample-and-Hold



Figu re 9. 400 Msps. 5 Bit Hybrid Sample-and-Hold

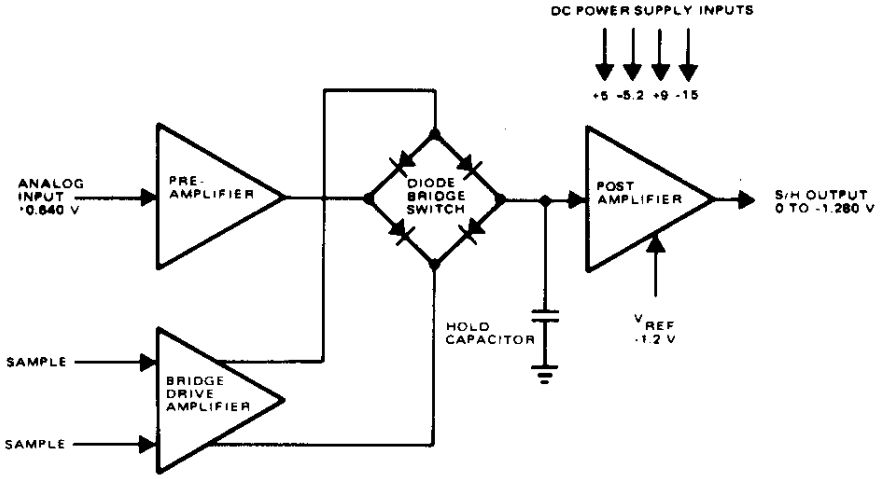


Figure 8. Hybrid Sample-and-Hold Block Diagram