

# **FET AMPLIFIERS FOR COMMUNICATIONS APPLICATIONS**

**W. Keith Kennedy, Jr.  
Vice President  
Devices Group  
Watkins-Johnson Company  
Palo Alto, California**

## **ABSTRACT**

The Field Effect Transistor (FET) is revolutionizing microwave communications with both its low noise performance and high dynamic range. This paper emphasizes developed amplifier hardware available today for both ground and satellite applications. The focus is on the noise figures and output powers available from 4 to 15 GHz.

## **INTRODUCTION**

Communication amplifiers divide relatively easy into either low noise amplifiers for receiver applications or power amplifiers for transmitter applications. At the present time, the Field Effect Transistors do not have sufficient output power to be the final amplifier within most transmitters. For this reason, FET's are still largely utilized to drive a TWT in the transmitting chain.

The Field Effect Transistor is unique where semiconductor devices are concerned in their ability to achieve low noise performance at a bias level that has a minimum of sacrifice in output power performance. This difference is particularly startling to design engineers who are familiar with silicon bipolar transistors. Many of the amplifiers designed using bipolar transistors have extremely low output powers when biased for minimum noise figure.

## **LOW NOISE APPLICATIONS**

Data for this application is shown in Figure 1 where the noise figure as a function of frequency is presented for several frequency bands. This data differs from that given within the paper by Fank<sup>1</sup> which is also part of this conference. The reason being that the data within this paper is on finished amplifiers that are commercially available and not on the transistor itself as was the case in the referenced paper.

Probably the most popular amplifier during the early applications of Field Effect Transistors to the communications field was the 1.5 dB noise figure amplifier in the 3.7 to 4.2 GHz band. When FET amplifiers first became available at a competitive price, the amplifier noise figures for this band were in the 2.0 to 2.3 dB range using an FET with a 1.0 micron gate length. But further improvements in the geometry of the FET produced smaller (0.5 micron) gate length devices, and along with higher production rates to permit sorting transistors for minimum noise figure, the 1.5 dB noise figure was reached. These 1.5 dB noise figure amplifiers were instrumental in reducing the antenna size and hence the cost of small ground station terminals. This particular type of amplifier has matured during the last two years so that it can be purchased with 50 dB gain in large quantities for about \$1,200. However, this has been but the first of the applications for Field Effect Transistor amplifiers within the communications field, and many other fully developed units are now available.

The higher frequency units shown in Figure 1 include both the ground station and satellite receiver applications as well as the troposcatter communications band. At the high frequency end of Figure 1, this data on developed amplifiers is again sufficiently above the 2.5 dB noise figure reported by Estabrook et al<sup>2</sup> on a single module at 14.5 GHz. The noise figure of a total amplifier using such an input stage would be 3.2 dB due to the input isolator loss and second stage contribution. The data within Figure 1 is representative of what can be purchased in large quantities at reasonable prices rather than state-of-the-art performance data.

One of the major emphases in the fabrication of Field Effect Transistors is the effort to reduce the gate width on these devices. As already mentioned, the reduction in gate length from 1.0 to 0.5 microns substantially lowers the available noise figure at 4.0 GHz. The devices utilized to set the noise figures of all the amplifiers in Figure 1 are of the 0.5 micron variety. This author predicts that within three years a 0.25 micron device will be available that will lower the amplifier noise figure obtainable at 14 GHz to 3.0 dB.

The dashed line drawn in Figure 1 is, at first glance, not compatible with the 1.5 dB noise figure for 3.7 to 4.2 GHz. This apparent inconsistency is due to the use of packaged devices at the lower frequencies. The package parasitics can be matched out at the lower frequencies without sacrificing gain flatness, phase linearity, VSWR and temperature stability. As the amplifier operating frequency rises to the 8 GHz range, these package parasitics become more difficult to compensate for. If only minimum noise figure was desired, better performance could be obtained. When other performance criterion are considered, most designs switch to unpackaged devices and higher noise figures result.

Many amplifier designers might disagree with Figure 1 and maintain that the change to unpackaged devices does not necessarily result in higher noise figures. This is true. What

really produces the higher noise figures is the higher cost of sorting an assembled amplifier stage as compared to a packaged transistor. The yield factor also enters into this equation. The author has placed a judgment factor upon the cost today's systems designer will pay for low noise performance. With higher usage in these bands, the ground station amplifiers will have reduced noise figures. The noise figures for satellite receiver amplifiers will not be reduced solely by higher usage however. This is because the screening requirements upon the semiconductor wafer to establish its pedigree again preclude a cost effective sorting of devices for minimum noise figure.

## **LOW NOISE AMPLIFIER ALTERNATIVES**

A Field Effect Transistor has several competitors in the low noise area with the parametric amplifier being far superior to the FET amplifier in terms of noise figure. For the ultimate in noise figure, the paramp is definitely the choice. However, the paramp cost may be as much as a factor of 10 above the FET amplifier. Size and weight considerations also heavily favor the FET amplifier with the uncooled paramp also being 10 times larger in each of these categories. One of the areas in which the Field Effect Transistor amplifier has been quite successful is in replacing paramps within the second stage of a two stage parametric amplifier. Because of the high dynamic range performance of the FET amplifier, typically 20 dB of improvement can be obtained in this area. Thus, this paramp-FET combination is a particularly good choice for increasing the dynamic range over a two stage paramp configuration while experiencing only a minimum degradation in noise figure because of the dominating effect of the paramp in the first stage.

The other competitor to Field Effect Transistors is the tunnel diode amplifier. These two amplifiers are comparable in terms of noise figure. The Field Effect Transistor is lower in cost, smaller and weighs far less. However, the tunnel diode amplifier is far from dead. In the important areas of limiting and AM to PM conversion, tunnel diode amplifiers are superior to the current Field Effect Transistor amplifiers. There are techniques being developed at the present time to produce Field Effect Transistor amplifiers with limiting characteristics that more closely match those obtainable with the tunnel diode. If these techniques can be refined over the next two years, the tunnel diode will then be in jeopardy of elimination from many satellite applications. The Field Effect Transistor does have the definite advantage of dynamic range with low noise devices having 20 dB greater output power than that obtainable from tunnel diode amplifiers.

## **DRIVER APPLICATIONS**

As mentioned in the introduction, a Field Effect Transistor is not yet available with 10 to 40 Watts of output power to be used as a transmitter. It is an excellent driver, however,

and because of its greater dynamic range than tunnel diodes, it does provide much lower intermodular distortion.

The output power capability of Field Effect Transistor amplifiers is shown in Figure 2 as a function of frequency. This figure shows the difference between ground applications and satellite bands because of the desire to derate performance in recognition of a conservative input power or chip operating temperature in satellite applications. Progress in terms of output power capabilities on Field Effect Transistors has been spectacular and perhaps even more rapid than the noise figure revolution. As an example, three years ago the Watkins-Johnson Company was selling bipolar transistor amplifiers for satellite drivers operating from 3.7 to 4.2GHz. This amplifier today should definitely utilize Field Effect Transistors and would increase the intermodulation performance by a minimum of 10 dB.

Again, as in the case of Figure 1, several amplifier designers might object that the output power levels shown in Figure 2 are too conservative. Ho, for example, has reported on an amplifier with +37dBm of output power for 3.7 to 4.2 GHz<sup>3</sup>. This amplifier would be very expensive for today's flight requirements, but in three years it could be feasible.

An unique advantage for the transistor amplifier designer that the power Field Effect Transistors have is that the impedance is easier to match to than bipolar devices with equivalent output power. This translates into less gain and phase variation as a function of frequency for the systems designer. Gain flatness  $\pm 0.1$  dB peak to peak per channel is typical for many satellite applications. Each of the curves in Figure 3 demonstrates this gain flatness. These amplifiers can be compensated for very stable gain as a function of temperature. For example, Figure 3 shows gain change as a function of temperature for an amplifier covering 7.9 to 8.4 GHz. The systems designer should be particularly aware of the need to compensate transistor amplifiers and should specify the amplifier compensation carefully. It is also necessary to realize this specification has a tremendous impact on the cost.

The FET amplifier is also an excellent performer in terms of phase linearity as shown in Figure 4. The FET amplifiers also have very low AM to PM conversions within their linear operating region. Once saturation begins, however, the AM to PM conversion becomes much larger than that normally experienced with tunnel diode amplifiers. To some extent this problem is circumvented by the FET driver amplifier's 30 to 40 higher dynamic range, but the tunnel diode is still supreme for limiting applications.

## **PACKAGING ADVANTAGE**

The FET amplifier does have a special advantage over the tunnel diode amplifier, especially when noise figure is not the driving requirement. That advantage is the ability to

design low VSWR amplifiers in very small stripline integrable packages such as shown in Figure 5. The input and output stages are balanced for low VSWR at a small sacrifice in noise figure. This type of amplifier can be dropped into higher level integration boxes without SMA connectors and used as distributed gain in 10 to 20 dB blocks. This author feels that the availability of such stripline compatible, low gain, high dynamic range building blocks will revolutionize RF designs for satellite applications.

## **RELIABILITY**

Field Effect Transistors have been tested extensively for their reliability performance. At the present time, amplifiers containing eight Field Effect Transistors have calculated MTBF's in excess of  $5 \times 10^6$  hours for satellite applications. Testing has occurred both at many manufacturers facilities as well as at independent laboratories.

## **FUTURE TRENDS**

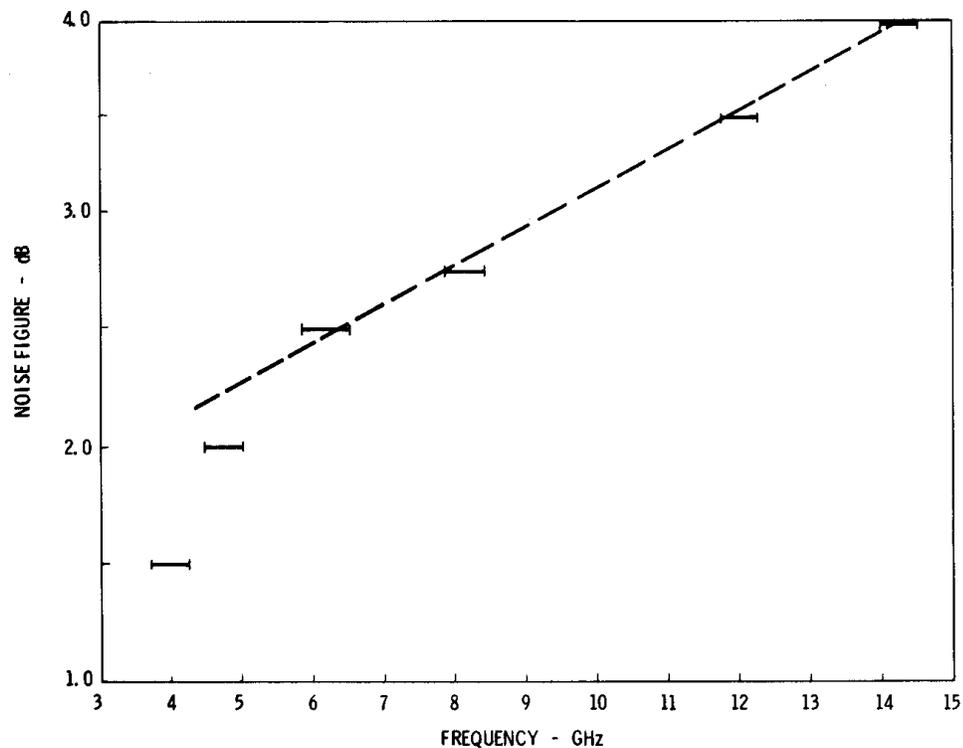
There are two major trends to FET development. The, first is the development of new fabrication techniques to lower the noise figures of the devices. This low noise work has concentrated in the area of smaller geometries and better contacting procedures. The second area in which device performance is being advanced is in improving the output power. While much of the multi-cell work already done on silicon bipolar devices can be extended to the Field Effect Transistor, some special techniques must also be developed. However, the major problem in increasing the output power of individual devices will be in solving the problems associated with conducting the heat away from the active layer of the Gallium Arsenide semiconductor chip. Flip chip bonding techniques are required for the next generation of power devices. A flip chip configuration is especially important as all three of the FET terminals are positioned on the upper surface of the chip. This compares to the bipolar transistor where one of the device's terminals is the substrate material. The substrate of a Field Effect Transistor is only a physical support for the active layer of the device and should not be placed between the thermal activity of the active region and the heat sink. Until one or more chip bonding techniques are fully evolved, commercially available chips will be limited to the few watt output power levels and the 10 to 20 Watt chips will remain a laboratory phenomena.

## **ACKNOWLEDGMENTS**

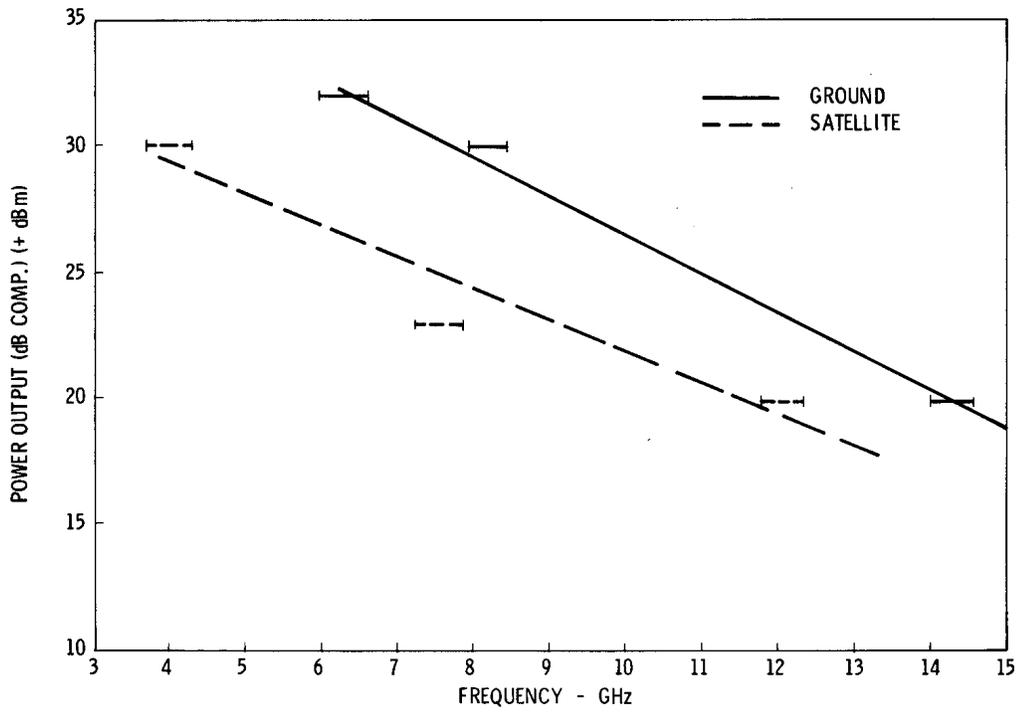
The author wishes to acknowledge several discussions with both P. Estabrook and S. Livingston on the general area of FET communication amplifiers and especially their comments on the specific subjects discussed herein.

## FOOTNOTES

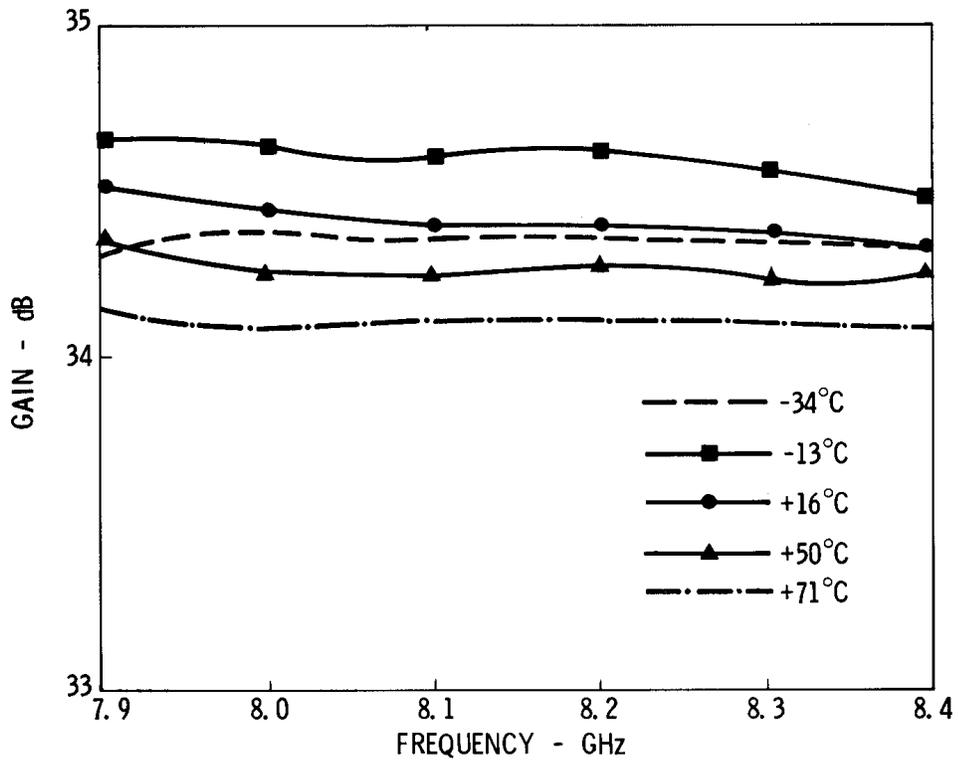
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2. P. Estabrook, C. M. Krowne, E. J. Crescenzi, Jr. and R. E. Stegens, "A Low Noise Single Ended GaAs Schottky FET Amplifier for a 14 GHz Satellite Communications Application", 1978 IEEE MTT-S, Ottawa, Canada, June 28, 1978.
3. P. T. Ho, "A 7 Watt C-Band FET Amplifier Using Serial Power Combining Techniques", 1978 IEEE MTT-S, Ottawa, Canada, June 28, 1978.



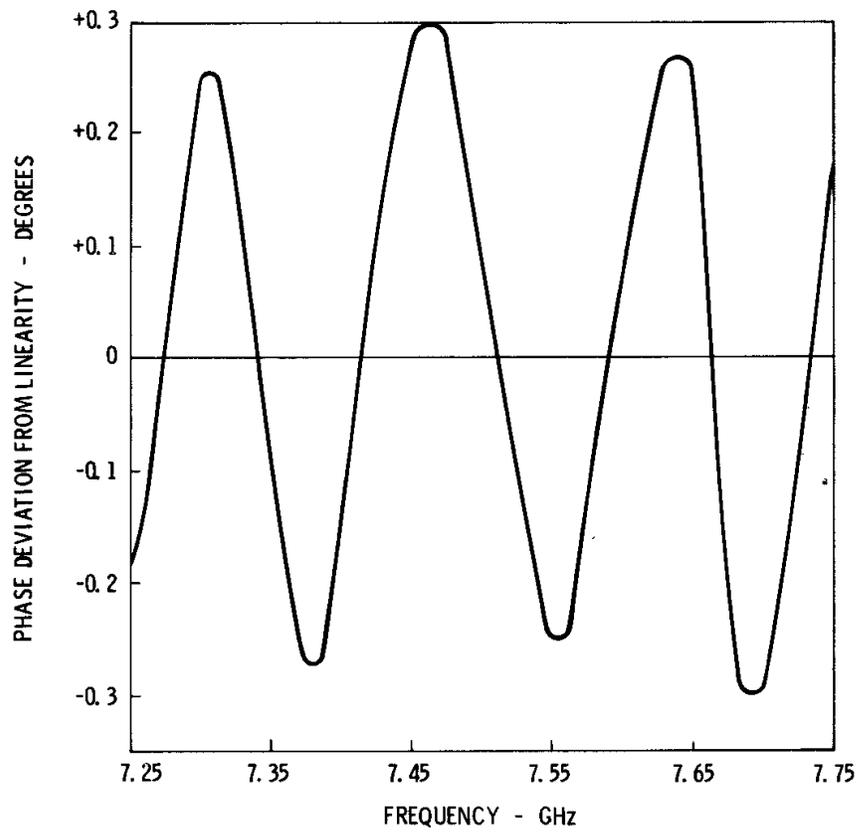
**Figure 1 - Commercially Available Noise Figure as a Function of Frequency for Communication Applications**



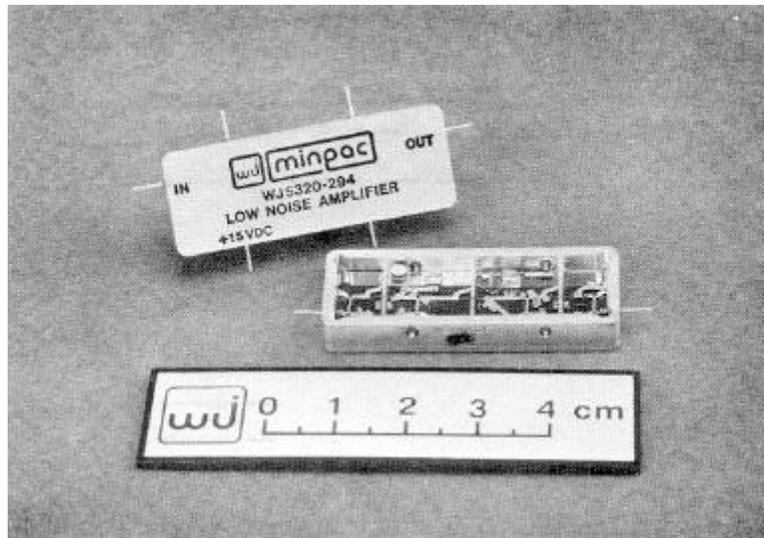
**Figure 2 - Readily Available Output Power as a Function of Frequency for FET Communication Applications**



**Figure 3 - Gain as a Function of Frequency and Temperature for a Low Noise Satellite Amplifier**



**Figure 4 - Phase Deviation From a Linear Response for a Satellite Driver Amplifier**



**Figure 5 - Stripline Compatible FEI Amplifier**