MNOS SPACECRAFT RECORDERS

J.E. Brewer
Westinghouse Electric Corporation
Baltimore, Maryland

ABSTRACT

MNOS memory components are well suited for use in spacecraft recorders. Recorder design considerations and MNOS chip requirements are reviewed, and projections for 10^8 and 10^9 bit recorders are presented.

INTRODUCTION

Metal-nitride-oxide semiconductor (MNOS) technology can be used to fabricate large scale integrated devices which provide nonvolatile read and write data storage. Present day integrated circuits can meet some recorder needs. With the development of higher bit densities per chip, the possibility of general purpose 10^8 and 10^9 bit capacity recorders is very real.

The purpose of this paper is to examine the potential of MNOS for realization of spacecraft recorders. The requirements of the recorder application are restated as reported in the literature. The nature of MNOS memory is briefly reviewed. Some of the considerations important to recorder unit design are discussed. Finally, the characteristics of 10^8 and 10^9 bit recorders as implemented with MNOS chips of different storage capacity are summarized.

INTRODUCTION

The shortcomings of magnetic tape recorders have motivated serious attempts to find a viable alternative memory. Tape recorders have a poor reliability history on U.S. spacecraft. These units tend to fail catastrophically rather than degrade gracefully.

Tape systems are difficult to apply properly. The designer must contend with long start and stop times. Only serial operation is possible. The bit rate is uneven because of wow, flutter and jitter. The presence of rotating parts must be considered to avoid affecting the angular momentum of the spacecraft. The motor employed must be examined for electromagnetic interference. Recorder packaging and testing can be rather complex.

A solid-state unit would of course avoid all of these problems. Consideration has been given to construction of recorders using CCD components or magnetic bubbles. The storage density, nonvolatility, low power dissipation, and relative radiation hardness of bubbles has generally caused a preference for bubbles over CCD. MNOS devices have all the advantages of bubbles, but are easier to package, simpler to interface, and allow much more design flexibility.

RECORDER REQUIREMENT

Reference [1] reported on a survey of recorder requirements for future U.S. spacecraft missions. Capacity needs tended to cluster at about 10^8 bits. A few missions were projected as needing 10^9 bits. The authors concluded that a "standard" recorder design of 10^8 bits would meet roughly half of future program requirements. From the characteristics of existing tape recorders, they proposed a set of target specifications which are competitive with tape units and meet a large percentage of potential user needs.

bit capacity	10^8 bits
record rate	10^5 bits/second
playback rate	10^8 bits/second
power	20 watts (worst mode)
weight	10 pounds
volume	800 cubic inches

Data rates and recorder usage will of course vary with the mission. In earth orbit a recorder would typically accumulate data slowly during the orbit. When the spacecraft passes a ground station the data would be read out rapidly for transmission to earth. Therefore, the recorder might be written only once per orbit. For a 1.5-hour orbit period, the memory would be written 16 times a day. Over a six-year period the accumulated write cycles would be about 35,000.

MNOS TECHNOLOGY

Present day MNOS technology has achieved the level of maturity necessary to allow the construction of reliable memory systems. The state of the art can best be communicated by reviewing the elements of a suitable memory device. These include the MNOS memory transistor, the storage cell, and the integrated memory chip. The MNOS technology, like all integrated circuit technologies, is advancing rapidly, and it is important to consider near-term growth possibilities.

MNOS nonmemory transistors are similar in form and function to the well known MOS transistor, except that the insulator region is composed of two dielectric layers. As shown

in figure 1, a nonmemory transistor gate structure typically consists of 800 angstroms of oxide (SiO_2) under 450 angstroms of nitride ($Si_3 N_4$).

The dual dielectric transistor can be used for nonvolatile storage of information. When the oxide layer is made very thin (≈21 A), it becomes possible to electrically insert or remove charge from traps in the nitride close to the nitride-oxide interface. When power is removed, the charge will remain within the insulator for very long time periods.

A change in the quantity of charge in the insulator will cause a corresponding change in threshold voltage of the transistor. For binary information storage the threshold voltage is shifted or switched into two distinguishable levels. The most positive threshold level places the transistor in the high conduction (HC) state, and the symbol V_{HC} is often used to describe that state. Similarly, the most negative threshold is a low conduction (LC) state, and it is usually symbolized as V_{LC} .

Figure 2 shows a cross section of a drain source protected (DSP) memory transistor [2], and presents a schematic symbol equivalent circuit diagram. The middle symbol represents the memory transistor associated with the thin oxide region. The arrow on the gate identifies the variable nature of the threshold voltage. The symbolized gaps between the source, substrate and drain imply enhancement mode operation (for the illustrated structure, this is not completely true because the HC state can be depletion mode). The transistor symbols on each side represent nonmemory transistors associated with the thick oxide regions.

The thick oxide serves to protect the thin oxide from stress associated with material imperfections and/or electric fields. The p-channel enhancement mode nonmemory transistors determine the high conductance state of the overall DSP structure, and therefore, the DSP device is confined to enhancement mode operation. This is an important issue in that it allows the device to be readily interconnected into large arrays without having to contend with difficult parasitic current problems.

Many models of memory device operation have been presented in the literature, and the general phenomena involved are reasonably well understood. The models in general are not adequate to account for all facets of device behavior. Usually the transistor structures are designed for charge transfer between the silicon and traps in the nitride by direct tunneling. It is possible that both electron and hole conduction occurs. The nitride traps are believed to be distributed in both energy and space. The tunneling oxide is a complex layer with ill-defined transitions from silicon to oxide and from oxide to nitride.

In an integrated memory device, a memory transistor will be subjected to pulses of prescribed amplitude and duration in order to shift between V_{HC} and V_{LC} . The threshold

voltage magnitude after a given pulse depends on the pulse response characteristic of the transistor and the initial threshold voltage. A small time after the threshold voltage has been switched it begins to decay. For times on the order of a year the voltage decay is linear with the logarithm of time.

After a transistor has been subjected to about 10^8 switching cycles, changes begin to occur in the pulse response characteristic and in the decay rate. In the literature, the ability of a transistor to withstand cycling is referred to as "endurance." The endurance rating of a device is stated as the number of accumulated erase-write cycles which can be tolerated before it is probable that memory cell operation would be affected. Reference [2] gives a discussion of the factors involved in endurance, and presents data which indicates that 10^{10} cycles can be tolerated with ±20-volt, 100-microsecond pulses and still achieve 2,000 hours retention.

The endurance of a transistor depends on proper control of electric field strengths and the properties of the dual dielectric structure. Control of the nitride thickness is an important factor, and the advent of low pressure chemical vapor deposition (LPCVD) of the nitride has significantly improved production uniformity. Endurance ratings will vary from manufacturer to manufacturer because of processing and geometry differences. Ratings will vary from application to application even for a given manufacturer because the device stress levels may be different.

Commercial manufacturers making devices intended to be alterable read-only memories have set endurance ratings as low as 10^5 cycles. Manufacturers for the military making BORAM type devices have set ratings of 10^7 or 10^8 cycles. Military RAM type devices using nonsaturated pulse conditions can achieve 10^{12} cycles. Since a typical spacecraft recorder might accumulate 35,000 cycles in six years, the endurance of MNOS is more than adequate for the application.

The thin oxide memory transistor has been found to be a very hard structure. Memory in MNOS devices can survive an accumulated dose of 10^8 rads (Si) independent of dose rate [4] [5] [6].

The MNOS technology has long been recognized as having the potential for very high bit density, and recent circuit designs are beginning to achieve this goal. Figure 3 shows a conventional MNOS two-transistor cell used in an 8,192-bit BORAM device. Two-transistor cells with differential detection circuitry are used as a means of ensuring high yield and adequate retention in the presence of normal process variation. Four masks are used to form the cell and alignment is not critical. No contact windows exist in the cell. All of the features are stripes. The two transistors are entirely independent in that each has a separate source and drain diffusion.

A more advanced cell design appears in figure 4. Here a polycrystalline silicon layer has been added to allow column switching. In this design, adjacent transistors can share p+ diffusions, and the spacing between columns is eliminated. Using these dimensions, one can build 0.5-mil^2 two-transistor cells or 0.25-mil^2 one-transistor cells.

As changes in circuit geometry and process sequence are introduced and proven, MNOS cell sizes will shrink dramatically. The MNOS cell is simpler than that required for CCD or MOS structures [7]. Present day cells will allow fabrication of economically viable 16K- or 32K-bit chips. In the future, the bit density will exceed 131K bits.

A variety of MNOS memory circuits are currently available from several suppliers. Most of these devices were intended for use as electrically alterable ROM. For the recorder application, it is more efficient to use a BORAM (block-oriented random-access memory) organized chip. BORAM devices allow simplification of control circuitry, simplification of addressing, and an increase in recording rate without a power penalty.

The Westinghouse BORAM 6008, shown in figure 5, is an example of this type of circuit. As shown in figure 6, the chip contains a 256-word by 32-bit RAM and a 32-bit shift register. All I/O takes place serially through the shift register. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32bit latch.

The RAM and the shift register operate independently. High bit rates may be maintained at the I/O terminals while the RAM need operate at only 1/32 of the external rate. If a record rate of 10^5 bits/second is desired, the time available for processing 32 bits would be 320 microseconds. Because the write time per 32-bit row is on the order of 200 microseconds, the speed of the chip is adequate for the recorder application. In practical recorder circuits it is likely that more than one chip would be enabled to receive data, and thus even higher recording rates are easily achieved.

To achieve the desired packaging densities and radiation hardness, some further chip development work is necessary. The BORAM chip mentioned above will operate after 3 x 10^4 rad (Si). With circuit changes, the tolerance can be increased to about 10^5 rads (Si) and 10^{10} rads/second transient. Achievement of these goals has recently been demonstrated on a part made using processing similar to the BORAM device [8].

RECORDER DESIGN CONSIDERATIONS

Recorder design is to a large extent dictated by the nature of the memory component. The choice of MNOS BORAM gives considerable freedom in both electrical and mechanical design. Because of the basic nature of an MNOS part, some very advantageous design strategies are possible.

The nonvolatility of MNOS allows the recorder design to achieve low power and high reliability without giving up performance. A given MNOS device need not be powered up except for the small time interval when it is to be used in a data transaction. In a recorder this might mean that only one or two chips are ever active. For the entire storage section of a recorder, the power requirement while writing or reading may be made to be less than a watt.

Because of the use of power switching, the normal environment for a memory chip in the recorder would be the powered down mode. This condition greatly enhances chip reliability [7] because of the great difference between active chip failure rate and dormant chip failure rate. An active chip has voltages applied and electric field stresses exist within the chip. A dormant chip has all voltages removed and electric field stresses within the die are greatly reduced. The failure rate of a dormant MNOS chip may be conservatively estimated as one-tenth that of an active chip.

This natural reliability advantage can be further enhanced by the use of some form of redundancy. Because of the serial flow of data and the desire for low power, probably the most appropriate scheme is to divide the storage into a number of modules. For the memory to be considered fully functional, in modules out the n modules are required to be operational. Designs of this type can achieve 0.999 reliability at three years with approximately 20 percent device redundancy.

The MNOS memory component eliminates some of the design limitations that are associated with magnetic bubble devices. An MNOS chip can operate over the full military temperature range of - 55°C to + 125°C. The data signals to and from an MNOS part are at normal integrated circuit logic levels. Special sense circuits are not required. Data is stored in addressable arrays. There is no rotating shift register to keep track of or to control. Of course such items as bias magnets, rotating field coils, and field driver circuits do not exist. Data access and timing is not constrained by rotational latency. Power switching circuitry must deal with only small amounts of current working into noninductive loads.

Packaging an MNOS memory system is much easier than packaging a magnetic bubble system [7]. At every modular level within the systems there is much less to package in an MNOS unit. Figure 7 shows the hybrid circuit package currently being used for MNOS BORAM chips. Note that this 1- by 2-inch hybrid contains 16 chips. At the comparable modular level a bubble system would have to include memory chips, preamplifiers, X and Y field coils, and bias magnets. At the card level and system level, this trend continues because circuitry and components are required to control the magnetic fields which do not exist in the hybrid.

From a packaging point of view, a solid-state recorder can be divided into a storage section, a control section, a power supply, and a cable entry section. The storage section consists of some arrangement of memory components and essential interface circuitry which is replicated to achieve the required storage capacity. The volume required for the control, power supply, and cable connectors does not vary significantly with storage capacity. Therefore, the volume of a recorder can be computed as some fixed volume plus the volume associated with a single memory card times the number of memory cards.

In comparing MNOS and bubble packaging, the volume required per memory chip in the storage section and the bit density per chip are the important factors. The 10^8 bit bubble recorder projected in [1] required 7.78 cm^3/chip in the storage section. An MNOS recorder needs only 1.77 cm^3/chip in the storage section. In this case the bubble chip must contain five times more bits than the MNOS chip to maintain volumetric parity.

The number of bits per chip is the parameter which determines the viability of a solid-state recorder. Table 1 compiles the number of chips required to 10^8 and 10^9 bit recorders for various chip capacities. Obviously, the larger the number of bits per chip the better the packaging situation. For a 10^8 bit recorder, a 16,384-bit chip allows achievement of a recorder volume less than 800 cubic inches which [1] claimed to be competitive with tape recorders. The use of 32,768 bits/chip and larger will provide a significant packaging advantage over tape. To compete with bubble packaging the MNOS die must be at least one-fifth the size of the bubble die. A 65,536-bit MNOS chip can provide denser packaging than a 262,144-bit bubble chip.

RECORDER DESIGN EXAMPLES

MNOS recorder design involves a number of tradeoffs which can significantly alter the characteristics of the memory system. In the examples which follow, performance in terms of record and playback rate was held to the target goals in order to minimize power. The MNOS component is capable of much higher performance, but this feature was deemed to be of no value for this application.

Power dissipation is determined by the efficiency of the supply, the power required for control logic, and the power in the storage section. As a worst assumption, it is assumed that the supply is only 50 percent efficient. Control logic power depends on the choice of the integrated circuit technology. The low operating speed will allow the use of CMOS. In some cases, bipolar circuits will have to be used to accomplish level shifting. Maximum dissipation associated with control circuitry is less than 1 watt.

The storage section consists of MNOS memory chips, driver and buffer circuits, and power switching circuits. Sixteen MNOS chips are packaged in hybrid circuits similar to

that shown in figure 7. Sixteen hybrids are placed on a memory card that measures 6 by 8.5 inches. Therefore, a memory card contains 256 chips. During recorder operation, only one card is addressed at a time, and two chips on that card are powered up. Dissipation from those two chips during the worst operating mode is approximately 0.7 watt. The dissipation in the associated drivers, buffers, and power switches is less than 1 watt. Total storage section dissipation is less than 1.7 watts, and does not vary with the addition of more memory cards.

The total recorder dissipation is seen to be less than (1 + 1.7) x 0.5 or 5.4 watts. The power dissipation remains within this limit whether the recorder contains 10^8 or 10^9 bits.

Table 2 summarizes the parameters for 108 bit recorders implemented using four different MNOS chip sizes. The designs are compared against the target parameters suggested in [1]. All of the recorders are identical in capacity, bit rates, and power. They differ in weight and volume. It appears that even a 32K-bit chip can provide volumetric efficiency greater than the 125,000 bits per cubic inch target. The designs range from 219,298 bits per cubic inch for a 32K-bit chip up to 606,060 bits per cubic inch for a 262K-bit chip.

Weight predictions fall short of the design target until a 131K-bit chip is used. In each case, the packing density was assumed to be 1.15 grams per cubic centimeter.

Table 3 presents similar data for 10^9 bit recorders implemented using three different chip sizes (in this case, the storage capacity was taken as 2^{30} bits which is 7.4 percent greater than 10^9 bits). The smallest chip considered feasible for construction of this size of memory was 65K bits. Redundancy would definitely be employed to ensure reliability in the presence of a large component count. Bit rates and power are identical with the 10^8 bit recorders. Weight and volume are small enough to allow serious consideration of the systems on a spacecraft.

The use of MNOS BORAM devices allows the recorder to be used as an addressable device rather than just a serial unit. For the recorder design examples, it was assumed that the host system would specify a starting block address. Reading or writing would then continue in a serial fashion from that point in the recorder.

When larger MNOS chips are employed, the cost per bit becomes quite low. System prices in the range of 0.01 cent per bit to 0.03 cent per bit can be achieved as the product matures.

CONCLUSIONS

The MNOS technology has the potential of providing superior cost effective recorders for use in spacecraft. The achievement of that potential depends on the availability of larger bit capacity chips. The prognosis for achievement of larger chips is good, and MNOS recorders can be expected to emerge in the early 1980 time frame.

REFERENCES

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[8] J. Fagan, P. Smith, D. Barth, and T. Shutt, "1 Kilobit Radiation Tolerant AROM," *Government Microcircuit Applications Conference (GOMAC*, Nov 14-16, 1978.

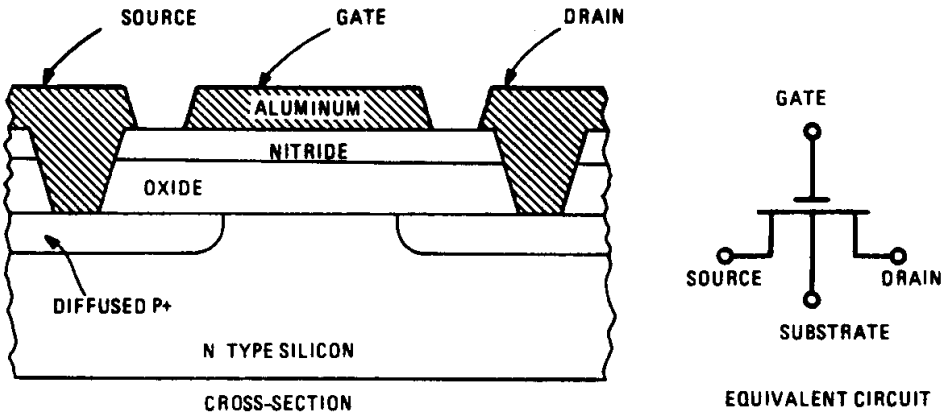

Figure 1. MNOS Nonmemory Transistor

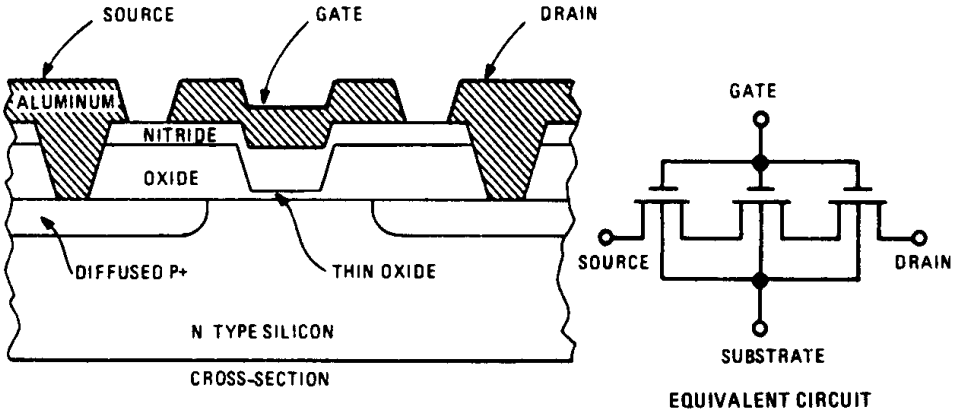

Figure 2. MNOS Drain Source Protected Memory Transistor

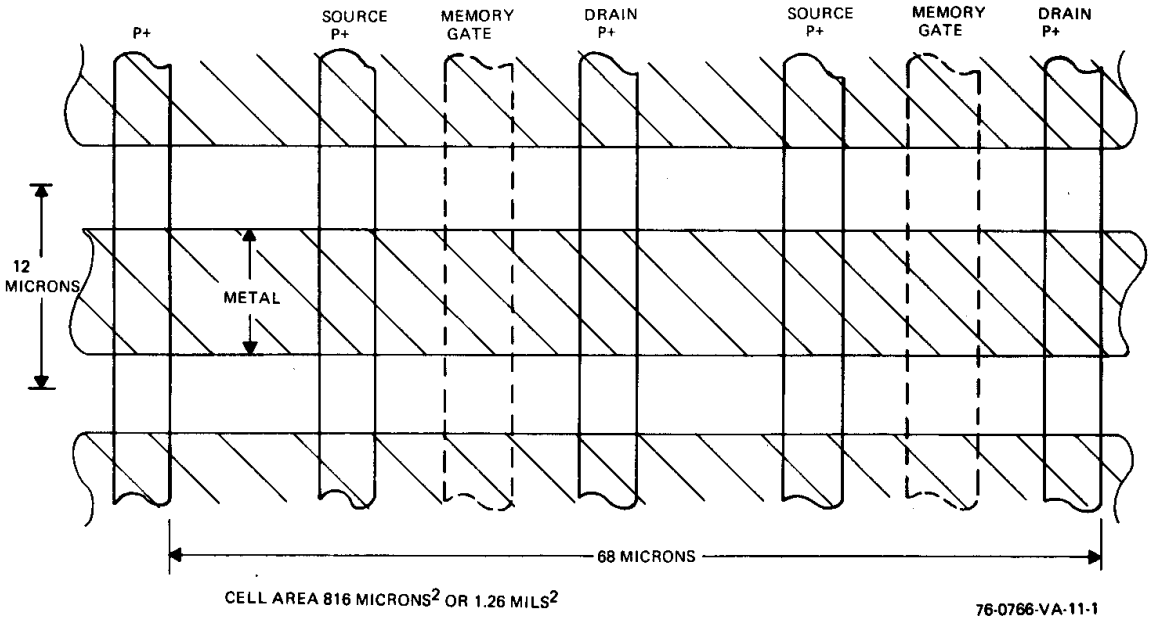

Figure 3. An MNOS Two-Transistor Cell of Conventional Design

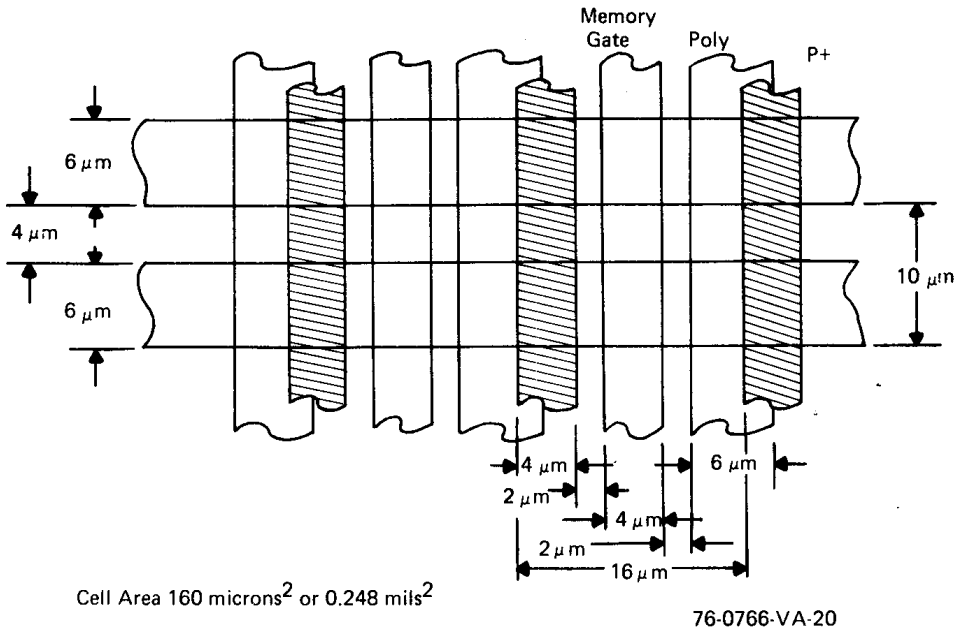

Figure 4. MNOS Single Poly Layer Cell

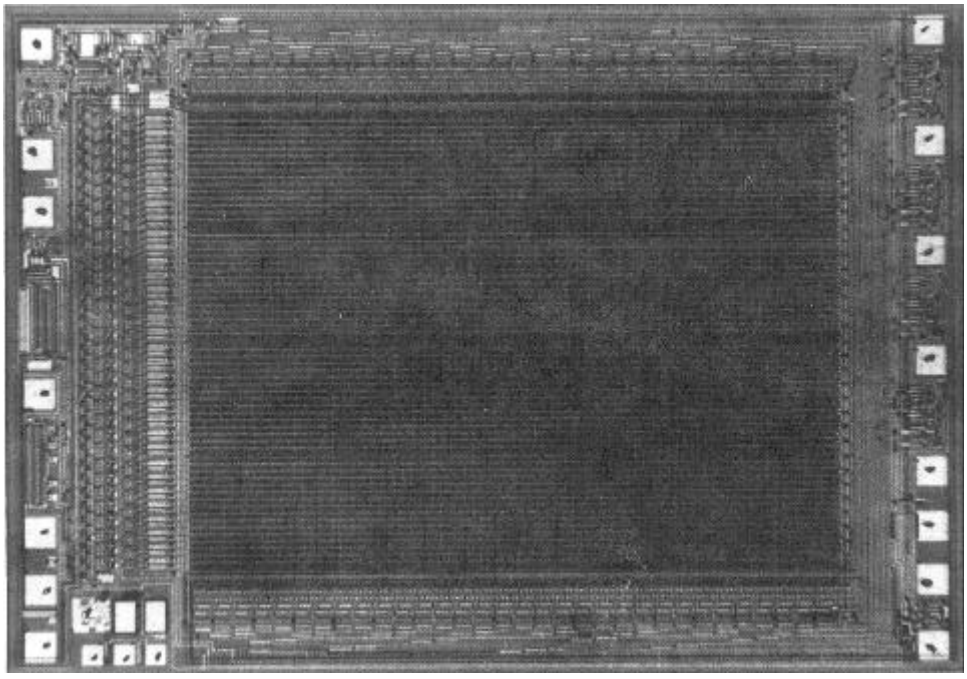

Figure 5. BORAM 6008 Die

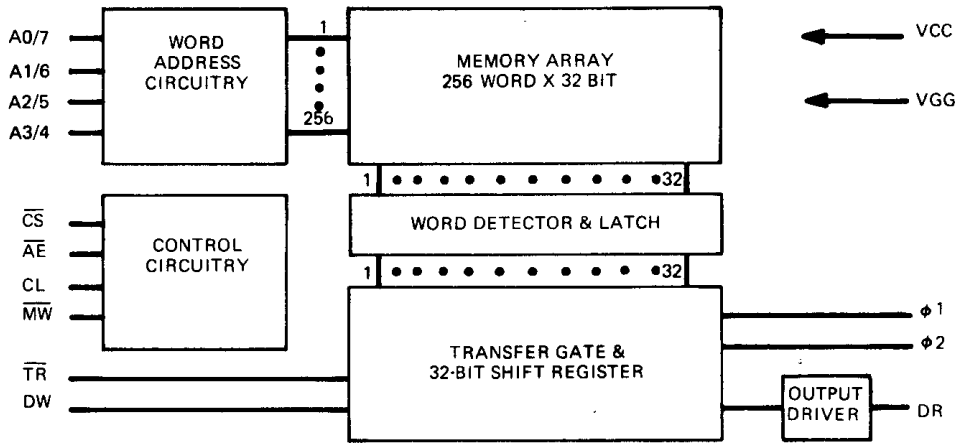

Figure 6. BORAM 6008 Functional Block Diagram

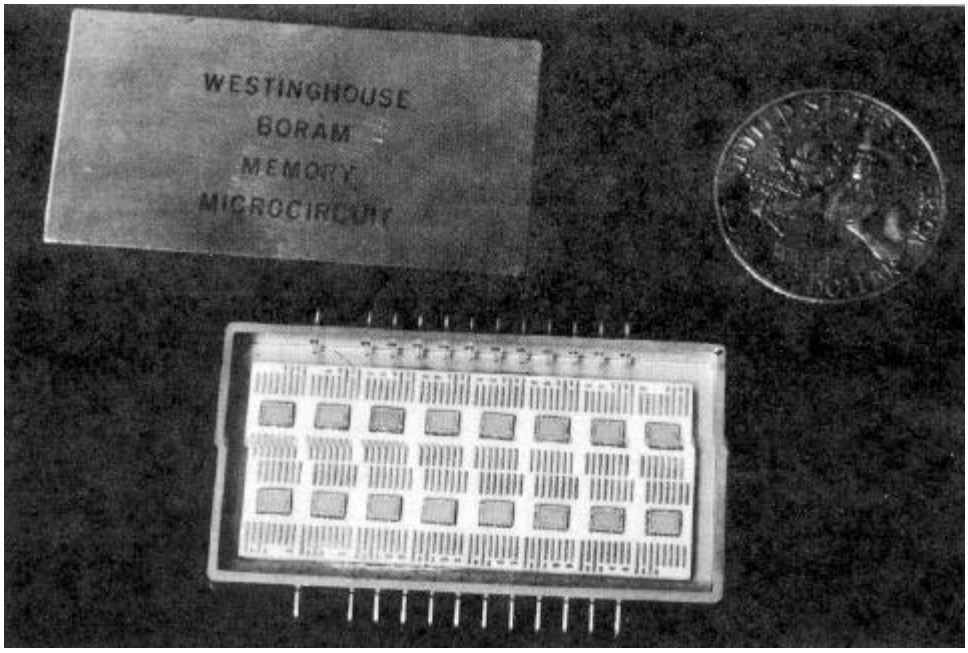

Figure 7. BORAM Memory Microcircuit - Westinghouse Part 647R527G01

TABLE 1
CHIP REQUIREMENT FOR 10^8 AND 10^9 BIT RECORDER

Bits/Chip	Number of Chips Required with No Redundancy	
	10^8 Bit Recorder	10^9 Recorder
8,192	12,288	131,072
16,384	6,144	65,536
32,768	3,072	32,768
65,536	1,536	16,384
131,072	768	8,192
262,144	384	4,096

Chip requirement projection uses $3 \times 2^{25} = 100{,}663{,}296$ as $\approx 10^{-8}$ and $2^{30} = 1{,}073{,}741{,}824$ as $\approx 10^9$

TABLE 2
10^8 BIT MNOS RECORDER DESIGN PROJECTIONS

Characteristic	Design Target	MNOS 32K Bit Chip	MNOS 65K Bit Chip	MNOS 131 K Bit Chip	MNOS 262K Bit Chip	Units
Bit Capacity	10^8	10^8	10^8	10^8	10^8	Bits
Record Rate	10^5	10^5	10^5	10^5	10^5	Bits/Sec
Playback Rate	10^6	10^6	10^6	10^6	10^6	Bits/Sec
Power	20	5.4	5.4	5.4	5.4	Watts
Weight	10	19	12	9	7	Pounds
Volume	800	456	290	206	165	Inches^3

TABLE 3
10^9 BIT MNOS RECORDER DESIGN PROJECTIONS

Characteristic	MNOS 65K Bit Chip	MNOS 131K Bit Chip	MNOS 262K Bit Chip	Units
Bit Capacity	10^9	10^9	10^9	bits
Record Rate	10^5	10^5	10^5	bits/sec
Playback Rate	10^6	10^6	10^6	bits/sec
Power	5.4	5.4	5.4	watts
Weight	79	42	24	pounds
Volume	1897	1010	567	inches^3