

A SOLID STATE DATA RECORDER FOR SPACECRAFT TELEMETRY APPLICATIONS

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ABSTRACT

A Solid State Data Recorder (SSDR) has been developed which offers a high reliability alternative to tape recorders in many spacecraft telemetry applications. The storage medium used in this recorder was ferrimagnetic garnet films supporting nonvolatile magnetic "bubble" domains. This technology is very flexible and permits a recorder design which can simplify much of the interface with the telemetry system. The recorder was designed using modular construction consisting of a Digital Control Unit (DCU), Power Supply, and two Memory Modules.

The Digital Control Unit (DCU) is made up of four independent microprocessor controlled data channels, configuration control, and a telemetry and test interface. The configuration can be programmed so that the SSDR can operate as a 1, 2, or 4 serial channel recorder, or a single 8-bit parallel channel configuration. Each channel has a complete command set and can operate independently of the other channels. Details of the system organization and operational characteristics are presented.

The Memory Module was designed with 32 magnetic assemblies, or cells, each containing 16 serial 102.4K bit magnetic "bubble" memory chips. Sense and operator electronics, and field coil drive electronics are also located in the memory module.

A prototype SSDR has been fabricated. This prototype is designed for 10^8 bits of storage but was populated with 128 chips for a 1.3×10^7 bit capacity. Preliminary tests indicate satisfactory operation. Results of these tests are presented and variations with designed characteristics discussed.

INTRODUCTION

Data storage is one of the most important functions in a spacecraft telemetry system whether it be mass data storage, because data transfer links are inadequate, buffer storage to regulate the flow of data, or transient storage to permit processing of data prior to transmission. The most cost effective method currently available to perform these functions is magnetic tape recording.

It has been recognized for some time that tape recorders are failure prone and significantly reduce the system reliability of the spacecrafts. Additionally, the operational characteristics of tape recorders placed constraints on the design of the telemetry system. For these reasons, NASA Langley Research Center has investigated magnetic "bubble" domain technology as a potential alternate to tape recording in spacecraft telemetry systems. This investigation has led to the development of a 10^8 bit Solid State Data Recorder (SSDR) and the fabrication of a prototype for system evaluation.

In a previous paper, Howle² presented a general description of the system. In this paper, the general system is reviewed briefly, detailed design considerations discussed, and preliminary test data presented.

GENERAL SYSTEM DESCRIPTION

The Solid State Data Recorder is an approximately square box which is 12.7 by 12.8 inches on a side and 4.7 inches thick. This box weighs 43 pounds and is conductively cooled through the base plate and into the spacecraft structure. It is modularly constructed and consists of a Digital Control Unit, Power Supply, and two Memory Modules.

The characteristics of the SSDR were summarized by Howle² and are presented in Table 1.

TABLE I
SSDR CHARACTERISTICS SUMMARY

Storage Capacity	1.04 x 10 ⁸ bits
Size	760 in ³
Weight	43 pounds
Configuration	
Serial-Programmable	1, 2, or 4 channels
Parallel-8 bit	1 channel
Max Data Rate	
Each Channel	1.2 M bits/sec

Total	2.4 M bits/sec
Power (1 channel, 10K bits/sec)	13.7 watts
Operating Temperature	-10° C to +60° C
Nonoperating Temperature	
No loss of data	-40° C to +85° C
With loss of data	-50° C to +125° C
Predicted MTBF	41,000 hours

This recorder was designed to meet typical spacecraft mechanical environments of vibration (sine 10 to 15G, Random .4 G²/Hz), shock (20 G), acceleration (50G) and thermal vacuum (10⁻⁵ torr, -10° C to +125° C).

When describing a system design, it is often difficult to follow how each component fits into the system. Figure 1 is a component matrix which identifies the various SSDR subassemblies. This paper follows Figure 1 in that it starts with the Memory Device and works up through each level and finally describes the total system.

MEMORY DEVICE

The bubble memory device is fabricated using a (Y, Sm)₃ (Ga, Fe)₅ O₁₂ garnet film. A diagram of the memory device is shown in Figure 2. The chip dimensions are approximately 6 mm on a side. The bias field (nominally 100 oe) is directed out of the plane and the rotating field (nominally 52 oe) rotates clockwise. The rotating field starts and stops along the 0° or S/S direction. The rotating field must be brought to operating value or zero within an angular tolerance of ±15° and undershoot must be held to less than 1 oe. An inplane holding field of 4.3 oe is required to stabilize the bubble rest position.

The propagate structure is a 16 micron T-bar pattern with approximately 2 micron line widths and 0.9 micron spacings. The bubble diameter is approximately 4 microns. The inside corners are T - x and the outside corner are bent H. The detector is a 100 element stretch with a sensitivity of about 1 mv/ma.

The memory device is organized into a single closed serial loop. An annihilator is directly inserted in the loop. The generator is located outside the loop but a propagate path allows the generated data to propagate and merge into the storage loop. Data are transferred out of the loop by a passive replicator. Since the transfer is by replicate, the data also remains in the storage loop and is nonvolatile. The detector and generator propagate paths lengths are chosen so that read, write, and erase occurs in the same period. The phasing of the operator currents are as shown in Figure 2.

The choice of a serial organization over a major/minor loop is difficult and becomes less clean as devices with 8 microns periods or less become available. The primary arguments against the choice of a serial organization are yield and access time.

In a major/minor loop organization, one can allow for faulty loops by a software work around using a simple controller. By including a number of redundant loops, the total capacity of the device can be maintained. Strong evidence has been presented by Singh³ demonstrating the yield improvements by allowing 1, 2, or more faulty minor loops. Our experience has indicated that the yield of serial devices is actually much greater than expected. Although yield improvement is always needed, the system advantages of the serial loop outweigh the increased yield in a recorder type application.

The primary disadvantage is loss of access time which is not an important consideration in a data recorder application. Advantages of the serial device are the simplicity of the interface with a buffer used in a synchronous operation and the ability to operate in the incremental mode. Other advantages include fewer leads and a simpler controller.

MEMORY CELL

The key unit in the recorder is the memory cell. The mechanical design of the memory cell was described by Becker⁴. Eight (8) of the magnetic memory devices are mounted on a ceramic carrier along with the sense matrixing diodes. Two of these carriers, a drive coil set (X coil and Y coil), and the bias structure make up the cell. A photograph of the cell is shown in Figure 3.

The bias magnets are used to establish the static field to center the operating point in bias margin. The chip carriers are tilted with respect to the bias field to generate the inplane holding field. Within the bias structure, there is a small perturbing field coil which is used to determine the operating point and perform margin testing. Once determined the strength of the bias magnets are adjusted to center the operating point.

The memory device is fabricated with a requirement that the operating margin be greater than 10 oe at room temperature. The chips are matched so that the combined 16 devices have approximately 6 oe margin at room temperature to insure adequate margins from -10°C to +60°C.

The drive coils are a pair of orthogonally wound coils as shown in Figure 4. The X coil is opened at the ends to permit insertion of the carriers. A set of ferrite keeper plates are used to increase sensitivity (oe/amp) and confine the rotating field to the cell area. Copper plates are placed in the coils to reduce the vertical component of the rotating field. Currents are induced in the plates by the vertical component of the rotating field which

tend to keep the field horizontal. Measurements of coil properties were made at 150 KHz and in a resonant circuit. Typical values of key parameters are shown in Table 2.

TABLE 2
TYPICAL DRIVE COIL PROPERTIES

AT 150 KHz	X AXIS	Y AXIS
R_{ac} (ohms)	1.5	1.0
Q	11.0	19.0
L (μ H)	19.0	21.0
Sensitivity (oe/amp)	18.0	19.0

DATA STORAGE SUBSYSTEM

The Data Storage Subsystem (DSS) consists of two Memory Modules interconnected by a dual bus system through which the Digital Control Unit (DCU) can obtain access to an appropriate Memory Module. Any one of the four channel controllers in the DCU can obtain access to either or both Memory Modules through either the A bus or B bus. Access to a particular module is determined by the configuration control.

Each bus has a set of enable, timing, address and data lines. These buses are shown as inputs to the memory module in Figure 5. The address lines are 5 bits parallel and selects one of 32 memory cells in the memory module. The data lines are 4 bit parallel bidirectional. The enable line controls the power distribution and the timing and control provides synchronization for the data transfer and coil drive and operator electronics.

Matrixing of circuits to minimize parts count and power strobing were used where feasible. All parts used were either space qualified or qualifiable. All parts were derated using MIL-STD-975 (NASA), Appendix A. Figure 6 is a diagram of the Memory Module mechanical layout. The 32 memory cells are arranged in 4 rows of 8 along either side. In the center there are the Sense Operator Board and the Coil Drive Board. Sixteen (16) coil drive matrix Electronics Boards are mounted on top of the memory cells. The total volume of this module is 227 in³ and weighs 13.8 pounds.

The Coil Drive is a nonresonant circuit generating a trapezoidal current waveform. The primary factor leading to the nonresonant circuit is to reduce parts count and the need for a low impedance switch to stop the rotating field within the memory chip overshoot and angle tolerances. Additionally, operating a serial chip in the stop/start mode in conjunction with an input buffer requires first bit detection. With the rotating field off, the stripe about

to enter the detector will collapse into a bubble. The drive circuit must provide a charging time to allow time for the bubble to strip out before entering the detector.

The sense channel configuration is shown in Figure 7. The resistors shown in Figure 7 are the active and dummy detectors on the memory chip. The differential potential on the sense bus is a function of the component mismatch, detector resistance change due to the presence of a bubble, and the charging time. For this reason, component match is critical and the bus capacitance must be kept to a minimum.

Initially, the bridge current is turned on to allow charging of the sense bus. Approximately 1.25 microseconds later the sense amp input is undamped allowing it to charge. The differential input is sampled for about 50 nanoseconds to determine the state of the detector.

Sixteen (16) such circuits are paralleled to detect the output of the 16 memory chips in each cell. The particular cell is determined by the state-of the cell sense select switches.

Similarly, the generator circuits are matrixed over 32 cells and determined by the cell generate select. The generator control circuits are also 16 wide to permit writing a 16 bit wide word into the memory chips located in the memory cell. The data on generator and sense lines are transferred to or from a 4 bit wide bidirectional bus at the interface. The annihilators of the memory cell are in series to permit simultaneous erase.

DIGITAL CONTROL UNIT

A detailed command list was described by Howle² and will not be repeated here. Basically, all commands appropriate for a tape recorder are available. In addition, a set of interrupt commands (go to read(X), go to write (X)) permits quick access to a given cell. There is also provided a set of skip commands which restricts access to a particular cell. The interrupt commands will override the skip command such that a given cell can be either eliminated if faulty or protected if critical data are stored. If critical data are stored in a particular cell (X) then the skip cell (X) command will take cell (X) out of the available memory for all routine data storage. Access to that cell can be obtained only by a go to read (X), go to write (X) which overrides the skip (X) command.

A block diagram of the Digital Control Unit is shown in Figure 8. The heart of the system is four independent smart controllers. Each controller contains a Rockwell PPS-8 microprocessor, two 2K by 8 bit read only memories (ROMS) for control firmware, and 256 by 8 bit PMOS random access memory (RAM) for status and variable storage. The PPS-8 was chosen because it is PMOS and has a superior radiation tolerance. A 512 bit core memory is available to provide nonvolatile status storage. In the core memory, data

such as previous mode, read pointers, and write pointers are stored to permit total power shut down or recovery from a power failure.

Each channel is totally independent such that multiple operations can be performed. This permits each implementation of operations such as data rate buffering.

EXPERIMENTAL PROCEDURE

One of the memory cells was subjected to mechanical sine vibration per MIL-STD-810B, Method 514. Data were stored in the memory cell prior to vibration and read out afterwards. One of the memory devices showed a degradation of the upper bias margin. Inspection of the cell showed no mechanical damage, however, small particles were observed on the chip. Removal of these particles returned the bias margin to its original level. It was postulated that the particles were debris from the scribe and bread operation and were causing distortion in the local fields. This postulate was verified by inducing similar failures with garnet particles placed on the chip surface. To correct this failure mode the chip surface was perfected with 1/2 mil mylar preforms which remove surface contamination away from the magnetic surface. Vibration tests were then repeated and demonstrated that memory devices were adequately protected. This change was made in the chip design used in fabricating the prototype.

A complete prototype of the Solid State Data Recorder has been developed. All electronic multilayer boards were fabricated and evaluated. All mechanical assemblies were fabricated. This prototype was then populated with 8 memory cells or 128 memory chips. Figure 9 is a photograph of the completed prototype.

The Solid State Data Recorder was tested over the various configurations and modes. Operational parameters such as power were found to be within design tolerance. In testing, two problems were demonstrated. First, the high temperature operation was limited to less than 40° C. Second, typical error rates were of the order of 10^{-6} errors per bit, which was higher than the program objective of 10^{-3} errors per bit.

DISCUSSION

A review of the system design indicated that the problem was in the memory chip design. A test chip was fabricated with the following modifications. The material used to support bubbles was changed from gallium substituted to calcium germanium substituted garnets. The passive replicator was changed to an active replicator and the detector was changed to a side by side dual detector with alternate bit detection. Preliminary tests on this chip indicate sense margin was adequate for a 10^{-9} error per bit at the detector level.

In addition to the above detector changes, the asymmetric chevron propagate structure was incorporated to increase yield. Based on these changes and the related data, we have concluded that the temperature and error rate problems are solved.

In a redesign of the memory cell two changes would be made first, the drive coils would be made symmetrical with the carrier and both the carrier and drive coils would be tilted with respect to the bias field. This would reduce the system power. Second, a cell containing 8 chips would be used. This is also a power consideration since it would make the peak power and average power closer and make a higher efficiency power supply design possible. Additionally, the matching of memory chips in groups of eight would be easier and provide overall improvement in cell level bias margins.

In a redesign of the memory module, a reduction in the size of the sense matrix would be recommended. Basically the capacitance of a 32 memory chips long sense bus is too great to permit proper charging within the sense window.

With the design improvements discussed, a solid state data recorder has been developed which is suitable for spacecraft applications.

ACKNOWLEDGEMENTS

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I would also like to thank the people at Langley for their preliminary designs, supporting experiments, and hardware testing at every level of development. Particular mention is due Paul Hayes, Ronald Gorten, Charles Nichols, and William Howle.

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	SSDR CONTAINS	MODULE CONTAINS	CELL CONTAINS	DEVICE CARRIER CONTAINS	MEMORY DEVICE CONTAINS
MODULE	2				
CELL	64	32			
DEVICE CARRIER	128	64	2		
DEVICE	1024	512	16	8	
BITS	1.04×10^8	5.2×10^7	1.6×10^6	8.2×10^5	102 400
	SSDR	MEMORY MODULE	CELL	CARRIER	MEMORY DEVICE

FIG 1 SSDR COMPONENT MATRIX

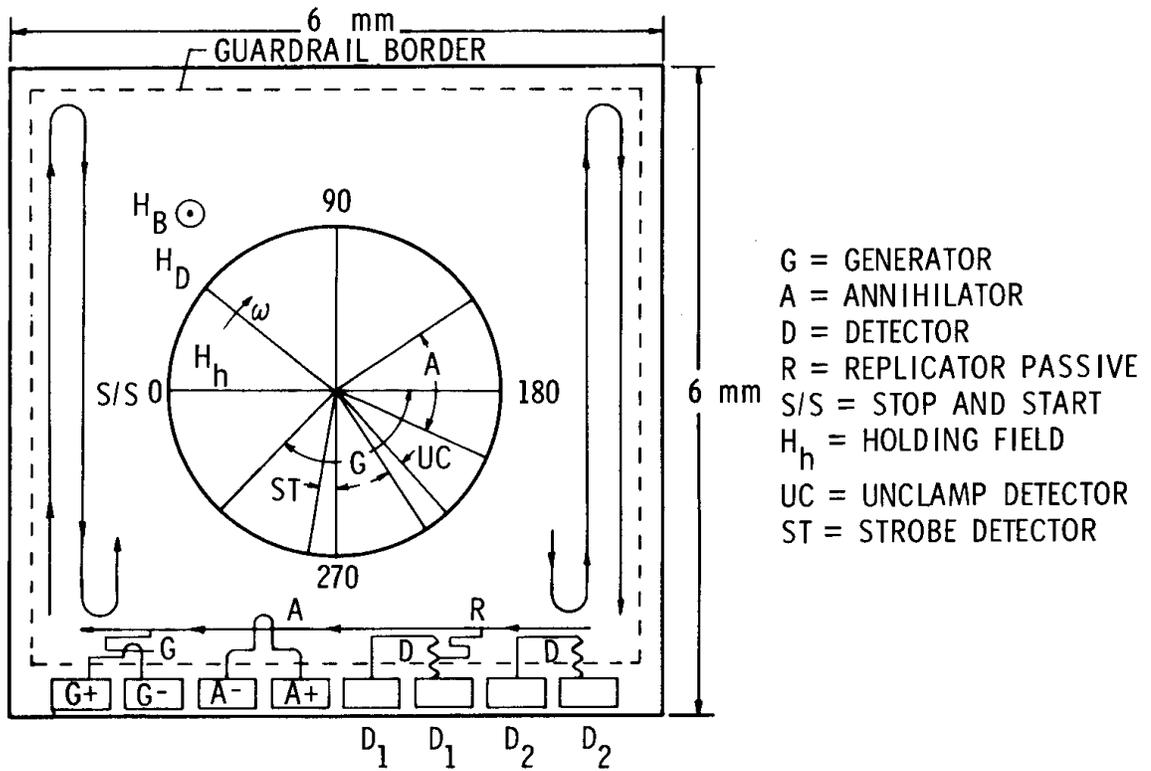


FIG 2 MEMORY CHIP SCHEMATIC

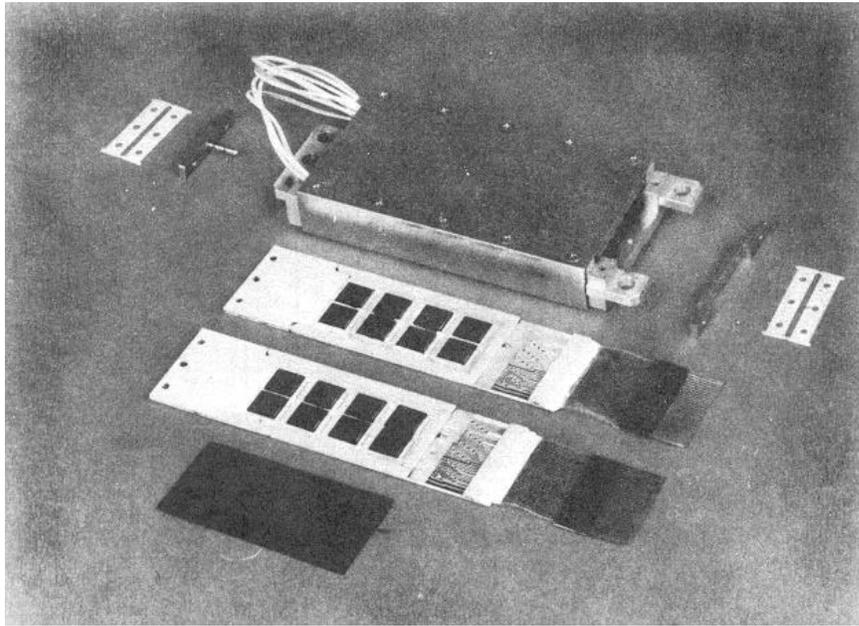


FIG 3 MEMORY CELL PHOTOGRAPH

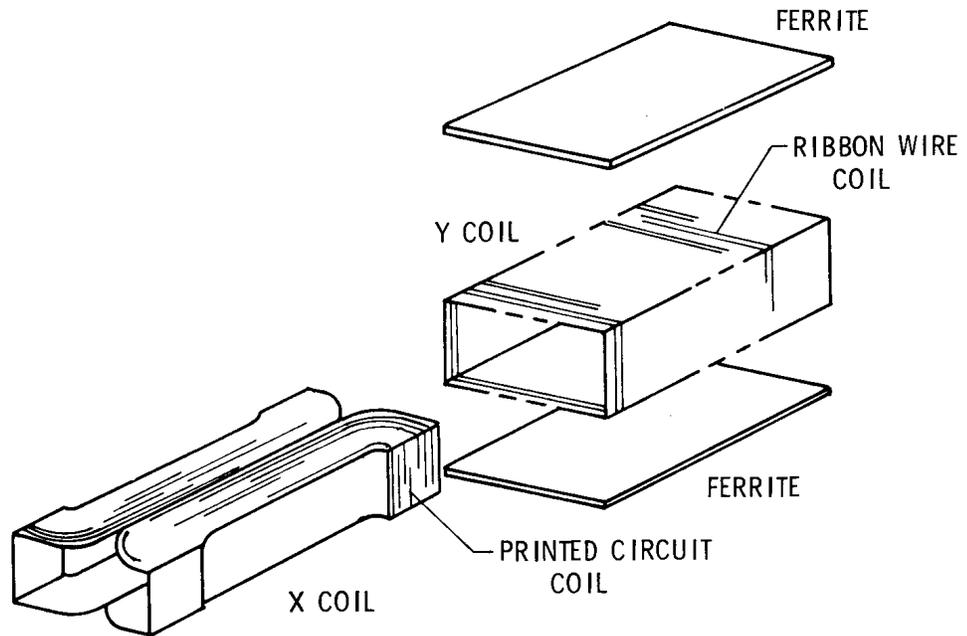


FIG 4 MEMORY CELL COIL DESIGN

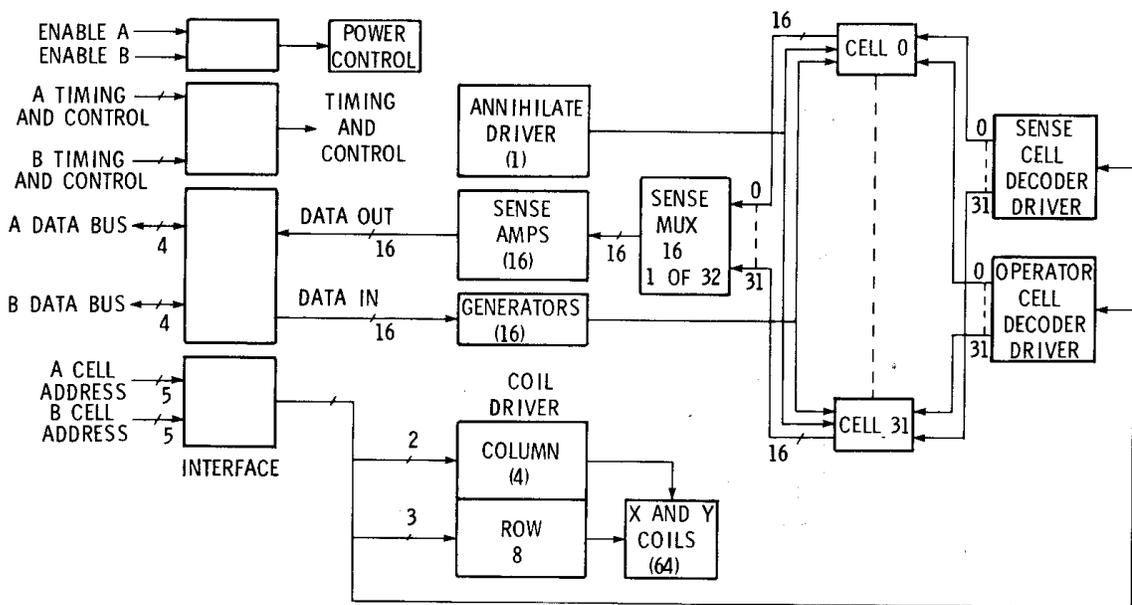


FIG 5 MEMORY MODULE BLOCK DIAGRAM

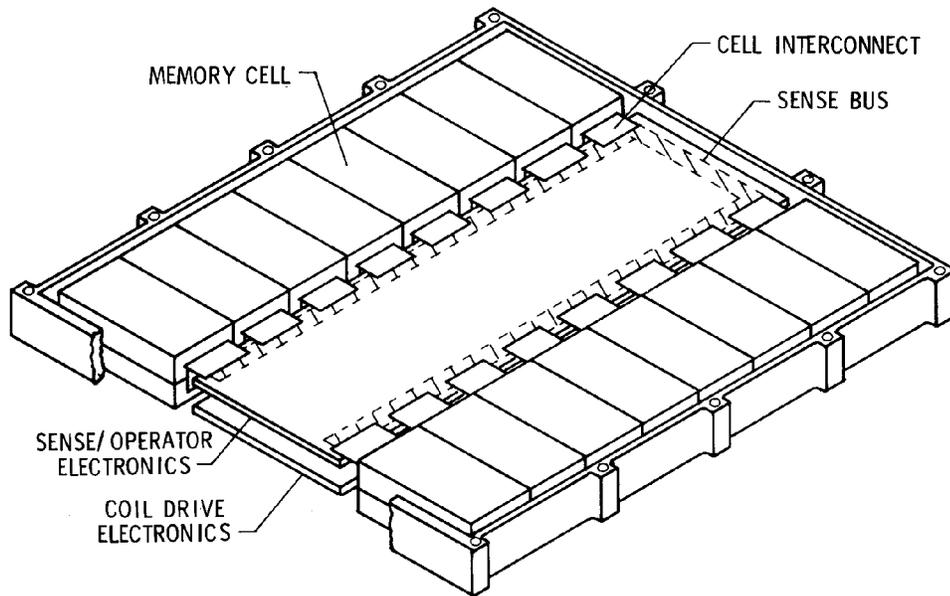


FIG 6 MEMORY MODULE

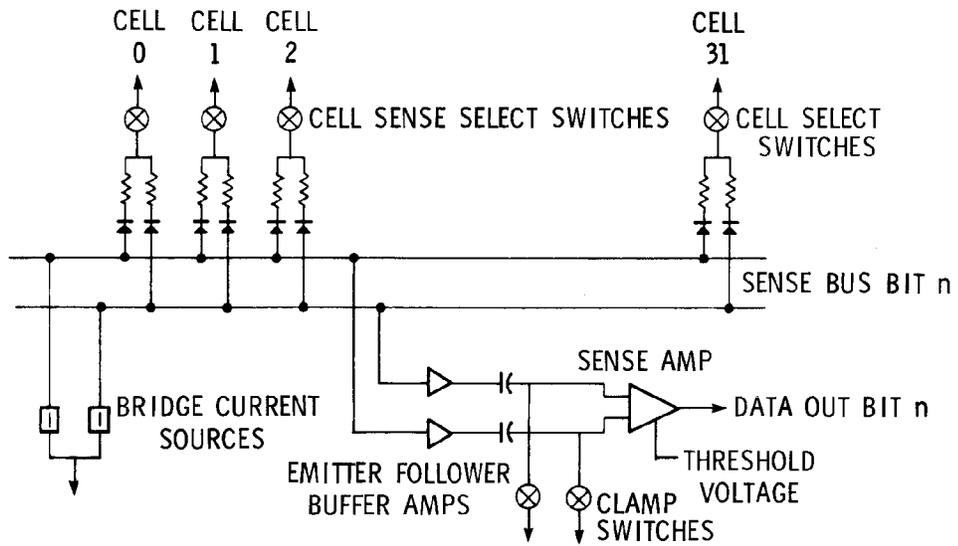


FIG 7 SENSE CHANNEL CONFIGURATION

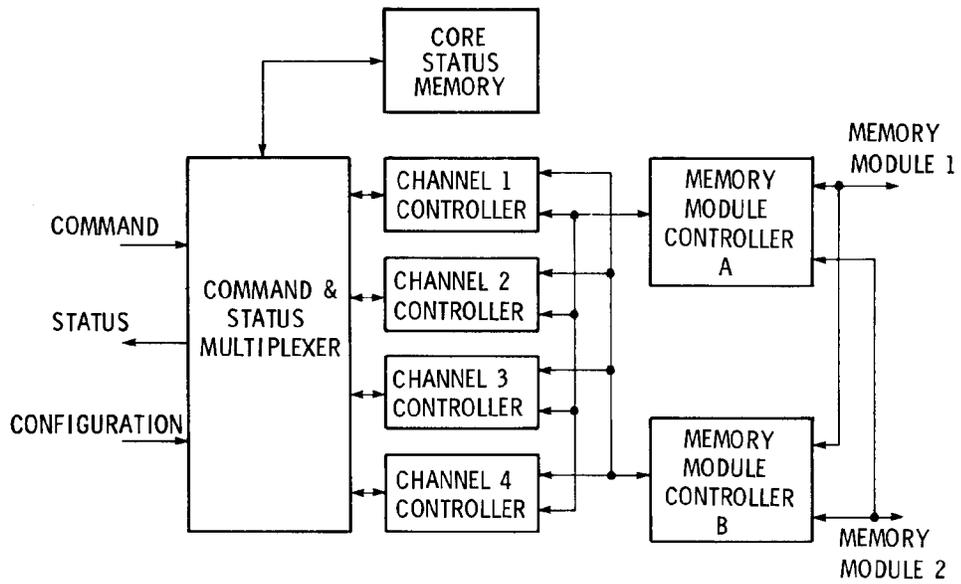


FIG 8 DIGITAL CONTROL UNIT BLOCK DIAGRAM

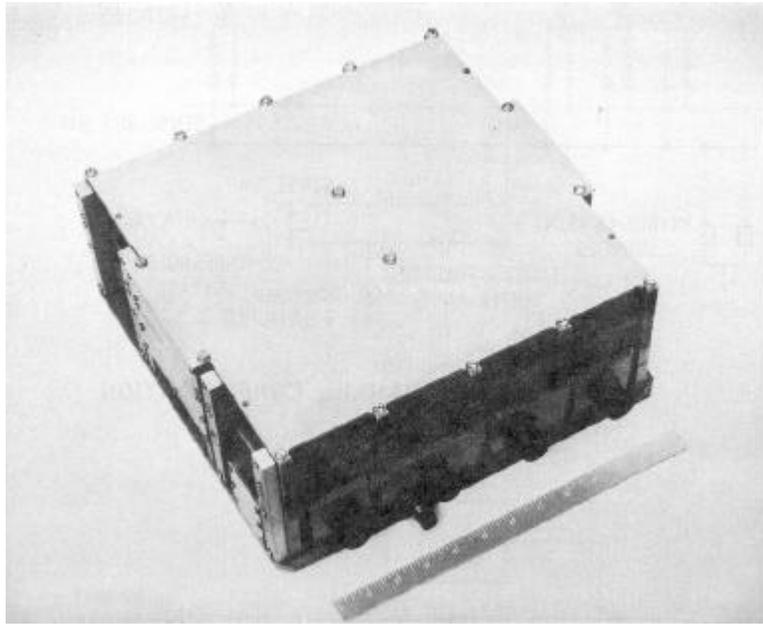


FIG 9 SOLID STATE DATA RECORDER PHOTOGRAPH