

AN EXTENDED PHASE -LOCK TECHNIQUE FOR AIDED ACQUISITION

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ABSTRACT

In a phase-locked PM demodulator, the input signal is modulated by a periodic waveform, particularly when the loop bandwidth is less than the sideband to carrier spacing, and thus discrete sidebands are apt to appear about the carrier frequency. This frequently results in a sideband locking instead of phase-locking to a selected carrier and aided-acquisition is then required. Conventional techniques such as discriminator-aided-acquisition have been implemented by Mostrom¹ and Victor et al.² to correct this problem, however, this approach necessitates a large carrier to noise ratio (CNR) in the bandwidth of the discriminator. The current study describes a novel approach to extend the threshold for a phase-locked loop designed for Hartman Systems' telemetry receiver. By phase remodulating the error signal, the network reduces the phase swing of the signal and restores the carrier power so as to provide anti-sideband properties for biphase and PM modulation up to 1.3 radians deviation at all modulation frequencies and at a signal level where CNR is greater than 5 dB above PM threshold.

INTRODUCTION

A conventional phase locked loop consists of a phase detector (PD), a loop filter and a voltage controlled oscillator (VCO). In this loop (illustrated in Figure 1), the input intermediate frequency (IF) signal with a phase of $\Theta_i(t)$ is transmitted into a phase detector of which the gain factor is K_d (in volts per radian). A typical K_d for a double balanced mixer used as a phase detector is approximately 0.5 v/radian. The VCO outputs a signal with a phase of $\Theta_o(t)$, which is compared against Θ_i by the phase detector. The output voltage from the PD, V_d , is then filtered by the loop filter. When the loop is locked, the PD is linear and V_d can be expressed as $V_d=K_d(\Theta_i - \Theta_o)$, i.e., the PD output voltage is proportional to the phase difference between the IF input and VCO output signals. Frequency of the VCO is determined by the controlling voltage, V_c , generated by the error sensing integrating amplifier embedded in the loop filter. The level of this controlling voltage is linearly proportional to the frequency deviation, $\Delta\omega$ from the center frequency with a gain factor K_o .

Using the above type of circuitry for phase demodulator applications, a short coming encountered is that false lock on a sideband rather than carrier frequency is possible due to modulation, particularly when the loop bandwidth is less than the sideband to carrier frequency difference. Mostrom¹ and Victor et al.² have attempted to correct this problem using a discriminator-aided acquisition, however this approach necessitates a large carrier to noise ratio (CNR) in the bandwidth of the discriminator.

An Extended Range Phase Locked Loop (ERPLL) is designed to achieve acquisition function in PM demodulator application for the Advanced Range Instrumental Aircraft (ARIA) receiver AN/AKR-4, developed under airforce contract. By adding a phase modulator and an inverting amplifier to a conventional phase locked loop, the ERPLL is realized.

ERPLL Theory of Operation

In the ERPLL currently described, the overall gain factor K_d of the phase detector is modified due to the addition of a phase modulator and insertion of an inverting gain amplifier in the control insertion loop, as illustrated in Figure 2. In this design, the output of the phase detector (a double balanced mixer) is amplified, phase reversed and fed back to the linear phase modulator, which is in turn connected to the mixer. The phase detector outputs a new voltage, V_d' , which can be expressed as $V_d' = K_o(\Theta_s - \Theta_o)$, where $\Theta_o = K_m V_c + \Theta_i$ or $K_m A V_d'$, when Θ_i used as a reference is set to 0° . One can rewrite the V_d' as $V_d' = K_o \Theta_s - K_o K_m A V_d'$ or

$$V_d' = \frac{K_o \Theta_s}{1 + K_o K_m A} = K_d \Theta_s$$

The transfer function, $F(s)$, for a conventional integrator is

$$F(s) = \frac{A (t_2 s + 1)}{t_2 s + 1 + (1-A) t_1 s}$$

The modified transfunction, $F(s)$, for Figure 5(b) becomes

$$F(s) = \frac{t_2 s + 1}{t_1 s - \frac{t_1}{A} + \frac{t_2 s + 1}{A}}$$

$$\text{where } A = \frac{R_f}{R_4}$$

Using such an active filter, the strong signal tracking rate is defined by $\Delta\omega \leq \omega_n^2$. For a 5kHz loop bandwidth, maximum sweep rate yielded by this loop is 14 MHz/sec. For a 200kHz step change in input frequency and a loop gain of 7.2×10^6 , the velocity error is approximately 0.174° , which ensures optimum bit error rate performance in PM mode.

PM Demodulator Application

Also designed as part of the above ARIA receiver circuitry is a wide band, Extended Range, Phase locked detection loop for PM demodulation. Similar to that stated above, this loop incorporates a phase modulator circuit, an inverting amplifier and a double balanced mixer. Additional circuitry included are phase adjustor for phase matching the reference signal to the IF signal and an amplifier that provides amplification for the demodulated PM data output from the phase detector. A similar type of analysis to that described above is applicable to the PM detector.

By using the extended range PLL technique, demodulation of signals up to 120° deviation can be achieved. The linear portion of a conventional PLL phase detector is $\pm 60^\circ$. However, for the ERPLL, the linear region can be extended as a function of inverting amplifier gain.

The PM demodulator is phase locked by virtue of the APC loop. Therefore acquisition, tracking and anti-sideband capabilities are directly related to the APC loop parameters described above. Listed in the following table are the loop parameters designed for the ARIA receiver.

Table I

Strong Signal BL Loop BW	Minimum Tracking Rate at <u>0 dB in IF</u>	Maximum Strong Signal Phase Noise	Minimum Automatic Acquisition <u>Range</u>	Maximum Acquisition <u>Time</u>
10 Hz	5 Hz/sec	10° rms	-	-
30 Hz	50 Hz/sec	3° rms	-	-
100 Hz	550 Hz/sec	2° rms	±25 kHz	0.6 sec
300 Hz	5 kHz/sec	2° rms	±75 kHz	0.5 sec
1000 Hz	55 kHz/sec	1° rms	±200 kHz	0.3 sec
5000 Hz	500 kHz/sec	1° rms	±200 kHz	0.2 sec

A) Strong Signal Bandwidth:

The PM loop bandwidths are front panel selectable in 6 steps. These steps are: 10 Hz, 30 Hz, 100 Hz, 300 Hz, 1000 Hz and 5000 Hz. For each bandwidth, a Type II, second order control loop is employed. Automatic search is included for all but the narrowest two bandwidths. The 10 Hz and 30 Hz loops will be manual acquisition, only due to the extremely long acquisition time required. In the automatic mode, search is carried out in the 5000 Hz bandwidth. This will allow for a fast acquisition time. After the signal is acquired, a TRI-STATE switch network switches the necessary loop constants into the loop filter allowing "TRACK" in the selected front panel bandwidth. Precision components are used as the filter constants which would allow for a tolerance of better than 20% for loop parameters.

B) Tracking Rate:

For a Second Order PLL with a damping factor of 0.707, the natural frequency

$$\omega_n \approx \frac{\omega_{3dB}}{2}$$

Analysis by Viterbi has shown the following limit: $\Delta\omega_{max} \leq \omega_n^2$ where $\Delta\omega_{max}$ is the maximum permissible rate of change of input frequency. The limit states that the sweep can never exceed the square of the natural frequency or the loop will fall out of phase lock. Using this analysis for the above Table I yields:

B1) 10 Hz BW (w_n 31.4 rad/sec)

$$\Delta w = 6.28 \times 5 \text{ Hz/sec} = 31.4 \text{ rad/sec/sec}$$

$$\Delta w \leq w_n^2$$

$$31.4 \leq 31.4^2$$

B2) 30 Hz BW ($w_n = 94.2 \text{ rad/sec}$)

$$\Delta w = 50 \times 2\pi = 314 \text{ rad/sec/sec}$$

$$\Delta w \leq w_n^2$$

$$314 \leq 8.8 \times 10^3$$

B3) 100 Hz BW (w_n 314 rad/sec)

$$\Delta w = 550 \times 2\pi = 3.45 \times 10^3 \text{ rad/sec/sec}$$

$$\Delta w \leq w_n^2$$

$$3.45 \times 10^3 \leq 314^2$$

B4) 300 Hz BW ($w_n = 942 \text{ rad/sec}$)

$$\Delta w = 5 \times 10^3 \times 2\pi = 31.4 \times 10^3 \text{ rad/sec/sec}$$

$$31.4 \times 10^3 \leq 942^2$$

B5) 1 kHz BW ($w_n = 31.4 \times 10^3 \text{ rad/sec}$)

$$\Delta w = 55 \times 10^3 \times 2\pi = 345.4 \times 10^3 \text{ rad/sec/sec}$$

$$345.4 \times 10^3 \leq (31.4 \times 10^3)^2$$

B6) 5 kHz BW ($w_n = 15.7 \times 10^3 \text{ rad/sec}$)

$$\Delta w = 500 \times 10^3 \times 2\pi = 3140 \times 10^3 \text{ rad/sec/sec}$$

$$3140 \times 10^3 \leq (15.7 \times 10^3)^2$$

C) Strong Signal Phase Noise:

The worst case requirement for phase noise is the one for the narrowest PLL bandwidth, 10 Hz. The phase noise specified is 10 rms (20 peak assuming Gaussian noise). This is 0.33 radians peak deviation over noise. Referenced to a 10 Hz bandwidth, this would translate to a noise component being approximately 16 dB below the carrier at 10 Hz offset. Since phase noise is budgeted as slow noise in a 1 Hz bandwidth, this would correspond to a phase noise component equal to -26dBc at 10 Hz offset. The synthesizer and the VCO used for the ARIA Receiver have phase noise budgets of 20 to 25 dB better than that required.

D) Minimum Acquisition Range

The sweep to acquire circuit contains a ramp waveform which is summed into the Loop Filter. Weighting resistors are switched into the ramp circuit and allow sweep ranges as specified in the table. These resistors will be automatically switched upon loop bandwidth selection.

E) Maximum Acquisition Time

The rate of the search sweep will be 5 Hz which will permit acquisition of less than 0.2 seconds for all of the automatic bandwidths.

The receiver circuitry is designed so as to be phase-locked to the input signal in any of the coherent modes. The loop tracks Doppler and transmitter uncertainties within the constraints up to Δf of ± 250 kHz.

SUMMARY AND CONCLUSION

The above study describes the operation theory and applications of an Extended Range PLL circuitry. By using a double balanced mixer and phase modulator, the above Extended Range Phase Locked Demodulator yields a bandwidth of greater than 2 MHz. The use of phase remodulation reduces distortion to less than 2 % at phase deviations of 60 , and less than 5% at deviations of 130° . Bandwidth improvement factor (ratio of loop bandwidth to IF bandwidth) permits acquisition and tracking of signals of up to a -15 dB CNR in the selected IF or +6 dB SNR in the phase lock loop, whichever occurs first for manual acquisition. An Extended Range Acquisition PLL employing phase remodulation also discussed is field proven to prevent locking onto any sideband of any signal with up to 1.3 peak radian phase deviation.

ACKNOWLEDGEMENT

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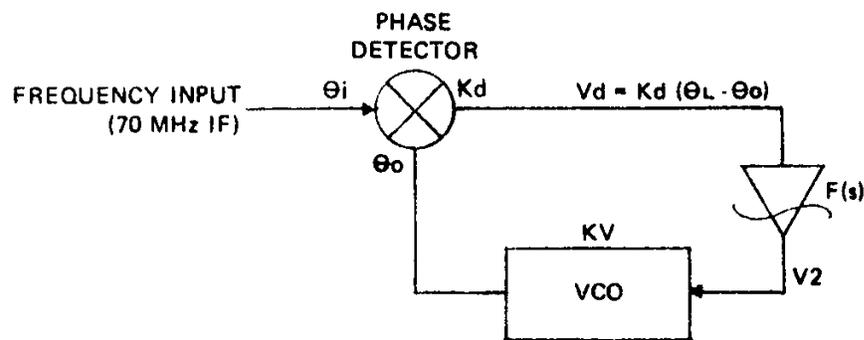


Figure 1 Conventional Phase Locked Loop, Block Diagram

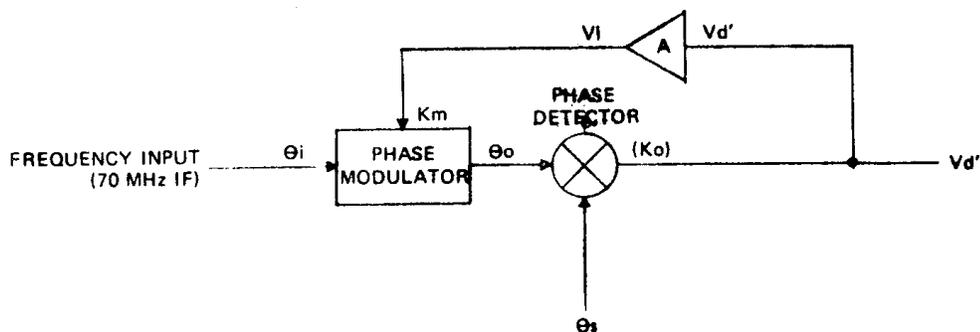
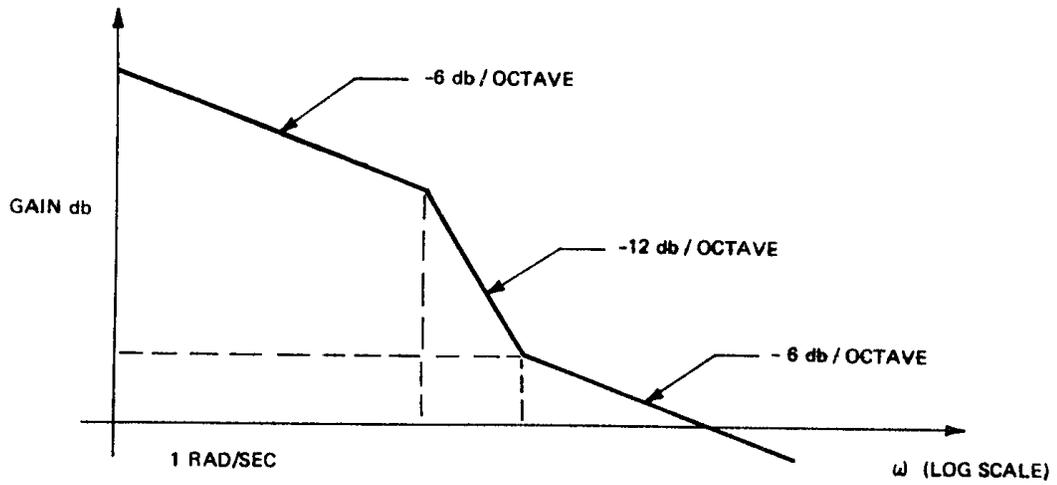
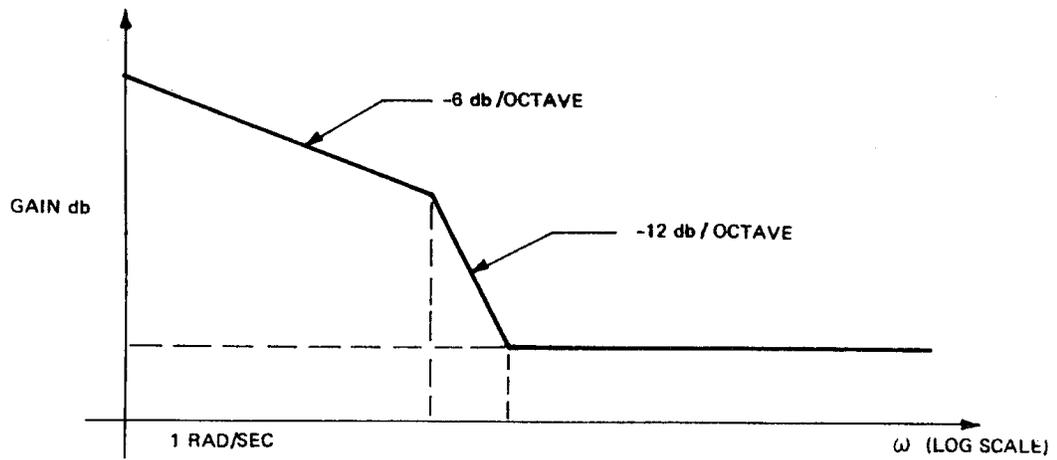


Figure 2 Typical Extended Range Phase Detector



3 (a)



3(b)

Figure 3
Typical Open-Loop Amplitude Response (a) Conventional
Second-Order, (b) ERPLD

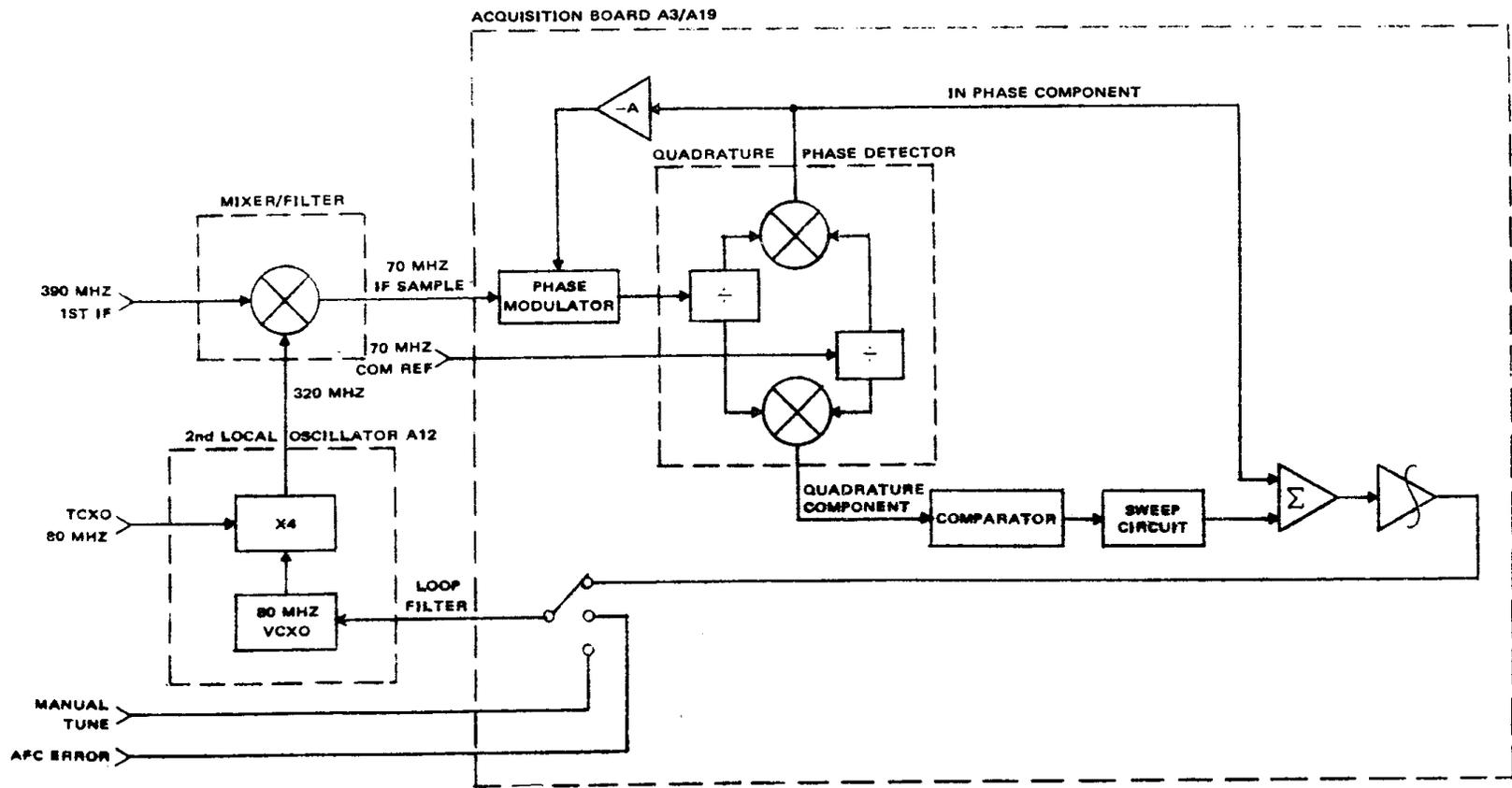
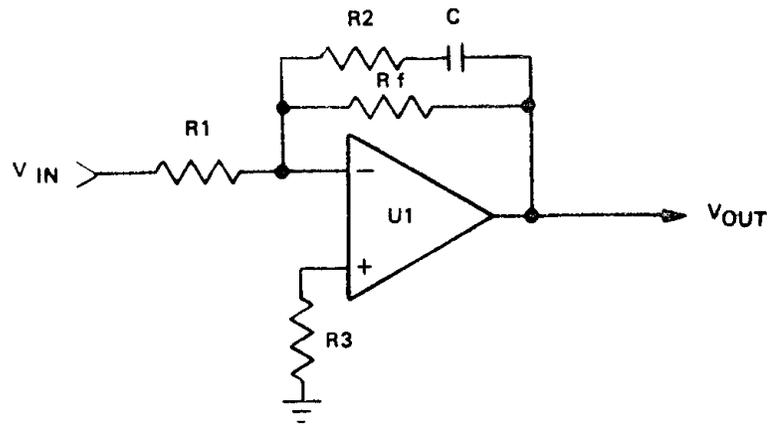
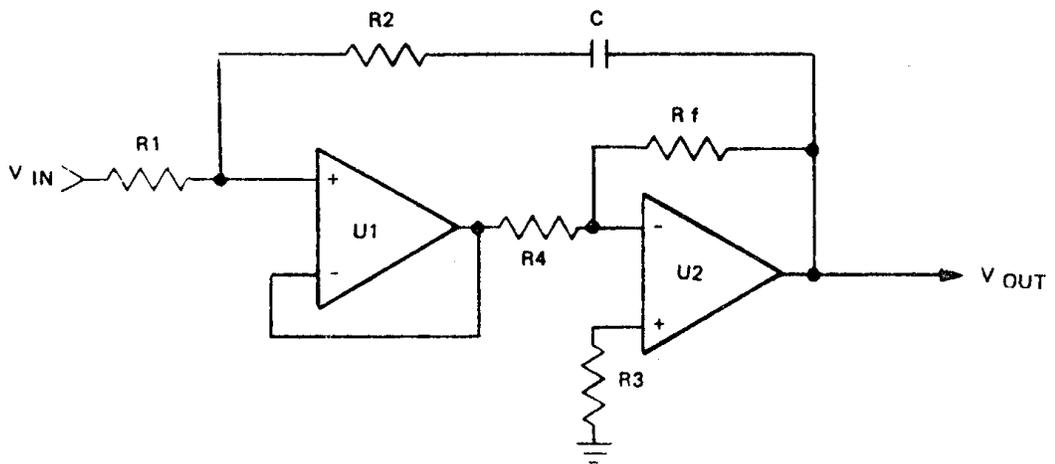


Figure 4 ARIA Receiver Phase Locked Loop Simplified Block Diagram



5 (a)



5 (b)

Figure 5
APC Loop Filter (a) Conventional (b) Modified ARIA Receiver Version