DIGITAL FSK/AM/PM SUB-CARRIER MODULATOR on a 6U-VME-CARD

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ABSTRACT

Aerospace Report No. TOR-0059(6110-01)-3, section 1.3.3 outlines the design and performance requirements of SGLS (Space Ground Link Subsystem) uplink services equipment. This modulation system finds application in the U.S. Air Force satellite uplink commanding system. The SGLS signal generator is specified as an FSK (Frequency Shift Keyed)/AM (Amplitude Modulation)/PM (Phase Modulation) sub-carrier modulator. GDP Space Systems has implemented, on a single 6U-VME card, a SGLS signal generator. The modulator accepts data from several possible sources and uses the data to key one of three FSK tone frequencies. This ternary FSK signal is amplitude modulated by a synchronized triangle wave running at one half the data rate. The FSK/AM signal is then used to phase modulate a tunable HF (High-Frequency) sub-carrier.

A digital design approach and the availability of integrated circuits with a high level of functionality enabled the realization of a SGLS signal generator on a single VME card. An analog implementation would have required up to three rack-mounted units to generate the same signal. The digital design improve performance, economy and reliability over analog approaches. This paper describes the advantages of a digital FSK/AM/PM modulation method, as well as DDS (Direct Digital Synthesis) and digital phase-lock techniques.

KEY WORDS

SGLS, FSK/AM/PM, Ternary FSK, Dibit Command Data, AM Phase Delay, Digital Phase-Lock Loop, Direct Digital Synthesis, Numerically-Controlled Oscillator

INTRODUCTION

GDP Space Systems has developed the FSK001, a single 6U-VME card SGLS signal generator. See Figure 1 for a graphical representation of the SGLS FSK/AM waveform. Earlier analog approaches to SGLS signal generation required three separate chassis: (1) a frame synchronizer with a phase-lock loop to extract the frame-formatted dibit encoded data and generate a rate-adjusted clock, (2) an FSK/AM modulator and (3) a phase modulator. The analog designs have limited tunability, require labor intensive alignments and are prone to drift over time and temperature. The digital techniques used in the FSK001 and the availability of high level functionality IC's have reduced the circuit board real estate required to generate the complex SGLS waveform. Additional benefits are increased flexibility, accuracy and reliability with virtually no required alignment.

HISTORY

There are two common analog methods to generate a ternary FSK signal and both have shortcomings. One method uses three oscillators free-running at the required FSK tone frequencies. The modulating data controls a switch to select the appropriate tone for each bit period. Amplitude variations of the resultant FSK signal, which originates from three independent sources, require alignment to remove. Furthermore, at each switching instant, the FSK signal exhibits a phase discontinuity; a nearly instantaneous jump to the arbitrary phase of a different oscillator. This phase discontinuity causes the signal to occupy a larger bandwidth than would be required if the phase remained continuous through the frequency transition. A second approach uses a single VCO (Voltage-Controlled Oscillator) whose output frequency is driven to each of the three FSK tone frequencies by applying one of three different DC voltages. In that the VCO frequency cannot change instantaneously, the output has no phase discontinuity, i.e., it is phase-continuous. VCO's with a sufficient range of frequency to generate all the SGLS tones have transfer functions that typically have linearity errors on the order of 5% and are also prone to drifting. Even with compensating circuitry and intensive alignment, this approach suffers with relatively large frequency errors.

The SGLS signal format requires the FSK signal to be amplitude modulated by a modified triangle wave which is synchronized with a specific phase relationship to the FSK frequency transitions. Historically, to accomplish this required a real estate-intensive analog phase-lock loop. The triangle wave, which has a frequency of one-half the modulating data rate, is phase-locked (synchronized) with a specific phase

delay to a clock derived from the modulating data clock. This phase delay, once set in the loop design, has limited range and is not readily adjustable.

Phase modulation of the SGLS signal requires an additional oscillator to generate a fixed sub-carrier frequency. A tunable sub-carrier would, of course, require more hardware and complexity. The traditional phase modulation process utilizes non-linear techniques. The phase modulation index (the amount of phase shift produced) is a non-linear function of the input modulating signal. Even over a limited range of adjustment, it must be compensated for linearity and accuracy.

DIGITAL SGLS MODULATOR THEORY OF OPERATION

The GDP FSK001 presents an improvement over traditional approaches to SGLS signal generation. It provides, on a single VME circuit board, the full functionality of a complete SGLS signal generation system, including:

(1) A frame sync for extracting and decoding dibit command data and frame parity checking.
(2) A phase-continuous ternary FSK modulator with full selectability of the frequency tone set.
(3) Amplitude modulation with full selectability of the modulation index and phase delay.
(4) Phase modulation by the FSK/AM signal with a fully tunable sub-carrier frequency and modulation index.
(5) An on-board PRN data generator with a fully tunable data rate.

In addition to the real estate economy, the FSK001, using digital signal processing offers significant strides in performance over the analog approach. DDS is used in the generation of the FSK tone frequencies, the PM sub-carrier and the PRN clock. One OCXO (Oven-Controlled CRYSTAL Oscillator) with an accuracy of better than 1 PPM provides timing for all of these signals. The use of NCO's (Numerically-Controlled Oscillators) provide a high degree of accuracy and flexibility. Applied to the FSK001, they effectively eliminate errors in: FSK frequency and amplitude variation between FSK tones; PM sub-carrier frequency and modulation index; amplitude modulation index and phase delay; and PRN clock frequency.

This digital approach yields an extremely versatile modulator. FSK modulating data is selectable from several possible sources including: (1) dibit command data, (2) direct ternary tone control data, (3) external serial data and (4) an on-board PRN data generator. Complete versatility is provided in the selection the FSK tone set, with each tone being tunable from 1 Hz to 5 MHz. The FSK signal can be modulated at data rates from 1 bps to 500 kbps. However, if amplitude modulation is required, then the data rate is constrained to 1 kbps, 2 kbps, 5 kbps or 10 kbps. The amplitude modulation index is adjustable from 33 to 100 percent modulation and phase delay is adjustable from 0 to 100 percent of the bit period. The phase modulation index is adjustable from 0 to 3.14 radians on a sub-carrier which is tunable from 1 Hz to 5 MHz. The FSK/AM/PM analog output of the FSK001 can be level adjusted from +20 dBm to -30 dBm (into 75 ohms). The GDP Model 784 is a rack-mountable, 3.5” high chassis housing the FSK001 modulator and a microprocessor controller. The controller handles data entry from a front panel keypad to setup the modulator, and it provides status feedback on a 2x40 alpha-numeric front panel display. Remote interface capability is available for unit setup and status feedback.
Refer to figure 2 for a functional block diagram of the FSK001. Dibit command data is the primary source of data for SGLS signal generation. When dibit command data is selected to modulate the FSK signal, it is accepted in a serial frame format of 48 bits per frame including 8 bits of overhead. Input data rates are limited to 2.4 kbps, 4.8 kbps, 12 kbps or 24 kbps. The frame sync locks to the input data by identifying a 7 bit sync word repeated in each frame. The frame sync, once locked, strips off the sync word and checks frame parity against an additional parity bit in each frame. The remaining 40 bits of serial data, with gaps left by the stripped overhead bits, are de-multiplexed into two parallel (dibit) data streams of 20 bits each and clocked out of the frame sync by a gated clock which is missing cycles corresponding to the overhead bits. A new clock running at a rate of 20/48ths of the input clock rate is needed to eliminate the data gaps. This is accomplished with a smoothing buffer consisting of: a FIFO memory, a VCO and a PLL loop filter. The gapped data is clocked into the FIFO by the gated clock and clocked out of the FIFO by a clock derived from the VCO. The FIFO Half-Full Flag serves as a phase detector that generates an error voltage which becomes the control voltage for the VCO by way of the loop filter.

The three remaining sources of data require less processing than dibit data. Ternary (1, 0 and S) data directly drives each of the three FSK tone frequencies with the restriction that only one tone be activated during any clock cycle. The occurrence of two or more simultaneously active lines is interpreted as an error condition and the

modulator continues to output the last valid tone keyed. External serial data and the internally generated PRN data cannot be used to drive ternary FSK tones. Instead, any two of the three tones are selected to be keyed by the ones and zeros of the data stream to generate binary FSK.

FSK modulation is generated by DDS techniques on the FSK001. Because of the DDS implementation and VME control of the tone set, the FSK frequencies may be set to any arbitrary value up to 5 MHz. The selected tone frequencies are setup as delta-phase data for an NCO and stored in an on-board static RAM. The FSK modulating data is used to update the NCO output frequency by initiating the transfer of the appropriate frequency data from RAM into the NCO. After pipeline delay, the frequency change occurs within a single NCO clock cycle (40 nsec.) and the phase is continuous. Having one common path, the FSK output exhibits no amplitude variation from tone to tone. In addition to being modulated by data, the FSK generator may also be forced to any of the three tone frequencies via the VME controller.

The FSK signal is amplitude modulated by a modified triangle wave. The triangle wave is digitally generated using an 11-bit up/down counter. Modulation index is controlled by setting two variables; terminal count up and terminal count down. The VCO in the smoothing buffer is running at 10.24 MHz which may conveniently be divided down to generate one of the four available bit rates for AM operation. The VCO clock is first divided by 1, 2, 5 or 10 to generate a clock running 1024 times the bit rate in order to drive the triangle wave generator (counter). The phase delay of the AM envelope to the FSK frequency transition is controlled with an additional variable which forces the counter to some value (within its count range) coincident with the rising edge of the one-half bit rate clock. The phase delay of the AM'ing signal can be set with a resolution of 1 in 1024. The FSK signal and the triangle wave are digitally multiplied to produce the FSK/AM signal. AM can be turned off by forcing the counter to hold at its terminal count up.

Phase modulation is also accomplished with DDS methods. The PM sub-carrier is tunable from 1 Hz to 5 MHz with an accuracy better than 1 PPM. The sub-carrier generation NCO accepts 16 bits of phase modulation data. A prescaled version of the FSK/AM product is connected to this modulation port. The prescaling is a function of the phase modulation index which may be set from zero to pi radians. Phase modulation may be bypassed for a card output of FSK/AM only.

Before being output, the digital FSK/AM/PM or FSK/AM is converted to analog with a 10-bit DAC. The DAC output is lowpass filtered then level-adjusted for an output range of -30 dBm to +20 dBm (into 75 ohms). The card output level is VME controllable to 0.1 dBm resolution.

CONCLUSION

The FSK001 digital FSK/AM/PM modulator offers economy and performance advantages over traditional analog approaches to SGLS signal generation. A full function SGLS signal generation system that once required three chassis is now available on a single 6U-VME card. These savings in board real estate and power consumption are possible because of the recent availability of high functionality IC's. With the use of digital signal processing, including direct digital synthesis, a high degree of accuracy is achieved for generated frequencies and modulation indexes. Circuit alignment is also virtually eliminated. The only adjustment on the board is the tweaking (±3 PPM) of a single oven-controlled VCXO. It is this from VCXO that all modulation signals and the internal PRN data clock are derived. DDS technology and VME control make the FSK001 flexible, thus more versatile than a system designed specifically for SGLS signal generation.

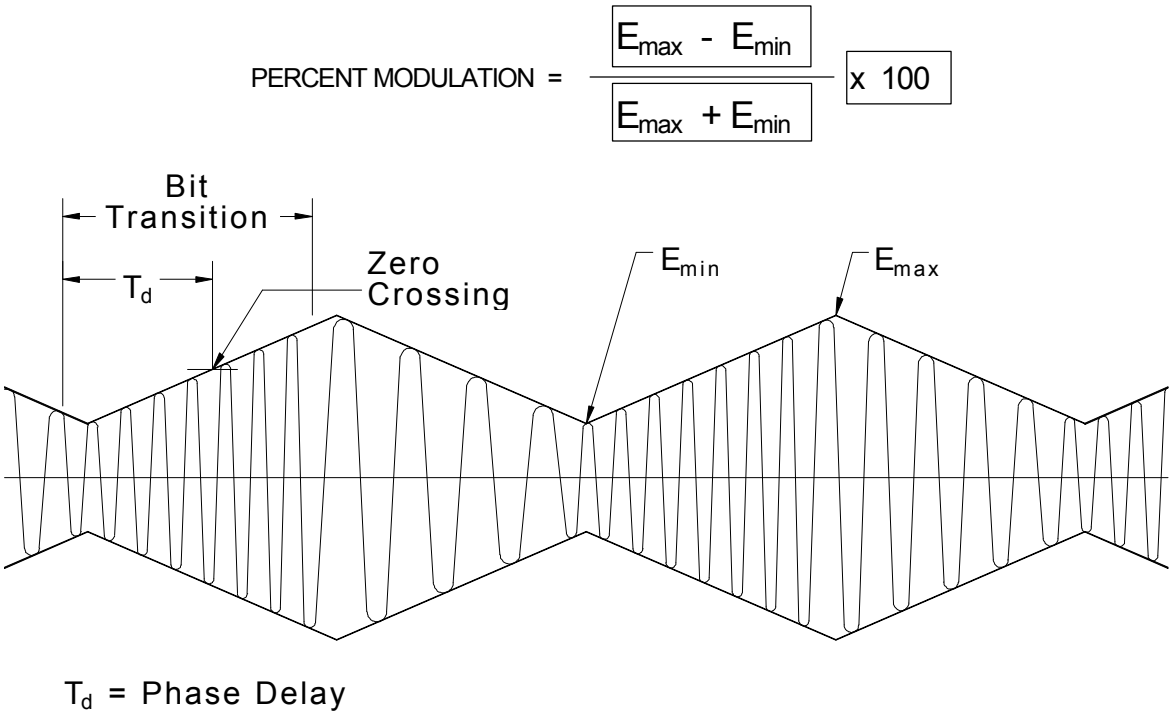

FIGURE 1 - SGLS FSK/AM SIGNAL WAVEFORM

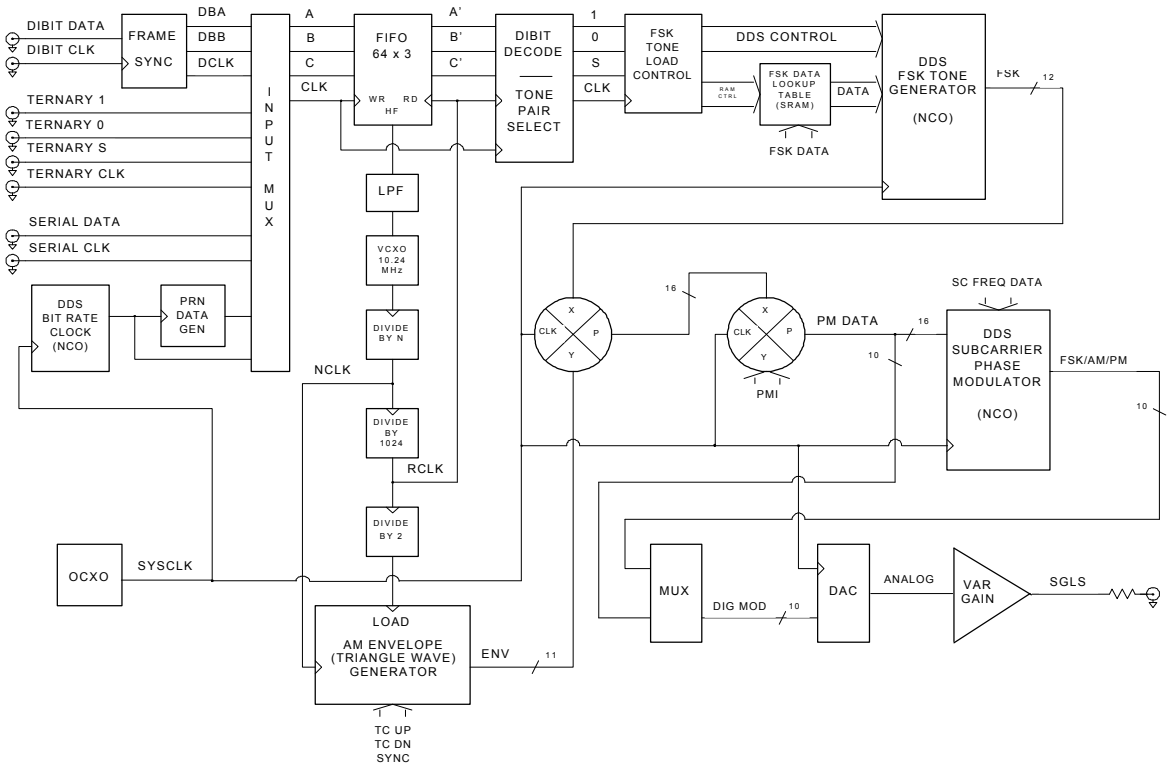

FIGURE 2 - FSK001 FUNCTIONAL BLOCK DIAGRAM