FARADAY CUP SYSTEM CONTROL LOGIC ON THE WIND SPACECRAFT

Anton Mavretic, Anastasios Konstantinidis, Emile Gergin, Runde Zhou
Boston University
College of Engineering
Department of Electrical, Computer and Systems Engineering
Microelectronics Research Laboratory

ABSTRACT

A satellite-mounted instrument has been developed to measure the energy spectrum of the solar proton flux in the solar wind. The instrument consists of a sensor --- the Faraday Cup, an analog signal processing chain, a high voltage modulator and a digital section. This paper presents the digital section designed and built in our laboratory which functions well to (a) interface with the main processor, (b) to provide the logic signals with proper timing to the analog circuitry, (c) to deliver the necessary bit pattern to the high voltage modulator, (d) to provide the calibration mode control signals when necessary, and (e) to synchronize the sequence of events at the begining of every spacecraft rotation. As with all space projects primary concerns beyond the logical functionality consistes of circuit power consumption, instrumental mass, radiation tolerance levels, stability with respect to temperature, and relative ease of component procurement. The NASA WIND laboratory spacecraft that will carry the experiment is due to be launched in December of 1992 and eventually come to park in an orbit at the first Lagrangian point.

INTRODUCTION

Currently project WIND spacecraft scheduled for launch in December of 1992 will carry an array of 8 experiment packages for measuring electric and magnetic fields and charged particles. Included will be a pair of Faraday cup detectors for measuring solar wind protons. The systemin consists of four interconnected subsystems (Fig. 1). The first of which is the sensor, the Faraday Cup, whose sole purpose is the detection of the incoming plasma. The cup has seven grids inside: five ground grids, one suppressor grid, and one modulator grid. The modulator grid can be thought of as the shuders to the window. As its voltage is modulated it modulates particle influx according to kinetic energy. There are two cups diametrically opposed on the spacecraft, therefore, as the spacecraft rotates about its axis once every three seconds, it can map out the solar wind distribution in its three directions. The second subsystem is the Faraday Cup system. It has

the responsibility for processing the detected plasma, assigning a digital count to a corresponding injected current level and interfacing with the remaining two sections to insure the smooth operation of the experiment. The third subsystem is the High Voltage Modulator. It is essentially a high voltage digital to analog converter. It accepts a six bit digital voltage and a 200Hz control signal and translates this to an analog voltage which is used to drive the modulator grid in the Faraday Cup. The fourth and the last subsystem is the digital processing unit, or DPU, which interfaces with the FCS through the Digital Processing Unit Instrument Interface, DPUII. The DPU acts as a central processor, it oversees the function of the two Faraday Cup experiments, as well as the two VEIS sensors, which detect the electrons in the solar wind. The spacecraft sunsensor actually generates a sun pulse at a certain time in each rotation. This sun pulse is transfered to the FCS via the DPU in the form of the "sunsync" enabling the experiment to orient itself with respect to the spacecraft's spin phase.

A closer look at the second subsystem, i.e., the Faraday Cup system (FCS), yields the finer details involved. It is an intricate ensemble of smaller subsections connected in series to yield a true measurement chain. Because there are two half cup collector plates, there are two parallel measurement chains for each Faraday Cup. At the front end of each chain is a preamplifier. It is directly connected to the collector plate on the cup and acts as a transimpedance amplifier converting the input current to an output voltage signal. The signal is then passed through three range amplifiers set to gains such that the total dynamic range of the system is 10^5. The output of each range amplifier is fed to a synchronous detector and then integrated. Since the output of the filter stage for all practical purposes is a sinusoid, the synchronous detection scheme yields a waveform that is rectified and hence carries inherent dc information. It is this information which is extracted in the integrator. Each integrators gives its own different readings corresponding to each level of amplification, a method for choosing the appropriate value for conversion must follow. This choice is made by the analog multiplexer. The integration is completed and range selection starts when the voltage of the integrating capacitor is held constant. Integration can resume only when the integrating capacitor is discharged completely. Given that at some higher levels of amplification saturation of the signal at 10V will occur the multiplexer begins its search by looking at the highest range, the one with the most gain. If the highest range is saturated it then looks at the second, followed by the third. The multiplexer will output the highest unsaturated range to the converter. After the a proper value has been chosen, the multiplexer outputs this to the logarithmic analog to digital converter. The converter is made up of essentially two simple building blocks. The first is a comparator which compares the input from the multiplexer to a decaying voltage governed by an RC time constant. When the decaying voltage reaches the input from the multiplexer the comparator changes state. It is this change of state that triggers the second section of the converter, i.e, 10 bit counter. The counter begins its count when the range selection is complete and ends when the comparator changes state thus equating a 10 bit

digital word to the input voltage. The 10 bit output word along with range information and various control bits are thus the responsibility of the final and largest block in the FCS, which is the provider of the control signals that are needed for the sequential operation of the measurement chain and is the avenue for information transfer to the DPUII via a 16 bit bidirectional bus and nine control lines and eventually to Earth through spacecraft telemetry. This logic and latching section of the experiment, from now on refered to as the logic board, will be presented in this paper in detail.

DESIGN METHODOLOGY

When viewed closely, the logic board can be seen as a union of smaller sections each with its own function (Fig. 2). The board provides the calibration circuit with the nine bits of information it needs to properly activate the current injection level. It also provides the modulator with the alternating six bit pattern that sets the energy window at the Faraday Cup. As a controller it assures the generation and distribution of the control signals that are necessary for the operation of the measurement chain and it contains the counting section of the logarithmic analog to digital converter and the output latches. The final section is the synchronous detector logic and level shifting stage.

The design process for the logic board consistes of grouping the subunits into two sections. The first is the latching and level shifting section consisting of the modulator value generator, the calibration circuit controller, the data output latches, the log A/D counters, and the synchronous detector's logic and level shifting. The second is the control logic section that provides the signals for the synchronous detector and the logarithmic converter. When the timing of the logic signals is investigated one can readily see the definition of distinct boundaries that if repeated in the correct sequence will provide the experiment the necessary flexibility in integration times. We accomplish this through two methods: (a) the logic signals are stored in memory segments and stepped through sequentially; (b) the logic signals are generated through discrete combinatorial logic.

The logic board outputs seven essential control signals to the analog signal processing chain. The calibrator and the modulator both need a 200Hz clock in order to generate the appropriate input signal at the preamplifier. This clock is called the U200 signal (U = undelayed). As the input waveform is processed a time delay is incurred between the input and the synchronous detector primarily due to the phase response of the filter stage. For proper synchronous detection, the logic board has to provide a delayed 200Hz, D200, control signal with respect to U200. The D200 signal has a delay set to the total delay from the preamplifier to the synchronous detector and is used in switching between positive and negative gains. The third signal is the HOLD signal. As the name implies, the signal has the responsibility for holding the charge on the integrating capacitor and keeping it held until a new measurement is ready to begin. DUMP signifies the end of

conversion and the beginning of a new measurement by discharging the integrating capacitor.

Up to this point the flow of logic has been to the inputs and the integrator. The fifth signal, MUXCLK , is a clock that drives the multiplexer since its job is to cycle through the three integrators and choose the highest nonsaturated output. The CHCAP signal is fed to the log A/D and charges the capacitor used to generate the RC time constant necessary for logarithmic conversion. The \CHCAP signal is used to clear the A/D counters so that the count begins at zero as the decay is triggered.

Operation of the logic board occurs under two regimes. The first is initialization, once every spacecraft spin, while the second is the normal mode of operation between spacecraft initializations. Accordingly the logic signals that are generated dictate a pattern of operation which consists of alternating variable time measurement frames and 5ms service cycles. The time programed by the DPU for integration of the incoming flux is equal to the time of the measurement frame. The 5ms of service corresponds to the allotted time for multiplexing or choosing the proper range, analog to digital conversion, writing of the output word to the latches, and dumping of the charge on the integrating capacitor. It also allows for the segmentation of the timing diagram into four blocks. By proper sequencing of these four blocks, the logic signals are recreated with allowances for variable integration lengths. The four segments are I for initialization, R for repeat, F for first, and S for service (Fig. 3).

The I segment is the first 5ms of every spacecraft spin and as such it is the marker for the begining of the logic signals. R repeats for a period of time equal to the desired integration time minus 5ms. F is the segment of time corresponding to the last 5ms of integration and is also the first segment during which service begins. The S segment is the 5ms service time before the start of the next integration period. A signal P is generated in logic and is used to step through the segments at 5ms intervals. A complete integration period consisting of one measurement frame and one service cycle is marked by the EOCY signal, end of cycle, and returns the order back to R.

The DPU has to provide the necessary control words and read the output data from the Faraday Cup experiment during the measurement frame. This, coupled with the DPU's fixed interrupt rate of 35ms, gives us the following operating sequence: as the integration times are multiples of 30ms and for each integration there is one 5ms service cycle the DPU will interrupt -service the Faraday Cup at least once every integration frame. At this time the DPU reads the data from the previous measurement and writes the controls for the following measurement. If the set integration is longer than 30ms the DPU will interrupt more than once. The first of these will set the conditions while the remaining are NOPs, no operations.

One final concern is the very last integration before a new sunsync. Since the spacecraft rotation rate varies slightly the last measurement may not be completed before the sunsync arrives. If this is the case the last measurement will be discarded and a new measurement started after I.

LATCHING AND LEVEL SHIFTING

Latching

The latching section of the logic board is assigned the task of writing or reading the proper control bits and data words to and from the DPUII. The signals that are latched consist of the two six-bit words corresponding to the modulator high value and modulator low value, the eight-bit word for the calibration level, the eight-bit word for the integration time, and the two sixteen-bit words for the output data. Since the DPU interrupts occur every 35ms, and since the integration time is determined by the science, specifically what angle the cup makes with the incoming solar wind, the control data must be double latched in order to insure that: (a) the DPU can meet its requirements to other experiments and service the Faraday Cup every 35ms, and (b) the digital board can continue to provide an arbitrary integration interval followed by a 5ms service cycle. For the output data, double latching is not required since the data will be written to the latches by the logic board, while the output enabling of the latches will be controlled by the DPUII. The DPUII communicates through a 16-bit bus; the least eight significant bits are used to transfer all the control words while the most eight significant bits are activated only when transfering data to the DPU. The latches used are HCS374 series and are octal D flip-flop's with a clock and an output enable.

(1) Calibration Latching

Calibration levels are entered by the DPUII when the first calibration latch is clocked with the /Calib Data signal. Since the output enable is tied low the data will be made available to the second latch on the rising edge of the clock signal. The second latch is clocked with the DUMP signal assuring that the calibration level is output to the calibrator during a service cycle. The calibration word is eight bits and includes an on/off bit, a shift bit, and six level bits giving the system a total of 12 possible current injection levels. If the calibrators on both of the analog boards are turned on simultaneously through the D7 bit of the input control word the power dissipation of the system will peak at the onset of calibration. One method for reducing this peak is to calibrate each measurement chain individually. In order to accomplish this we must bring into action a second control line. A possible calibration algorithm is to calibrate the FCS that is looking away from the sun.

The second line is available to us in the CAL/\MES signal, which is the signal to signify when calibration or measurement is occuring; combining it with D7 from the DPUII we can decode four operating states: (a) both calibrators are off and the analog boards are measuring solar wind, (b) both calibrators are on and the measurement chains are calibrated simultaneously, (c) chain A is measuring solar wind and chain B is being calibrated with a set current, and (d) chain A is being calibrated with a set current while chain B is measuring solar wind. Before we can do the decoding we first have to latch the CAL/\MES signal since it is the level that is important. This is done with a '74 series D flip-flop. The two control bits then define the bits K8(A) and K8(B) which turn on or turn off the calibrators on the analog boards, A and B. The functionality is shown below where the control bit D7 is equal to K8(A) and K8(B) being equal to the exclusive or of the two controls D7 and CAL/\MES, represented below as X.

$$C8(A) = D7$$
$$C8(B) = D7\overline{X} \oplus \overline{D7}X$$
$$= \overline{(D7\overline{X})(\overline{D7}X)}$$

By rewriting the expression for K8(B) we see that implementation is accomplished through the use of three 2-input NAND gates, HCS00's, and 2 inverters.

Calibration can occur at the beginning of a sun cycle or in the middle of a spin since the writing of the CAL/\MES signal will cause the calibrator to inject current to the cup at the first service cycle after the data is available. Since the data at the end of each spacecraft rotation is questionable and therefore discarded actuating the calibration mode during the first DPU interrupt will insure that calibration mode is on during the second integration period. One potentially useful result brought forth by the ability to calibrate each measurement chain individually is testing for crosstalk between the two analog boards in each instrument in flight.

(2) Modulator Latching

The two sets of modulator latches work on the same principle as the calibrator latching. The high byte is latched in with /MH while the low byte is latched in with /ML both are transfered to the second latch with the rising edge of HOLD. Since the output to the modulator is a six-bit value the second latches are output enabled with D200 for the high level and /D200 for the low level.

The resulting output is then multiplexed to yield the six bit MODVALUE through a HCS374 latch that is appropriately clocked yielding output that alternates between the high and low values. The clock signal is generated by delaying U200 with a HCS74 (D flip-flop) for one clock cycle, 10μs, generating a shifted U200. Taking the NAND of U200 and its shifted counterpart produces a signal X. Similarly the NAND of \U200 and the \Q

output of the flip-flop produces a signal Y. Finaly the clock signal for the multiplexing latch is then the AND of X and Y.

(3) Integration Time Latching

The integration time is different in that it uses the properties of a HCS161 series counter to mimic double latching thus saving one component. The /NI signal loads the eight bit integration word into the first latch and with the output enable low the counters have immediate access to the eight bits. They are loaded with this data on the rising edge of the clock when their LOAD input, the EOCY signal, is low. This, however, occurs only at the end of the I and S segments, the end of an old integration and the start of a new one.

(4) Output Data Latching

A 16-bit data word is the output of the electronics. It is latched into two HCS374's connected in series with the rising edge of the DUMP signal which signifies the last time during an integration cycle that the data is valid. During the following integration the DPUII reads the data by output enabling the latches with the /Coll A OE and /Coll B OE signals corresponding to both sets of data latches. The first 10 bits of the return word are data with the next two (11 and 12) being the range information. One bit designates wether the data is chain A or chain B. Another bit reflects wether the chain is in measurement mode or calibration mode and one bit tells if the modulator is on or off. The final bit is used as parity.

Level Shifting

The logic signals, HOLD, DUMP, D200, CHCAP, Range Info. 1A, Range Info. 1B, Range Info. 2A, and Range Info. 2B, drive the switches on the analog board and therefore must be level shifted. This is accomplished with two CD40109 series level shifters with each chip handling four signals.

Log A/D Counters and Range Selection

A section of circuitry used for logarithmic conversion for both chains is also located on the logic board and consist of 6 HCS161 binary counters with asynchronous clear, 1 HCS109 dual J-K flip-flop, and 1 HCS00 quad 2-input NAND gates. The circuitry for each chain consists of 3 '161's in series yielding the 10 bits necessary for conversion, 1 J-K flip-flop for gating the clock, and two NAND gates to place the counters in the appropriate state at the end of conversion.

Before the converter can begin, the multiplexer has to choose between the three ranges within 100µs. This is accomplished through a HCS161 counter that is clocked with the MUXCLK signal. The counter is cleared with the HOLD signal meaning that its outputs are always zero (Range Info. 1A or B and Range Info. 2A or B). As HOLD goes high the counter bigins its search through the three ranges to find the first nonsaturated integrator. Since the enable line of the counter is controled through the inverted comparator output the count will be disabled when the output of the comparator reads one corresponding to the first range with a value below that of 10V.

GENERATING THE CONTROL SIGNALS

Fairly early in the design process the approach for producing the logic signals was separated into two methods (Fig. 4). Proper function of the analog measurement chain can be observed by producing the necessary signals through: a) stored memory; b) combinatory logic. In both cases the circuitry can be devided into four subsections; the reduced clock and load generator, the integration time counter, the address and data generator, and the segment selector in the case of memory and the reduced clock and load generator, the integration time counter, the U200 and D200 generator, and the delayed signals generator in the case of combinatorial logic.

Generating Signals From a Memory Table

The logic signals necessary for proper operation of the FCS and the method by which they've been generated have gone through much refinement since the original design. After calculations, the allowable jitter error from the logic signals enabled the reduction of the driving frequency for the signals, and hence the necessary memory size to 2k x 8. This set the number of address lines needed to 10. The memory itself is a Harris 6617RH PROM (Radiation Hardened PROM).

As noted earlier the timing diagram can be separated into four segments; I (initial), R (repetitive), F (first), and S (second). Stepping through the segments is driven by a 100kHz reduced clock so that each data byte (8 signals) accounts for 10µs. Hence, 500 bytes are required to fill the 5ms period of a 200Hz waveform. The simplest addressing mechanism is obtained if the 5ms cycles begin at binary boundaries. The first power of 2 greater than 500 is 512, or 200H, which defines the memory segment size.

Generating Signals Through Combinatorial Logic

The second approach to the logic signals incorporated some different ideas when compared with the first approach. Although it was not the first design choice because of its increased complexity and chip count it quickly developed into our only alternative for the

following reasons. Since the environment in which the circuitry would operate has an elevated radiation level the radiation hardened versions of commercial logic was used (HCS' series). This meant that some parts that expedited the design were not available without extremely long lead times while others that were available had to be qualified for flight at an enormous financial cost to the project.

The major obstacle, however difficult the logistical issues regarding the availability of the logic components were, centered around the radiation hardness, or in this case softness, of the Harris 6617 2K x 8 PROM. It seems that although the data sheets on the chip state its radiation tolerance up to 100krad some preliminary evidence from the DPU and NASA Goddard state that the part is very questionable at 20k and certainly would have problems at 30k. Given that the radiation specification is at 20k and barring any increased solar activity that would further add to that fact, the design with the part is marginal at best with regards to radiation. One solution is to switch to bipolar PROMs. This means a substantial increase in power consumption and is simply unacceptable since the memory on the board needs to be active during continuous operation of the measurement chain. Therefore the alternatives left to us are (a) continue with the design as before in hope that the marginal radiation tolerances of the Harris part would cope well with the WIND environment or (b) redesign the logic section of the board by generating the signals normally derived from the PROM by discrete logic. Needless to say we chose the latter and optimized the circuitry as before to yield the least amount of hardware corresponding to the least amount of additional real estate. One area of optimization that was not discussed in previous missions was the operating frequency of the system. The 200Hz operating frequency was as in the past a compromise between the science on one hand requesting that the electronics take quicker and quicker snapshots at the incoming signal and the electronical preference of lower frequencies insuring the capability of operation within the open loop response of the amplifiers. This too has a limit since the lower one goes in frequency the closer one gets to the natural resonance of the mechanical components in the sensor which could couple undesired signal into the input. When it comes to logic 200Hz is an inconvenient number since it is not a power of two. Thus the components that were needed to generate the U200 and D200 signals included synchronous counters, eight input gates, and up down decade counters. These could be eliminated or replaced by less exotic approved for flight two input gates and asyncronous counters if the frequency of operation was changed slightly to accommodate logic by using a different reduced clock and counting to a convenient value (only two ones).

RESULTS AND DISCUSION

The two versions of the logic discussed so far differ not only in their approach to generating a specific signal, the number of components employed in each design and the types of logic gates used, but also in their power dissipation and the board mass. The

power dissipation is the first obvious concern in this design, since we are dealing with space the energy source for any instrument is less aboundant when compared to a simple wall socket here on tera firma. Therefore its reduction to the lowest possible levels is essential. In order to acheive this both versions of the logic were implemented using CM0S technology. An additional aspect of the design process was the mass budget of the instrument. This should be kept at an absolute minimum saving fuel and ultimately power. A comparison of the mass that each of the two alternatives will contribute to the instrument budget was calculated in a straight forward manner. The total mass of the logic board was set equal to the sum of the masses of the components (integrated circuits, resistors, capacitors), the mass of the G10 (1/16") board, and the mass of the Cu tracing and ground planes. In the case of memory version assuming a 6" x 7" board area and a Cu thickness of 0.002" we have a total mass of 245 grams. In the case of conbinatorial version we assume that an extra 3" x 7" piggyback board will be necessary. This makes the mass of the v2.0 board 300 grams.

Thus, from a designers point of view the memory versionis the one that seems to make the most scense. It is compact in board size, has fewer chips, and therefore easier to lay out, fabricate, and test. However appealing at first glance, it presented some unique problems. In order to do the functions of the logic board elegantly we were forced to use components that although abundant and easy to acquire in comercial form were not so readily available nor often used in space applications. First, this generated long lead times (in some cases up to 52 weeks) for the entire project. Second, since these components were not previously flown they had to be qualified and consequently presented an enormous financial cost to the project. Third, the logic board needed memory which possed problems with radiation hardness and more importantly questions concerning single-event upsets. The memory version of logic however served its purpose in the developemental stage of the total system and in particular the testing of the analog measurement chain delay between the preamplifier front end and the synchronous detector. Easily programable EPROMS allowed the fine tuning of the delay so that the final hard wired value was optimized in that respect.

Before the second version of the logic was attempted it was recognized that removal of the memory would increase the total number of components in our design. That fact coupled with a requirement that the design be totaly free of difficult parts made it extemely nessesary for complete optimization such that the final design would be comparable or better than the first with respect to power consumption, chip count, total mass, and mechanical orientation. One such method of optimization was established through an analysis of the system operating frequency, 200Hz. This was chosen as a comprimize between the mechanical aspects of the sensor on one hand and the frequency response limitations of the electronics on the other. However adequate a solution as far as the sensor and analog sections are concerned, this number presents problems for the logic. It is not a

number generated by 2^n and therefore needs multiple counting and decoding stages. By moving the operating frequency to 199.3Hz, a number as equally acceptable as 200Hz from a scientific and analog standpoint, we can generate the system clock through a minimum number of counters and 2-input NAND gates. This solves two problems. It reduces the number of components and also elliminates one of the expensive gates from the original design. Another area where optimization is evident is in the reduction of the 1MHz system clock to a 13µs reduced clock. This eventually saves on power since consumption in the components is directly proportional to their operating frequency. A third and power related issue is the illimination of memory. Although the memeory version used a low power CMOS PROM it was by far the most hungry component on the board when in continuous operation mode. Through its illimination and replacement with conventional counters, flip-flops, and logic gates the power consumtion was reduced by more than a factor of 60 (from $\approx$135mW to $\approx$2mW) under normal operation. The second version however, increased the board mass primarily through the addition of extra components nessesitating an additional piggyback to the logic board. This was an increase of 50g only to the logic board.

From the thermal design viewpoint, the elimination of the memory was a welcome bonus: it eliminates the one hot spot on the logic board. As this spot was to be cooled by two flanking aluminum spacers, these spacers are now eliminated, freeing the boards real estate for more profitable use.

CONCLUSION

A low power, low mass, radiation hardened logic board that functions as the system interface to the main processing unit aboard the spacecraft has been built and tested. The logic board also delivers the bit pattern to the high voltage modulator driving the Faraday Cup sensor while providing the calibration control signals when that mode is actuated. The delicacy of the designed microelectronics art and the elegance of the fine tunning and optimization methodology will be concretely confirmed following the launching of the WIND spacecraft in 1992 by NASA.

REFERENCES

[1] Akasofu, S. “The Dynamic Aurora”, Scientific American, May 1989, pg.60-97.

[2] Ansell, G.P. and Tirado, J.S., “CMOS in Radiation Environments”, VLSI Design, September 1986.

[3] Bridge, H. S., Belcher, J. W, Butler, R. J. , Lazarus, A. J., Mavretic, A., Sullivan, J. D., Siscoe, C. L., Vasyliunas, V. M. "The Plasma Experiment on the 1977 Voyager Mission", Space Science Reviews 21, 1977.

[4] Goddard Space Flight Center "GSFC Prefered Parts List PPL-18", October 1986.

[5] Grover, J.E., "Basic Radiation Effects in Electronics Technology", IEEE Tutotrial Short Course on Radiation Effects, 1984.

[6] Lanzerotti, L. J., Krimigis, S. M. "Comparative Magnetospheres", Physics Today, November 1985, pg.24-34.

[7] Lanzerotti, L. J.,Uberoi, C. "Earth's Magnetic Environment", Sky & Telescope, October 1988, pg.360-362.

[8] Mavretic, A. , Spritounias, E., Cano, M. "An Ultra Low Current, Large Dynamic Range Self-Calibrating Measuring System as Used for Plasma Current Detection", ISYNT '89, Zagreb., pg.401-409.

[9] Schroeder, J.E., Ocha, A., Jr. and Dressendorfer, P.V., "Latch-up Elimination in Bulk CMOS LSI Circuits", IEEE Transactions on Nuclear Science, Vol NS-27

[10] Srour, J., "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits", IEEE 1982 Anual Conference on Nuclear and Space Radiation Effects.

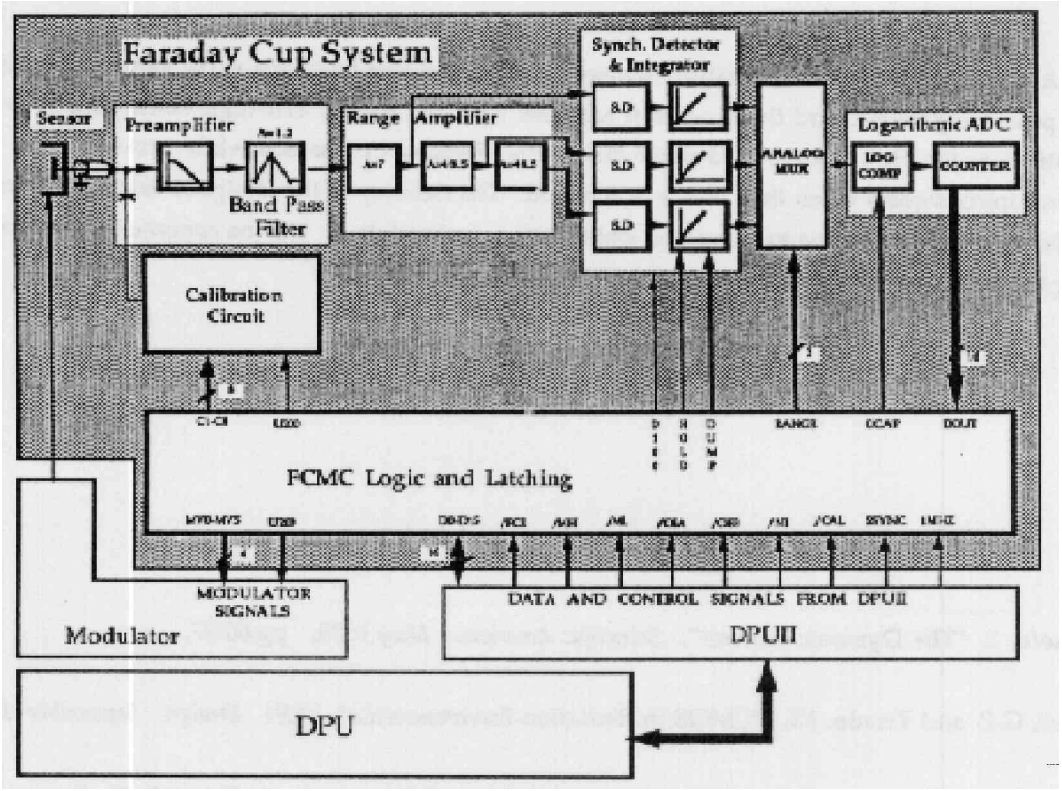

Fig. 1 The Faraday Cup System.

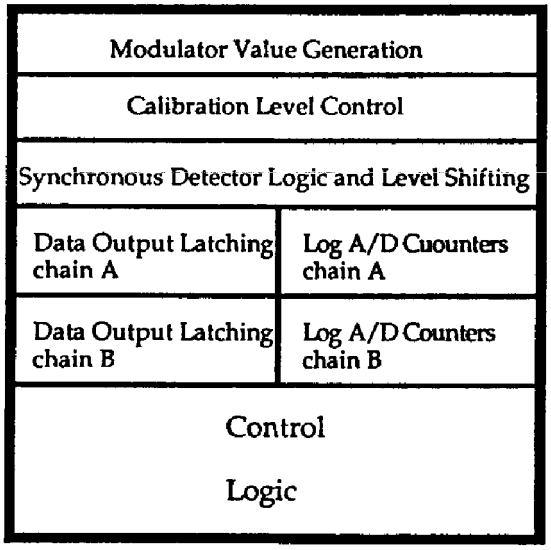

Fig. 2 Logic Board Block Diagram

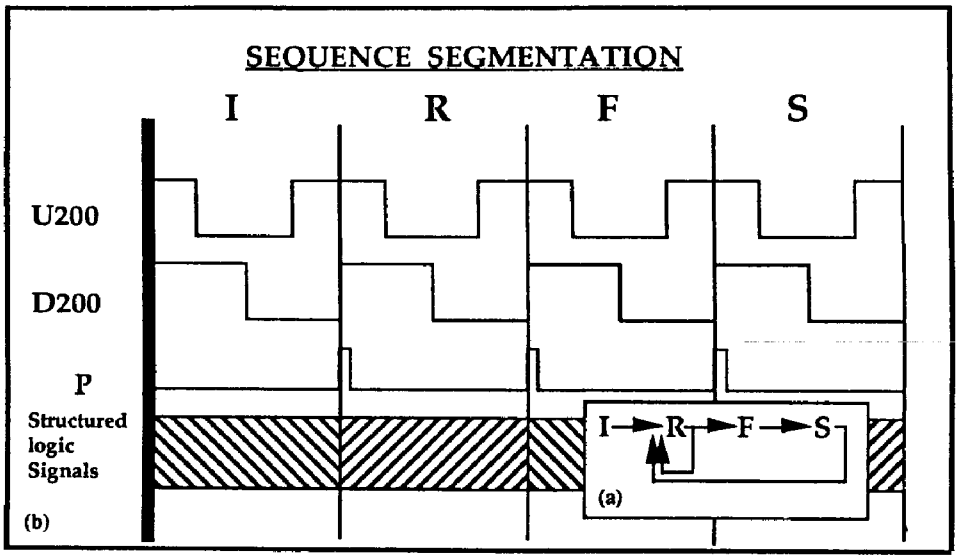

Fig. 3 Sequence Segmentation. (a) The segments are stepped through sequentially, first with I, then with R a number of times equalling the desired integration time minus 5ms, followed by F, and S, after which the new integration begins again at R. This continues for one spin when a sunsync initiates a new I. (b) Within each section the desired signals are structured allowing for the appropriate segmentation.

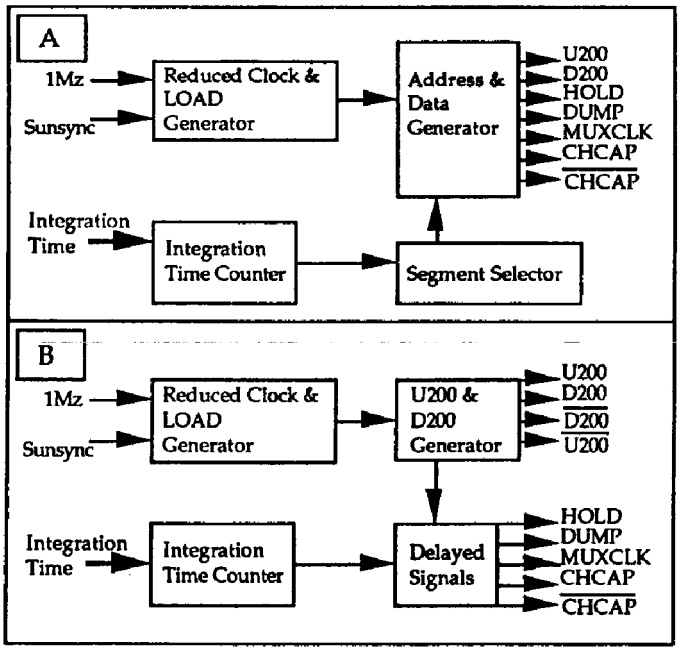

Fig.4 Logic Signal Generation. The logic signals are generated through two methods: (A) using memory, (B) through combinatorial logic.