PC PLUG-IN TELEMETRY DECOMMUTATOR USING FPGAs

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ABSTRACT

This paper describes the design of a PC plug-in card that incorporates all functions of the base band segment of a PCM decommutator which includes the bit synchroniser (BS), frame synchroniser (FS) and subframe synchroniser (SFS). FPGAs are used for the realization of the digital sections of the circuit. The card is capable of handling all standard IRIG codes. The bit synchroniser can handle data rates upto 1Mbps (NRZL), while the frame and subframe synchronisers have been designed to work upto 10 Mbps.

KEYWORDS

Decommutation, Bit Synchronisation, FPGA

INTRODUCTION

This development was aimed at building a portable decommutation system to be integrated into ground stations. Availability of high density FPGAs have made it possible to implement the complete logic in a single PC-XT compatible card. Actel's ACT2 FPGA-based circuits were designed using Viewlogic's design entry and simulation tools. Altera's MAX series EPLD was designed using MAXPLUS tools. The PC interface can program the chips' parameters, display their status and process interrupts generated by the chips while receiving data.

BIT SYNCHRONISER

The important specifications of the bit synchroniser are

- Bitrate : 10 bps to 1 Mbps
- Codes : NRZL, NRZM, NRZS, BIPL, BIPM, BIPS, DMM, DMS

- Input level : ±1V to ±4V
- Bandwidth : 0.1%, 0.3% or 1.0 %

The bit synchroniser is centred around the 4,000 gate A1240 FPGA. A block diagram of the bit synchroniser is given in figure (1). The bit rate clock is derived through a data transition tracking loop (DTTL) and an in-phase integrator is used for bit-recovery. Ambiguity resolution circuit is provided to handle bi-phase signals.
The Automatic Level Correction (ALC) circuit adds an offset to the input signal so that the sum falls within the range of the ADC. Implemented using the AD7523 DAC, its digital input is driven by the ALC estimator block in the FPGA. The analog output is added to the input signal and fed into the Automatic gain control (AGC).

Detailed Block Diagram of
Digital Bit Synchroniser

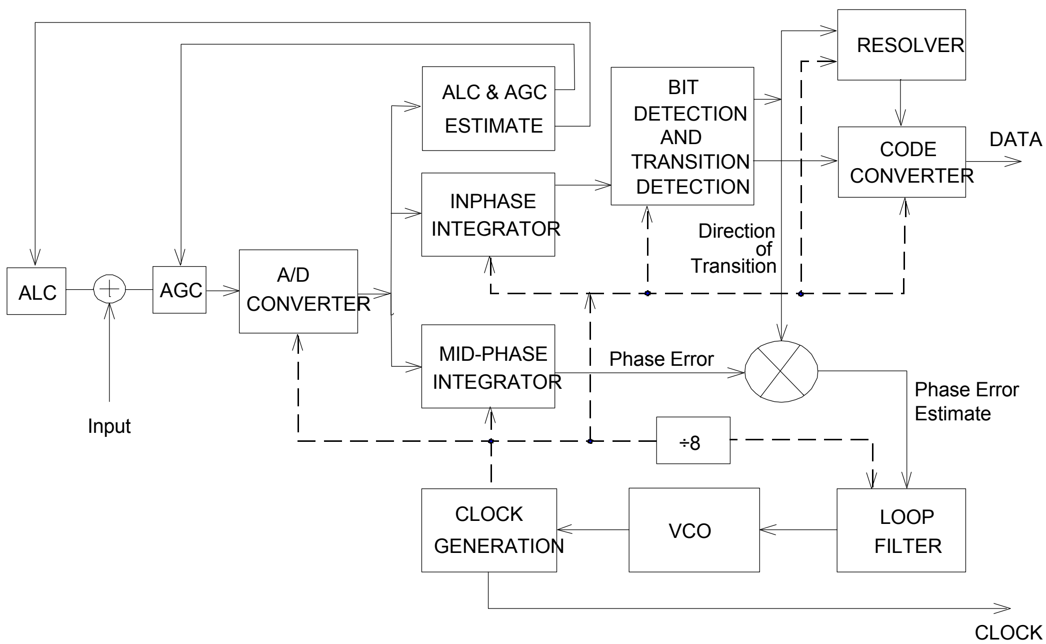

Figure 1

Implemented using the AD7523 in the multiplying DAC mode, the AGC adjusts the amplitude of input signals so that the ADC input is within range. Thus the ALC and the AGC ensure that the resolution of the ADC is always optimally utilised.

The digitising of the appropriately level-shifted and amplitude-corrected input signal is done by the AD9012 ADC. Conversion is done at eight times the bit rate with a resolution of 3 bits.

The ADC output goes to an in-phase accumulator, a mid phase accumulator and the AGC/ALC estimator, all of which are implemented in the FPGA. The 6-bit in-phase accumulator adds the successive outputs of the ADC. A new accumulation cycle is made to start from the beginning of a bit period and to terminate at its end. After 8 samples, the accumulated count is compared with the threshold, which is half the maximum possible value. The output of the comparator is the incoming bit. By XORing the present bit with the previous, a transition can be detected. The transition detector's output is +1 or -1 depending on the direction of the transition and is 0 if there is no transition.

The 6-bit mid-phase accumulator functions similarly except that it's accumulation is made to start from the middle of a bit period and to end at the middle of the next bit period. The accumulated count indicates the phase error of the derived clock with respect to the incoming clock. This value is multiplied with the output of the transition detector which can be ±1 or zero to get the phase error.

The phase error is fed to the loop filter which does an integral+proportional control. This is achieved by adding to the value got by accumulating previous phase errors, a constant multiple of the present phase error. The value of this constant depends on the required bandwidth and can be written into the FPGA through the PC interface. The phase error is converted to an analog value using a DAC that controls the VCO.

The VCO is implemented using a 74LS124 external to the FPGA. When the loop locks, the VCO frequency tracks the incoming bitrate. For an incoming bit rate of 'k' Hz, a number 'n' (a power of 2) is chosen so that the frequency 8kn falls within the range of frequencies that can be generated by the VCO. The VCO frequency can be varied over a 1:2 range and its output is divided by 'n' to get the sampling rate. To handle bitrates from 10 Hz to 1 MHz, the VCO frequency is varied from 4 MHZ to 8 MHz. The sub-multiples of the VCO output of various phases (obtained by division) are used for clocking different blocks of the circuit.

Bi-phase codes are handled by considering them as NRZL codes at twice the bit rate. The ambiguity resolution circuits needed for bi-phase codes work on the principle of detecting invalid bit patterns. The code converter block generates the corrected clock and converted data.

FRAME SYNCHRONISER

The important specifications of the frame synchroniser are

- Frame Sync Pattern length : 32 bits
- Word length : 32 bits
- Frame Length : 1024 words
- Bit Error Tolerance : upto 25%
- Bit Slip Tolerance : ±2 clocks

The basic function of the FS is to detect the presence of the Frame Sync Pattern (FSP) in the input bit stream, which marks the beginning of a frame. It also indicates, depending on the regularity of the FS pattern, the quality of the data received and uses the 'search-check-lock' strategy. In the 'search' mode, the FS searches for the FSP. Once this is got it goes into the check mode where it checks for the regular occurance of the FSP in the succeeding frames and if it does, it goes into the lock mode and maintains lock until there is a marked disruption in the arrival of the FSPs in the bitstream. The FS gives out two 'rate pulses': the frame rate which indicates the beginning of the frame, and the word rate which indicates the beginning of a word.

The main features of the frame synchroniser are

- implemented in a single chip: Actel's 8,000 gate A1280 FPGA
- capable of handling input bit rates upto 10 Mbps
- uses a 5-stage pipelined correlator to achieve high operating frequency
- needs only one input clock: the zero-degree bitrate clock
- dynamically adapting threshold
- data inversion detection and correction
- fully sequential design, optimised for the ACT2 FPGA

SUBFRAME SYNCHRONISER

The important specifications of the subframe synchroniser are

- Recycle Pattern length : 32 bits
- Location of pattern : anywhere in the frame
- ID Word Length : 8 bits
- ID Count Direction : up or down

The basic function of the SFS is to detect the presence of the Subframe Synchroniser Pattern (the recycle code or the ID word) in each frame. Like the FS, the SFS also indicates, depending on the regularity of the SFS pattern, the quality of the data received and employs a similar 'search-check-lock' strategy. The SFS gives out the 'sub frame rate' which indicates the beginning of the sub-frame.

The main features of the subframe synchroniser are

- implemented using a single chip: Actel's 4,000 gate A1240 FPGA
- works upto 10 Mbps
- single clock, fully sequential, FPGA optimised circuit

The SFS can also work with 'reversed' data like that coming from a tape playing in the reverse direction. Provision is also made to bypass the whole chip, if necessary.

The PC bus interface is implemented using the MAX 5128 EPLD.

CONCLUSION

The PC plug-in decommutator as described above has been realised and tested upto 1Mbps (NRZL), and found to perform satisfactorily. Since the data after synchronisation is available inside the PC itself, the acquisition and further analysis of the data can be easily done using available PC based tools. By making use of PC resources, this design saves cost by eliminating supporting interfaces necessary for an independent system and makes the testing of the hardware easier.

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