A CCSDS COMPATIBLE HIGH-RATE TELEMETRY FORMATTER FOR SPACE APPLICATION

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ABSTRACT

OSC is presently developing a high-rate telemetry collection and formatting component for NASA's EOS-AM1 spacecraft. This device, called the Science Formatting Equipment, is capable of collecting data at aggregate rates exceeding 130 Mbps. The collected data is formatted into CCSDS compatible data structures, error coded, and then routed either to a downlink output or to a recording device at data rates up to 150 Mbps. This paper serves as a brief introduction to this component.

KEY WORDS

Science Formatting Equipment, CCSDS, EOS, High-Rate Telemetry

INTRODUCTION

In terms of instrument data rates and the amount of science data generated, NASA's EOS-AM1 spacecraft, scheduled for launch in 1998, presents several exciting challenges. An electronic component called the Science Formatting Equipment (SFE) is at the heart of the science telemetry gathering function. Orbital Sciences Corporation (formerly Fairchild Space Company) is presently under contract to develop and manufacture the SFE. The SFE is responsible for collecting all of the spacecraft's science instrument data, formatting the data into frames compatible with the Consultative Committee for Space Data Systems (CCSDS) recommendations, and routing the formatted data to selected RF transmitters or solid state recorders.

As shown in Figure 1, the SFE accepts data from 12 science instruments that fall into 2 categories. Six of the instruments are designated as being "high-rate" and interface to the SFE using dedicated point-to-point links. When operating at their maximum rates, the 6 high-rate instruments chosen for EOS-AM1 generate data at the following rates: VNIR1=31.019 Mbps, VNIR2=31.019 Mbps, SWIR=23.053 Mbps, MODIS=10.800 Mbps, MISR=6.500 Mbps, and TIR=4.109 Mbps. The other 6

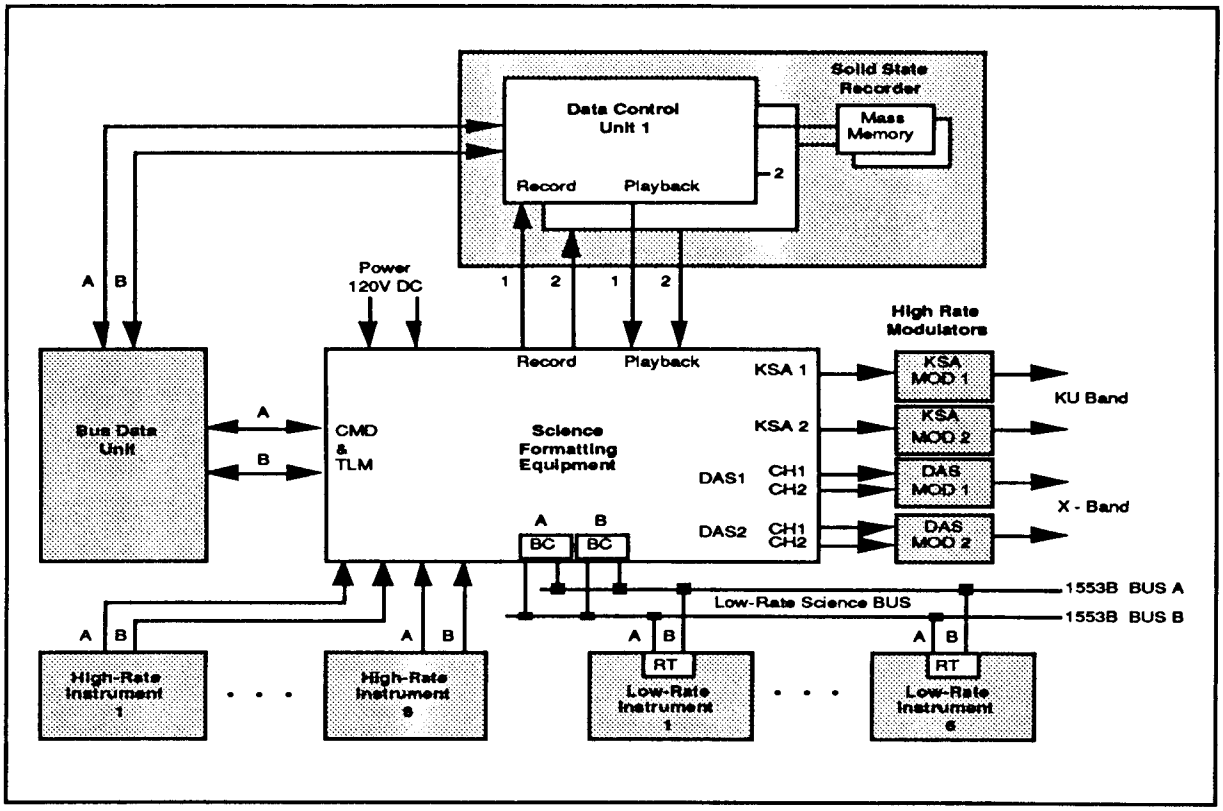

Figure 1: Block Diagram of the Science Telemetry Section of the EOS-AM1 Spacecraft

instruments are designated as being “low-rate” and share a redundant MIL-STD-1553B serial data bus interface to the SFE. When all of the low-rate instruments are operating simultaneously at their maximum rates they generate a total of 65 kbps.

The data received from all of the instruments is in the form of CCSDS compatible source packets. The major function of the SFE is to collect these variable length packets and embed them within fixed length data structures called Channel Access Data Units (CADUs).

The format of the EOS-AM1 CADU and other related data structures is shown in Figure 2. In CCSDS terminology, the SFE provides the Multiplexing and Virtual Channel functions.

The CADUs generated by the SFE are routed to 1 or more of several outputs including modulators and a Solid State Recorder (SSR). The configuration/status of the SFE is controlled/monitored via an external Bus Data Unit (BDU).

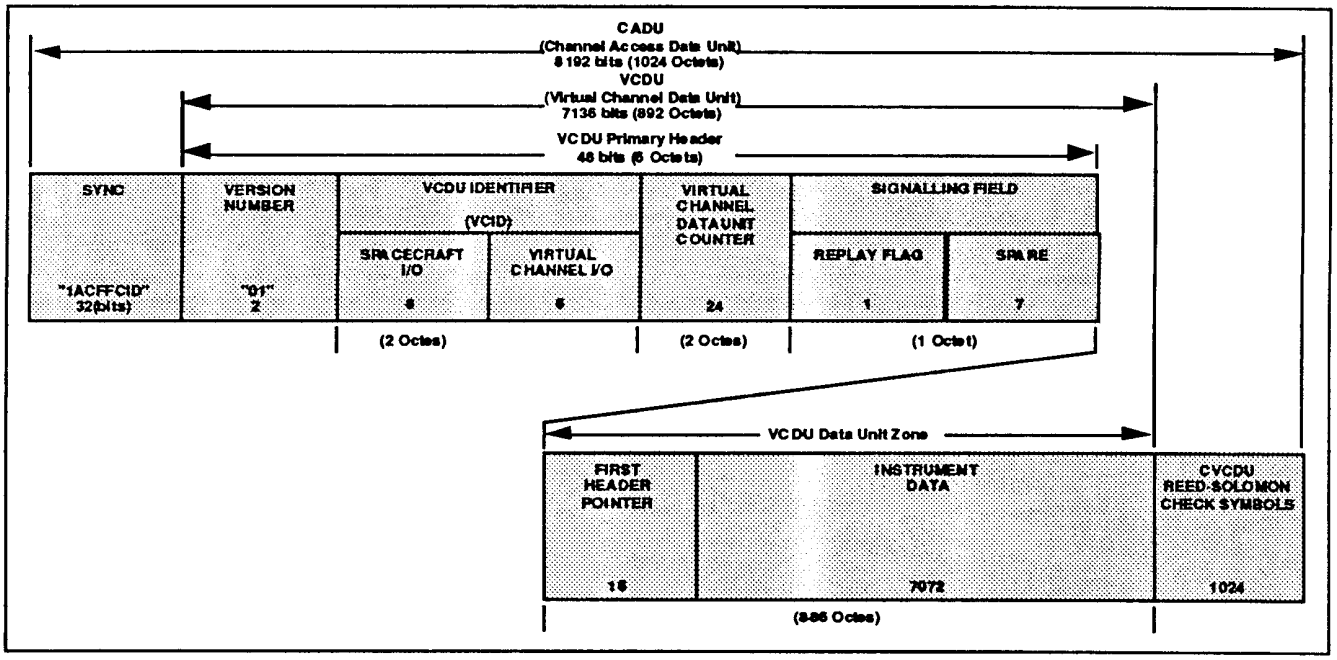

Figure 2: CCSDS Science Telemetry Frame Format

ARCHITECTURE OF THE SFE

The block diagram of the internals of the SFE is shown in Figure 3. This block diagram functionally shows half of a redundant configuration.

The 2 types of instrument interfaces are shown on the input (left-hand) side of Figure 3. High-rate instruments utilize dedicated, point-to-point electrical links to output their packetized data to a High-rate Packet Multiplexer (HPM) card at rates up to 50 Mbps. Each HPM card can service up to 3 such interfaces. Low-rate instruments utilize a 1553B serial data bus to transport their packets to the SFE's Low-rate Packet Multiplexer (LPM) card. The LPM card also provides the Command & Telemetry interface to the spacecraft computer via a BDU. As implied by the name, the Packet Multiplexer cards multiplex the received instrument data packets into fixed-length, CCSDS data structures called Virtual Channel Data Units (VCDUs) that are routed to the High-rate Downlink Interface (HDI) card via a backplane. The HDI prepends header information and appends Reed-Solomon check bits to the frame to form CADUs which are then routed to 1 or more RF modulator or Solid State Recorder outputs via the Frame Router (FR) card.

As mentioned above, the HPM, LPM, and HDI cards utilize a backplane interface to communicate with one another and to transport data. The industry standard Multibus II Parallel System Bus (PSB) was chosen to serve this function. The 32-bit wide PSB has a gross data transfer capability of 320 Mbps. One of the key reasons for choosing

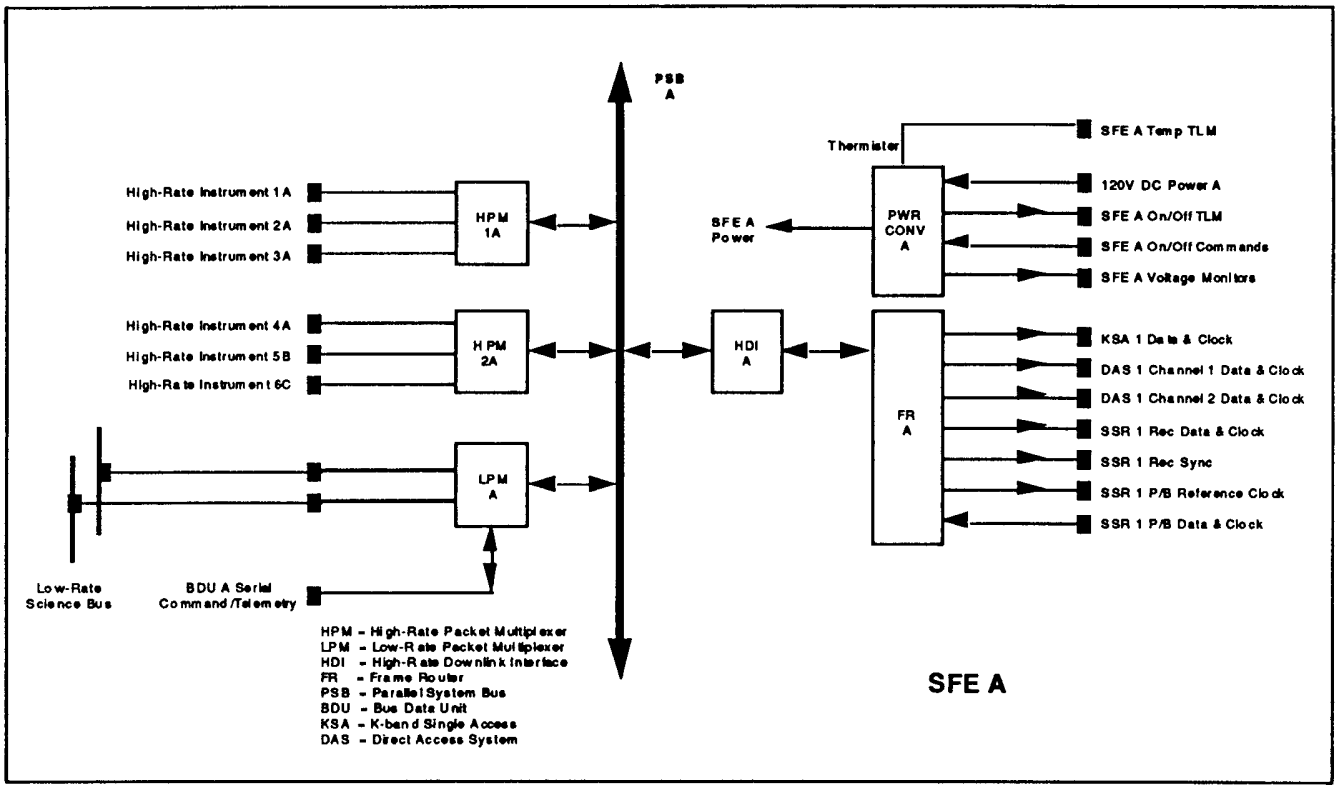

Figure 3: Block Diagram of the SFE

the PSB was the availability of a very efficient, low overhead transport mode called solicited messaging. It is this mode that is used to transport the frames between the SFE's Packet Multiplexers and the HDI cards.

A key design feature of the SFE is that while the external data interfaces are either serial (the instrument inputs) or 4-bit wide (the modulator outputs), most internal data paths are 32-bits wide. This allows the maximum use of low-power CMOS circuitry.

ELECTRONIC CARDS WITHIN THE SFE

As discussed above, the SFE contains 4 electronic card types, a backplane, a power supply, and a chassis. All functions are redundant. For redundant signal routing reasons, electronic card redundancy is accomplished by including 2 electrically isolated sets of circuitry on each printed circuit card.

High-rate Packet Multiplexer

The block diagram for the HPM card is shown below in Figure 4.

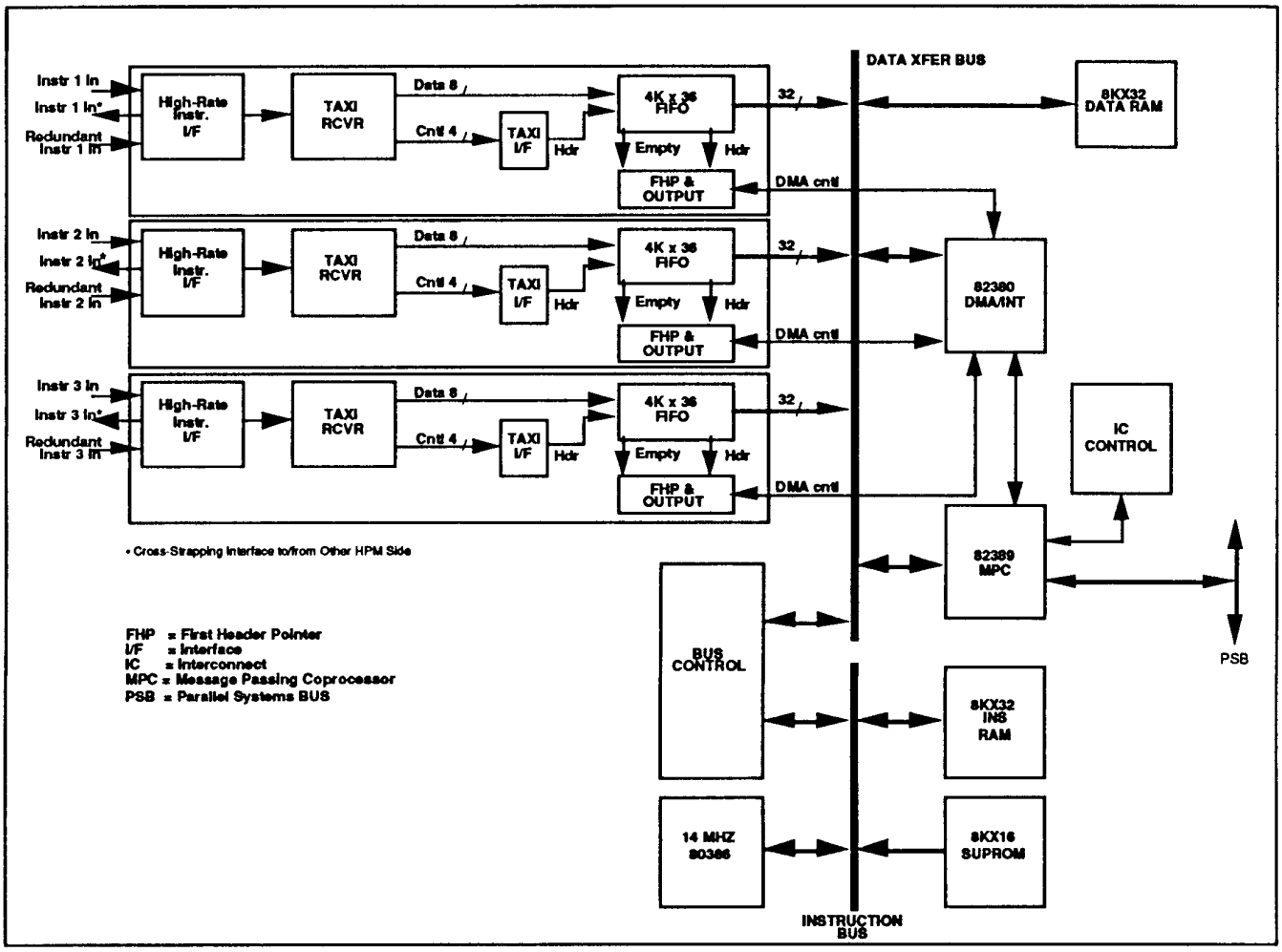

Figure 4: Block Diagram of the High-rate Packet Multiplexer Card

The HPM consists of 3 sections: a high-rate instrument interface section that services 3 instruments, a Direct Memory Access (DMA) based data transfer section, and the microprocessor based control section. As can be seen in this figure, the design is based around the Intel 80386 microprocessor and related family parts.

Each high-rate instrument interfaces to the SFE via an electrical serial data interface that utilizes a 4B/5B ("TAXI") encoding scheme. Although the instruments data rate varies depending on the instrument, the signaling rate across this link is always at 50 Mbps. A simplex protocol has been defined that uses TAXI control codes to delineate instrument packets. Each of the 3 high-rate instrument interfaces consists of a latching relay based redundancy switching front-end, an AMD 7969 TAXI receiver, a PAL that is used to detect packet control codes, a 4Kx36 FIFO stage that is used to buffer the incoming data, and a control Actel FPGA.

Under control of the 82380, Direct Memory Access (DMA) techniques are utilized to transfer the instrument data into the Data RAM where the VCDU data structures are built. To conserve DATA XFER BUS bandwidth, a dynamically sizing demand transfer DMA technique is utilized. When enough data for a particular instrument has been transferred to the Data RAM to fill a VCDU, the VCDU is queued for transport and the building of a new VCDU is initiated. Completed VCDUs are transferred to the HDI cards via the PSB under control of the 82389 Message Passing Coprocessor. To conserve bandwidth, the DMA solicited messaging capability of the PSB is utilized.

All of the HPM functions described above are controlled and coordinated by the 80386 microprocessor and associated PROM, instruction RAM, and software. In addition, control messages received over the PSB (from the LPM) are handled by the 80386. A split-bus architecture is utilized to isolate instruction fetch overhead to the INSTRUCTION BUS thus freeing up DATA XFER BUS resources. With this architecture, the HPM card is capable of supporting aggregate instrument data rates (from all 3 interfaces) at rates up to 65 Mbps.

Low-rate Packet Multiplexer

The block diagram for the LPM card is shown in Figure 5.

The LPM consists of 5 sections: a low-rate instrument interface section, a Command and Telemetry interface section, a Central Services Module section, a Direct Memory Access (DMA) based data transfer section, and the microprocessor based control section. Where feasible, the design of the LPM card is based on that of the HPM card and the LPM's DMA and control sections are nearly identical to the corresponding sections on the HPM.

In lieu of the high-rate instrument interface circuitry on the HPM, the LPM contains a MIL-STD-1553B serial data bus to interface to the 6 low-rate instruments. The United Technologies UTBCRT component configured as a Bus Controller is used as the centerpiece of this functionality. The 1553 RAM (shown in Figure 5) is used to hold the polling tables and as a temporary buffer for the resulting RT data. Similar to the HPM, DMA techniques are used to build VCDUs in the Data RAM which are then transferred to the HDI via the PSB.

The Parallel Systems Bus requires certain functions such as clocks and time-outs to be provided. These Central Service Module (CSM) functions are provided by the LPM card.

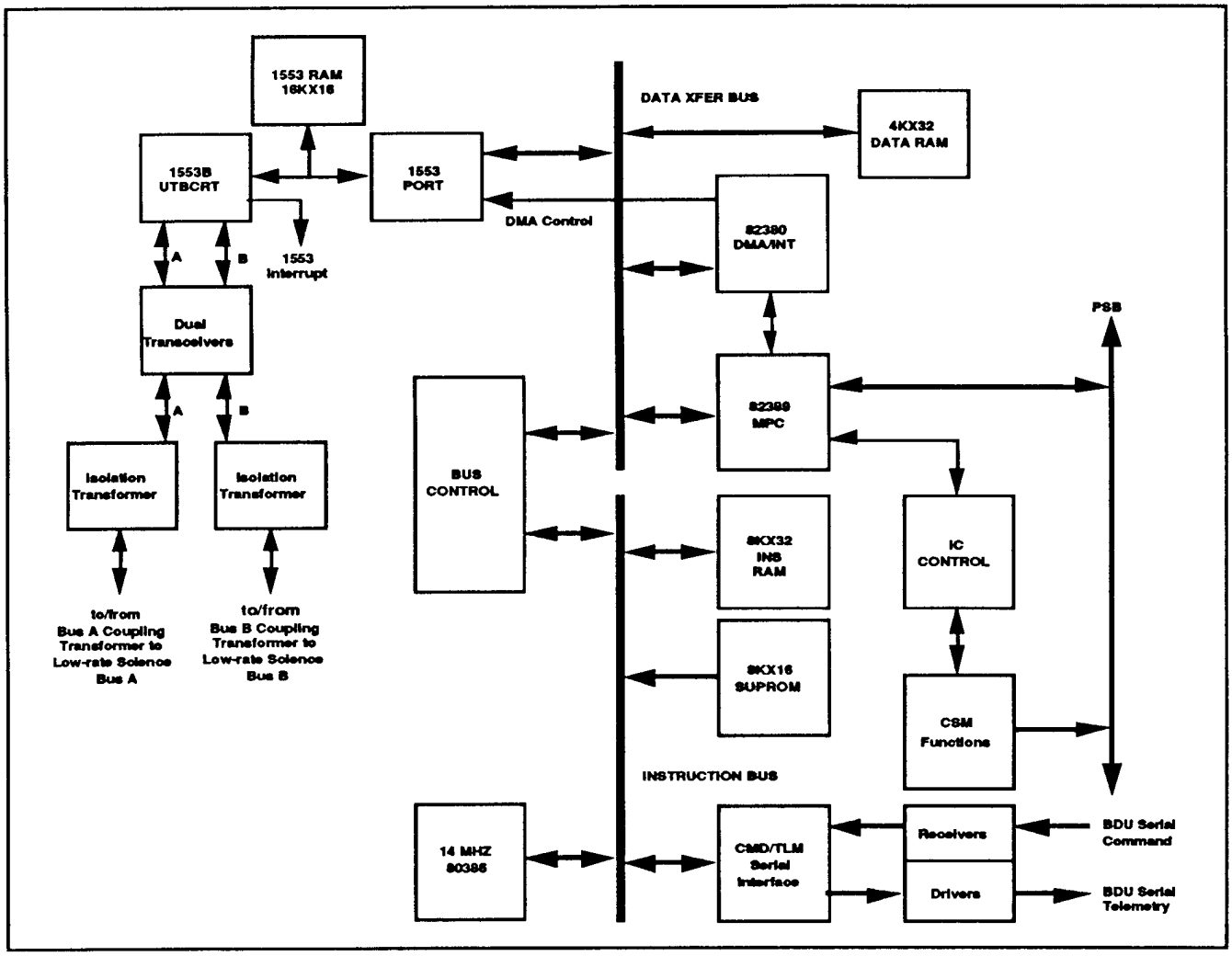

Figure 5: Block Diagram of the Low-rate Packet Multiplexer Card

In addition, the LPM card provides the serial command and telemetry interfaces to the external Bus Data Unit. The LPM hardware and software receives serial commands from the BDU, interprets them (based on pre-defined formats), and distributes needed information to other cards as necessary via the PSB. In the other direction, the LPM

periodically polls the other cards for status information and provides this telemetry information upon request to the BDU.

High-rate Downlink Interface

The block diagram for the HDI card is shown in Figure 6.

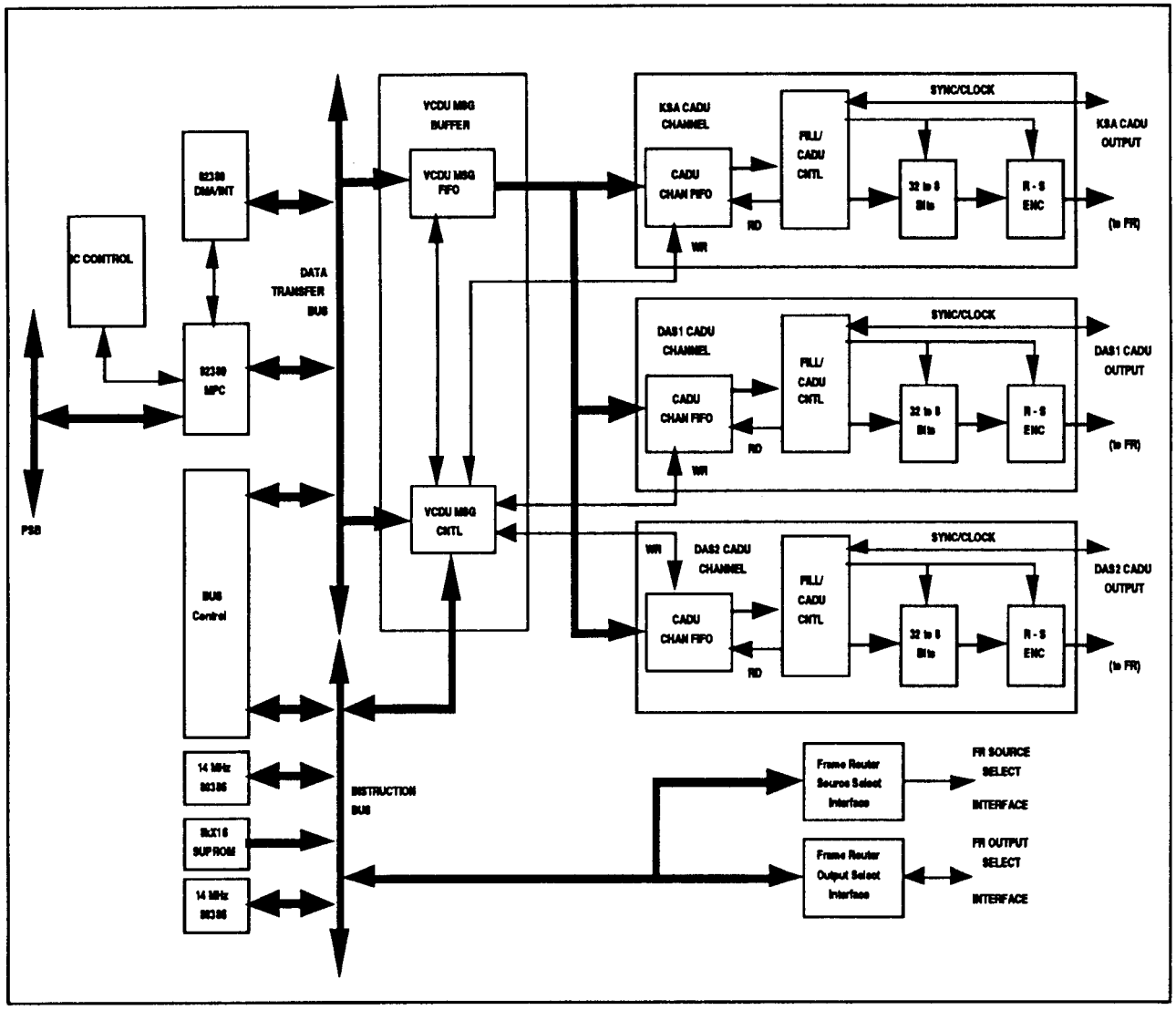

Figure 6: Block Diagram of the High-rate Downlink Interface Card

The HDI consists of 4 sections: a CADU building section, a Frame Router control section, and DMA/control sections similar to the corresponding sections on the HPM and LPM cards.

The CADU builder is one of the more complex hardware functions within the SFE. As VCDUs are received over the PSB from the packet multiplexer cards (HPM and LPM), DMA techniques are used to transfer them into the common VCDU message buffer FIFO. When a complete VCDU is successfully received into this buffer (the PSB protocol takes care of retransmissions if necessary), then 1,2, or all of the 3 CADU channel FIFOs are enabled to receive the VCDU. Each of the CADU builders is controlled by a state machine

FPGA (called Fill/CADU Cntl in Figure 6). The functions of this FPGA are to prepend the 32-bit CADU synchronization field and route the data through the Reed-Solomon encoder. The timing for these functions is driven from external signals received from the Frame Router card to which the 3 CADU channels are connected. Since CADUs are synchronous, fixed-length structures that are continuously generated, another function of the control FPGA is to produce "fill" CADUs when necessary (i.e., the CADU Chan FIFO is empty when the start of a new CADU is imminent).

The CADU outputs from the HDI are routed via a local bus interface to the Frame Router card. The control information for configuring the FR is maintained on the HDI card.

Frame Router

The block diagram for the FR card is shown in Figure 7.

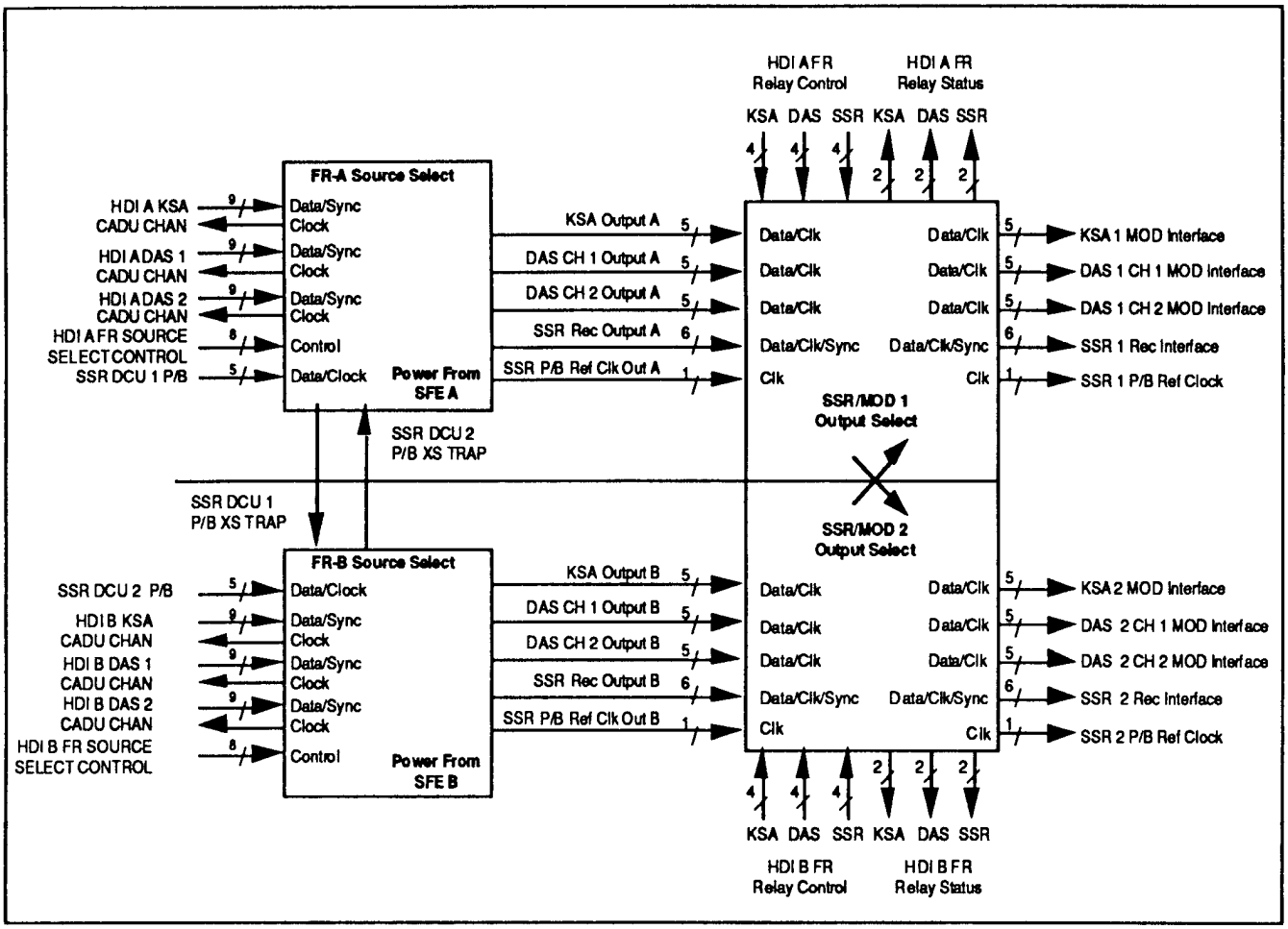

Figure 7: Block Diagram of the Frame Router Card

The FR card is a peripheral card to the HDI card and interfaces to the HDI card via a dedicated local bus interface. The FR card receives three 8-bit wide, FEC encoded data streams from each (redundant) side of the HDI card and one 4-bit wide playback data stream from each redundant portion of the Solid State Recorder. These data streams are routed (switched) to 4 redundant sets of 4-bit wide outputs - 3 (redundant) RF modulator outputs (KSA 1/2, DAS 1/2 CH1, and DAS 1/2 CH2) and a redundant Solid State Recorder record interface. Depending on the interface, the outputs can operate at data rates up to 150 Mbps. All data rate clocks and their derivatives are sourced from the FR card.

The required configuration information (switch matrix, clock rates, etc.) is maintained in the HDI and loaded into the FR as needed via an interface dedicated to this function. The actual FR configuration can also be read by the HDI from the FR via this same interface.

CONCLUSIONS

With interfaces up to 150 Mbps, the design of the EOS-AM1 Science Formatting Equipment required innovative approaches to meet the mission requirements while maintaining reasonable weight and power consumption. The OSC design approach utilizes the widely accepted Parallel Systems Bus interconnect architecture coupled with efficient card functionality partitioning to accomplish the required functions. A detailed discrete event simulation of the SFE was constructed and utilized to assist with design decisions and verification. As of June 1995, the SFE Engineering Test Unit has successfully verified that the design concept is sound. The flight version of the SFE will be delivered to the prime contractor early in 1996.