FIELD PROGRAMMABLE GATE ARRAY BASED MINIATURISED CENTRAL CONTROLLER FOR A DECENTRALISED BASE-BAND TELEMETRY SYSTEM FOR SATELLITE LAUNCH VEHICLES

Krishnakumar M., Sreelal S., Narayana T. V., Anguswamy P., Singh U. S.
(Electronics Group, Vikram Sarabhai Space Centre,
Indian Space Research Organisation, Trivandrum 695022, India)

ABSTRACT

The Central Control Unit (CCU) for a decentralised on-board base-band telemetry system is designed for use in launch vehicle missions of the Indian Space Research Organisation (ISRO). This new design is a highly improved and miniaturised version of an earlier design. The major design highlights are as follows: usage of CMOS Field Programmable Gate Array (FPGA) devices in place of LS TTL devices, high level user programmability of TM format using EEPROMs, usage of high density memory for on-board data storage and delayed data transmission, HMC based pre-modulation filter and final output driver etc. The entire system is realised on a single 6 layer MLB and is packaged on a stackable modular frame. This design has resulted in a 1:4 reduction in weight, 1:4 reduction in volume, 1:5 reduction in power consumption and 1:3 reduction in height in addition to drastic reduction of part diversity and solder joints and thus greatly increased reliability. This paper discusses the design approach, implementation details, tools used, simulations carried out and the results of detailed qualification tests done on the realised qualification model.

KEY WORDS

Field Programmable Gate Array (FPGA), Telemetry (TM) Format, Hybrid Micro Circuit (HMC), Very Large Scale Integration (VLSI)

INTRODUCTION

The launch vehicle missions of ISRO require the measurement and monitoring of a large number of parameters such as pressure, temperature, acceleration, vibration etc. A Decentralised Programmable Onboard Pulse Code Modulation Telemetry System is used for this purpose. It performs the following functions:

(a) Data acquisition and processing (if necessary).

(b) Telemetry formatting (encoding) as per Inter Range Instrumentation Group (IRIG) telemetry standards .

The system consists of a Central Control Unit (CCU) located near the RF transmitter and several Remote Units (RUs) located near the data sources connected by a differential, bi-directional, serial bus conforming to physical interface reqirements of MIL-STD-1553. The CCU performs the following functions:

(a) Provide the baseband PCM telemetry data as per the format(s) stored in memory.
(b) Address the RUs in sequence as dictated by the format(s).
(c) Accept the serial reply from addressed RU.
(d) Provide on-board data storage for delayed data transmission.
(e) Provide on-board data storage for the LS bits of data whose word length exceeds the telemetry word length.
(f) Provide system level interface to the on-board RF transmitter.
(g) Provide system level interface to the on-board computer for in-flight format switching.
(h) Provide suitable interface for the ground checkout system.

This paper discusses the design and development of a highly improved and miniaturised version of CCU. The major functional improvements over the earlier design are as follows:

(a) Field programmability of the telemetry format without unit dis-assembly or component desoldering by the usage of E ^{2}PROM based format storage.
(b) Provision for on-board time reference with 1ms. accuracy / resolution.
(c) Improvement of bit rate stability by the usage of digital, programmable frequency divider.

In addition the unit also provides all the inherent advantages of miniaturisation due to the usage of the following VLSI devices:

(a) CMOS Field Programmable Gate Arrays (FPGAs) of 2000 gate density from ACTEL Corp. to replace discrete TTL devices.
(b) High density RAM (1 MB) for temporary storage of delay and high resolution data.
(c) High density E^{2}PROM (256 KB) for storage of telemetry format.
(d) Custom Hybrid Micro Circuits (HMCs) for the analog circuits at the output stage.

The salient design requirements / specifications are given in Table 1. The design features, configuration and verification (simulation, implementation and test) are covered in the following sections.

DESIGN FEATURES

The CCU is a micro-programmed, pure hardware architecture where the micro-program stored in E ^{2}PROM is 40 bits wide. For each telemetry word, one of the following types of data has to be output, depending on the format:

(a) Frame Sync / Frame Identification code.
(b) RU data from one of 4 groups of RUs.
(c) Delay memory data.
(d) LS 4 bit data of 12 bit data words.
(e) Upper / Middle / Lower byte of 24 bit time reference code.

The 40 bit wide micro-program code is accessed by reading the byte wide E ^{2}PROM 5 times for each 8 bit telemetry word. The contents of this memory can be down-loaded externally from a PC under software control through one of the RU links. Hence the format is fully field programmable and docs not require disassembly of the package. This is done after putting the unit in program mode to distinguish it from flight mode in which the normal functions are performed.

DESIGN CONFIGURATION

The block diagram of CCU is given in Figure 1. The heart of the system is the Control and Timing (CAT) FPGA which generates the core control signals for the rest of the circuitry. Four times the output bit rate is used as the basic clock. The cycling of the system is controlled by the format stored in E ^{2}PROM. The 40 bit contents of format memory for each telemetry word are given in Figure 2. During the duration of a single telemetry word the following actions are performed by the CCU:

(a) Read the 40 bit contents of the format memory.
(b) Send the address to the appropriate RU (whose data is to be output in the telemetry bit stream 16 words later).
(c) Receive the reply from the appropriate RU (which was addressed 12 words earlier). 4 word periods are required for the received data to be parallelised, encoded and inserted into the output bit stream.
(d) Write the data received from RU into the RAM if it is to be delayed or is a 12 bit one.

(e) Select the data to be given to the final output from various data sources (IOIF FPGA for RU data, RAM for delay and LS 4 bit data, E ^{2}PROM for frame sync / frame identification code and the 24 bit timer for time reference code).

In addition to generating all the control and timing signals required for the above operations, the CAT FPGA also encodes the output data in serial Bi-Phase form and delivers the Clock, Word rate and Major frame rate signals for checkout port.

The RU interface circuit consists of line drivers, line receivers and pulse transformers and conforms fully to the physical interface requirements of MIL-STD-1553. The random logic requirements of 2 groups of RUs are met by a single FPGA (IOIF) and 2 of these are used to cater to the requirement of 4 I/O groups. This FPGA basically provides peripheral support for 15530 Manchester encoder / decoder, multiplexes the return data from RUs and generates the control signals for in-circuit programming of format memory in program mode of operation. It triggers the encoding cycle for each group on command from CAT FPGA and provides decoded data on request.

Group 0, RU0 link performs the additional function of providing interface with host computer in program mode of operations. The following functions can be performed in this mode:

(a) Write data to any location of format E ^{2}PROM.
(b) Read data from any location of format E ^{2}PROM.
(c) Write data to any location of delay / LS 4 bit RAM.
(d) Read data from any location of delay / LS 4 bit RAM.
(e) Enable / disable the software write protect of format E ^{2}PROM.

The sequence of data to be sent from host computer for one memory access operation is:
MSB of address $\Rightarrow$ LSB of address $\Rightarrow$ Data (irrelevant for read).
It may be noted that the 8 bits as above constitute the LS byte of 16 bit 1553 data and the MS byte contains a 4 bit identification field indicating the nature of data. Thus in addition to programming the telemetry format, the program mode also enables the diagnostics of on-board RAM. It may also be noted that the capability of locking the E^{2}PROM and the fact that the unit goes into program mode only if 2 external connector pins are pulled low ensure that inadvertant changes do not occur in the format memory contents while the unit is powered up or is in normal mode of operation.

The RAM-ADGN FPGA does the address generation for the delay data memory as well as LS 12 bit data memory. The 1MB memory is mapped for these operations are as follows :

(a) 00000 - 0FFFF : Delay RAM
(b) 1FF00 - 1FFFF : LS 12 bit data

Writing the delay data is done sequentially while reading is random. Hence the write address is generated by a 16 bit counter and the read address is evaluated from another 16 bit counter and a 9 bit offset read from format memory. The write counter and read counter are initially loaded with 16 bit constants, so that the reading will always be delayed with respect to writing by the required integral number of major frames.

Address generation for LS 4 bit data is simpler since all the data written in a major frame is read in that major frame itself. Hence the write address is generated by an 8 bit counter and the read address is latched from format memory.

The bit rate generation logic divides the oscillator frequency by an integer number to generate 4 times the bit rate clock required for the CAT FPGA. This logic is implemented using discrete ACT (Advanced CMOS Technology) devices due to I/O and speed limitations of FPGA. The CCU also features a format and bit rate switching and time reference reset capability. These functions are invoked by external commands received through a differential, opto-isolated interface.

The Bi-Phase(L) digital data output of CAT FPGA is subjected to the following analog processing by two 24 pin custom HMCs before it is output from CCU :

(a) Level shifting for converting the unipolar data to bipolar form.
(b) Filtering to limit the bandwidth of the signal modulating the RF carrier in the down-stream transmitter to 1.4 times the bit rate. Two 6 pole linear phase (Bessel) filters are employed for this purpose (for the two bit rates).
(c) Selection of the appropriate filter output by an analog switch as per the format change-over command status.
(d) Amplification to boost the output level and driving to 50 Ωoutput resistance as per the requirements of RF transmitter.

DESIGN VERIFICATION

The design verification was performed in two phases: extensive simulation using sophisticated CAE software and testing as per the flight acceptance guidelines of our organisation.

SIMULATION

Simulation was carried out in 3 phases :

(a) FPGA chip level simulation using Workview software from Viewlogic Systems Inc. on PC486. This consists of unit delay logic simulation to ensure the circuit functionality and post-route timing simulation after design validation and placement & routing to ensure at-speed performance.

(b) Board level digital simulation using DAZIX EDA environment from Intergraph Corp. on SUN platform. Here the FPGAs were modelled by EDIF 200 netlists, 15530, E ^{2}PROM and RAM by Logic Automation Behavioural models and miscallaneous digital logic by DAZIX library models. This simulation helped to establish the compatibility of FPGAs to the rest of digital logic.

(c) Analog simulation of the 2 HMCs using Accusim software from Mentor Graphics Corp. on Appollo DN 3500 platform. This helped in understanding the design margins of the analog portion of the design.

TESTING

A qualification model of the system was realised as a single 6 layer PCB mounted on a mechanical frame which is stackable over the RU and accompanying DC-DC converter. It gave advantages of 4.2:1 in weight, 4.9:1 in volume and 4.4:1 in power consumption when compared to the old version of the unit. In addition the modularity of mechanical design ensures "plug-and-play" capability with RUs. A complete suite of software tools were developed to convert the telemetry format to the format memory contents, down-load this to the CCU in program mode and then verify all the flight mode functions. Extensive testing at extreme environmental conditions of temperature, EMI, humidity etc. and vibration, shock etc. has established the quality of the package as per flight acceptance requirements.

CONCLUSION

A Central Control Unit (CCU) for a decentralised on-board base-band telemetry system has been designed using VLSI devices like CMOS FPGAs with high level user programmability of TM format using EEPROMs, usage of high density memory for on-board data storage and delayed data transmission, HMC based pre-modulation filter and final output driver etc. This design has resulted in considerable reduction of weight, volume and power consumption in addition to drastic reduction of part diversity and solder joints and thus greatly increased reliability when compared to an

earlier version of the design. The system has been realised and tested to flight acceptence norms of our organisation. Future work will aim at single-chip realisations of digital and analog functions and incorporation of higher level of intelligence, software programmability etc.

ACKNOWLEDGEMENTS

The successful design, realisation and testing is the result of a number of highly competent engineers and technicians as well as top level management support. We sincerely acknowledge their contributions. However, the following individuals deserve special mention. Dr. S. Srinivasan, Director, VSSC for keen interest and permission to publish this work, Dr. S. C. Gupta (Distinguished Professor, ISRO & previous Director, VSSC) for consistent support and encouragement, Shri R. M. Vasagam (Director, Directorate of Advanced Technology Planning, ISRO & previous Deputy Director, VSSC (Avionics)) for providing sustained inspiration and technical guidance, Smt. G. Padma and Shri S. Vasudevan Potti for technical support, Shri C. A. Ignatious and Shri K. T. Oommen Tharakan for technical discussions, Shri H. Surendra for realisation support, Shri K. Anand and Shri A.T. Rajeev for test and evaluation and Shri N. Govidarajulu and Shri R. Syamalakumaran for mechanical package design, HMC facility for HMC part realisation and Shri K. Damodaran for management and budgetary support.

Number of formats	:	2
Format size	:	3276 words (max)
Bit rate (nominal)	:	1 Mbps (max)
Word length	:	8 bits
Number of I/O groups	:	4 (max)
Delay memory capacity	:	64 Kbytes
Number of delay data per major frame	:	512 (max)
Number of 12 bit data per major frame	:	256 (max)
Time reference accuracy / resolution	:	1 ms.

Table 1 Salient design requirements/ specifications

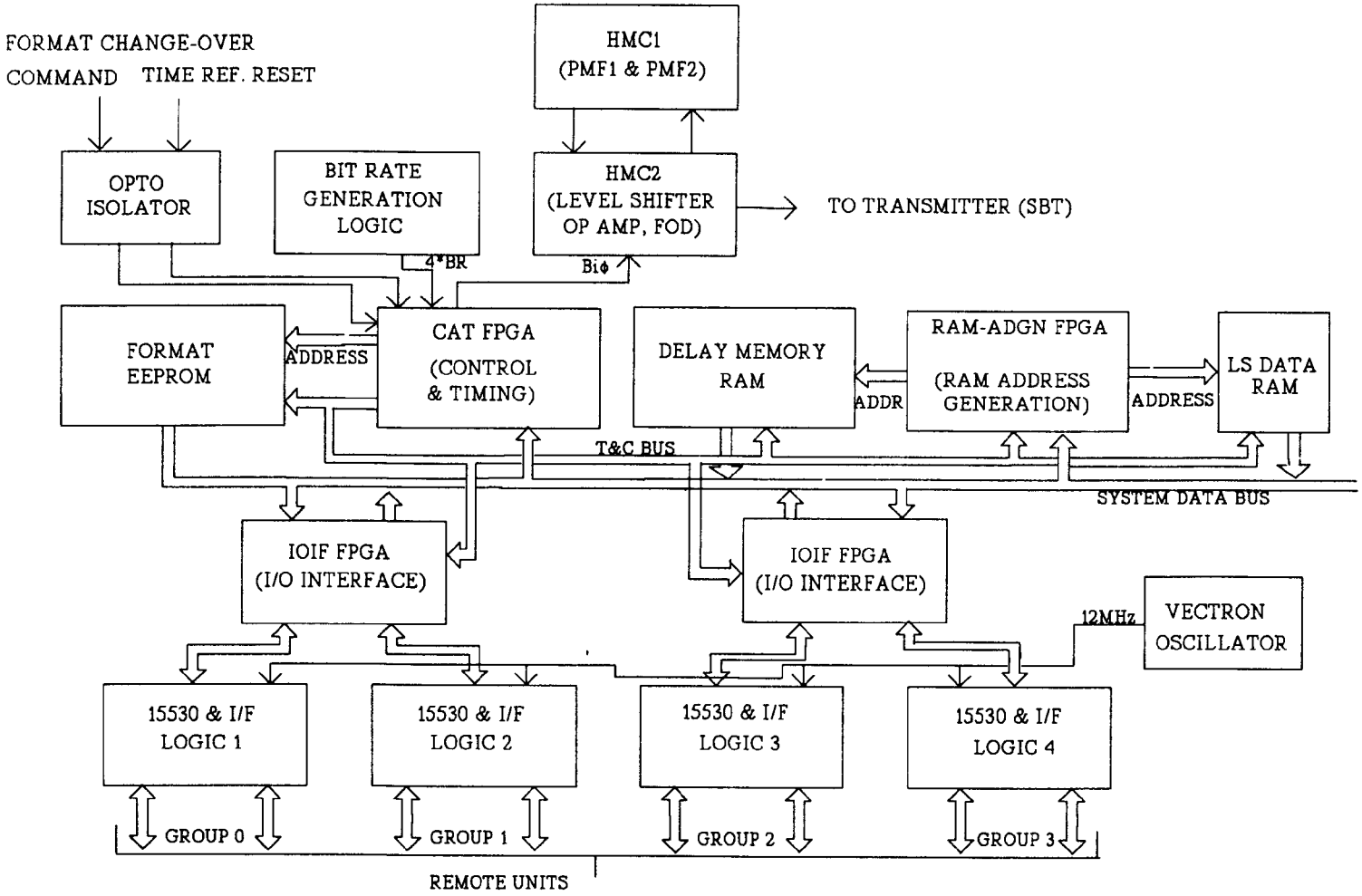

Figure 1 Block Diagram

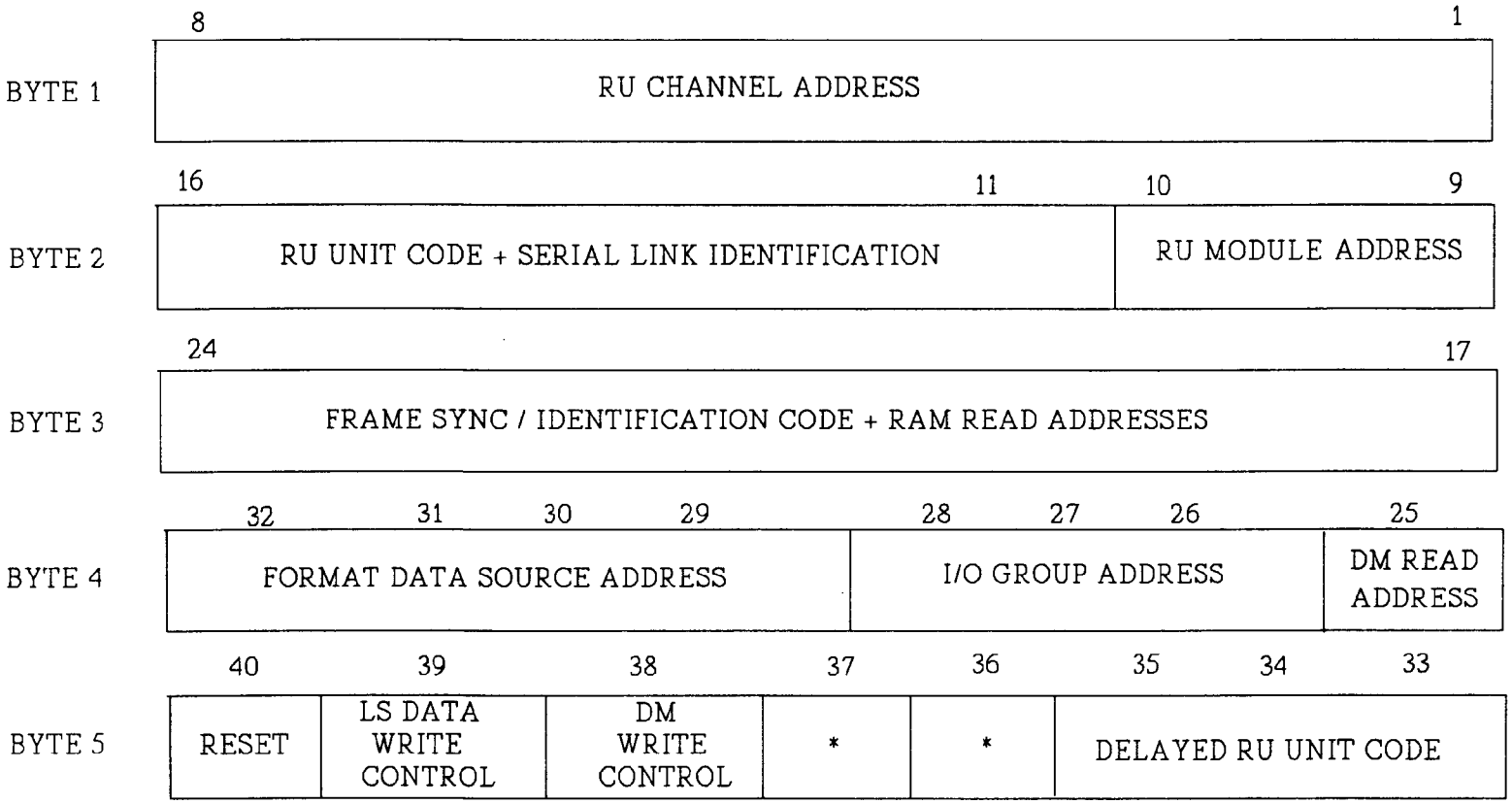

Figure 2 Format Memory Allocation