A SMALL STATE-OF-THE ART RANGE SAFETY TELEMETRY SYSTEM

Wes Lingerfelt
Engineer Specialist
ITT Federal Services Corp.
Vandenberg AFB, Ca. 93437

Dan Dawson
Director, Product Development
Veda Systems Inc.
California, MD. 20619

ABSTRACT

The US Air Force is required to protect the lives of individuals and property in areas potentially hazardous as a result of launch vehicle failures occurring from Vandenberg AFB, California. This paper describes the application of modern telemetry processing equipment to the Range Safety function.

KEYWORDS

Range Safety, PCM, PAM, FM/FM, Seamless Software Environment, Multiple networked processors, Ada, Veda, Silicon Graphics

INTRODUCTION

In order to assure the safety of personnel and property in surrounding areas, the 30th Space Wing, AFSPACECOM, requires replacement of aging telemetry equipment currently installed at Vandenberg. The new equipment, designated the Range Safety Telemetry System (RSTS), is Commercial-Off-the-Shelf hardware and software with software enhancements to perform Range Safety telemetry processing for various test vehicles flown at Vandenberg and off the west coast over the Pacific ocean. The primary function of the system is the extraction, conversion and output of Telemetered Inertial Guidance (TMIG) data for the Western Range Flight Safety Center (WRFSC). In addition, analog and discrete data is extracted from the input telemetry stream and output for observation on the existing Telemetry Data Display System (TDDS). The RSTS processes telemetry data to determine that acceptable flight safety conditions exist prior to launch and during flight of ballistic missiles and space launch vehicles.

SYSTEM FEATURES

The RSTS, undergoing design development by ITT Federal Services Corporation for delivery in 1994, is composed of two independent Veda Systems telemetry stations, each with redundant Pulse Code Modulation (PCM) stream processing capability which share an Interface Patch Bay assembly. Each telemetry station is configurable to accept up to two PCM streams (or two Pulse Amplitude Modulation (PAM) data streams converted to PCM) and one Frequency Modulation/Frequency Multiplex (FM/FM) input stream and process all of these as one telemetry processing configuration within a telemetry station. Each of the two PCM bit synchronizers in a telemetry station will process bit rates of up to 20 Megabits/second. Embedded or asynchronous data streams can be supported as well as two levels of subframe (subsubframe). Up to 16 input channels of FM analog data is digitized at rates that are individually programmable. A total of 500,000 samples/second can be ingested for engineering unit conversion and archival by each telemetry station.

The RSTS supports engineering unit conversion from 1st through 9th order polynomial conversions, table lookup to 256 point pairs as well as user definable engineering units conversion. The system provides a comprehensive derived measurement calculation capability. Up to 65,000 measurands can be processed by a RSTS telemetry station.

The RSTS provides graphic displays on Silicon Graphics workstations capable of scrolling plots, tabular test data and bar graphs. The displays are capable of simultaneously outputting data in various formats as programmed by the user through the systems' Telemetry Parameter Database.

The RSTS supports the high-speed recording of raw data for either post-test analysis or immediate retrieval. The User may recall display data for a second look at a critical sequence of events. In addition, the User can request subsets of the recorded data for observation, merging with other data, or further analysis and plotting using off-the-shelf software.

Telemetry outputs from each RSTS Telemetry Station consists of data on RS-232C lines to the Metric Data Processing System (MDPS) and the Telemetry Data Display System (TDDS) within the WRFSC.

SYSTEM ARCHITECTURE

The RSTS Telemetry Front-End (TFE) equipment is manufactured by Veda Systems Incorporated which uses three Silicon Graphics Incorporated (SGI) model 4D-V30/35 processors internally mounted on a VME platform in each TFE. The Iris Indigo workstations used with the telemetry stations are also manufactured by SGI. Ethernet is used to interface TFE's to the workstation displays. Figure 1 shows the architecture of a RSTS telemetry station.

Hardware Architecture

Dual Bus Structure

The hardware bus architecture of the ITAS Series-30 consists of a dual bus implementation where the VME bus (primarily the P1 connector) is used for setup and control of all ITAS telemetry modules. The second bus is the ITAS GME bus, or high-speed interface, which provides a dedicated path for real-time data flow between data input modules, such as PCM decommutators and data processing/output modules. This controlled impedance, high-speed data bus is implemented physically on the A and C rows (user definable per VME Rev. C) of the VME P2 connector. The resulting architecture permits host operating system setup and control, and allows data transfers to take place on the VME bus, while high-speed, real-time data transfers are occurring simultaneously on the dedicated GME high speed bus.

GME Bus Bandwidth

The GME bus operates as a broadcast data bus. The bus includes 24 address signals (bits), 32 data signals (bits), and control/reserved signals. The bus is non-multiplexed and can sustain parameter transfer rates of 16,000,000 parameters per second, where each parameter consists of 16 address/tag bits and 32 data bits.

The ITAS Series-30 GME bus architecture accommodates 65,536 uniquely tagged measurements and reserves 16 additional ID tag bits for future expansion (for a total of 32 ID tag bits per parameter). Each GME bus talker, such as a PCM decommutator, MIL-STD-1553 bus monitor, high-speed processor, or parallel input module, has the ability to drive all 16 GME ID tag bits during a bus transfer cycle. There are no arbitrary software prohibitions which preclude any GME bus talker from outputting 65,536 unique measurands. Note that unlike some systems, the separate GME data bus employed in the Series-30 eliminates the time determinism errors common to single VME bus implementations.

Parallel Processor Implementation

The ITAS Series-30's processing architecture implements a course grain parallelism which provides high performance, operating system commonality, and maximum

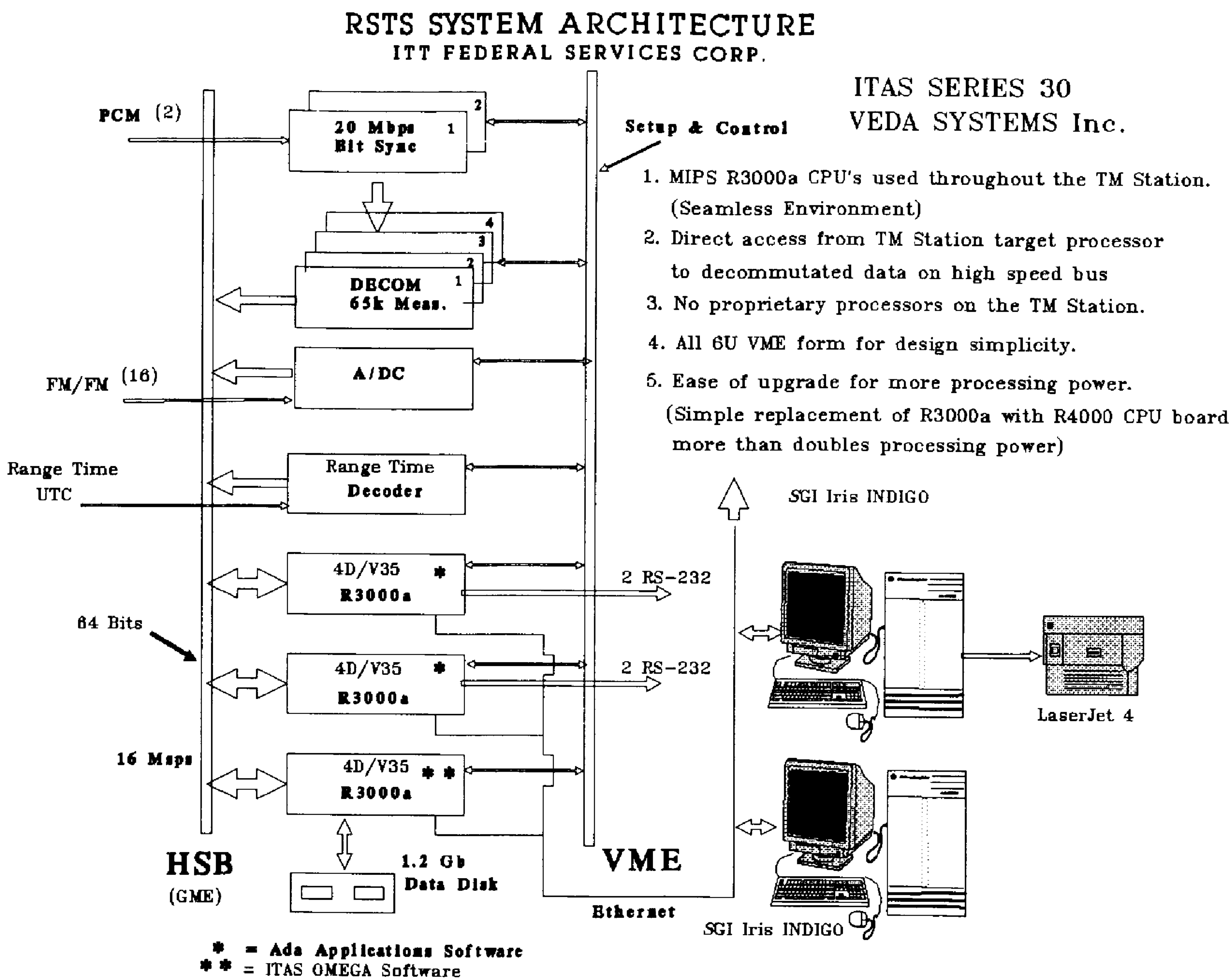
RSTS SYSTEM ARCHITECTURE
ITT FEDERAL SERVICES CORP.
ITAS SERIES 30
VEDA SYSTEMS Inc.
PCM (2)
20 Mbps Bit Sync
1
2
Setup & Control
1. MIPS R3000a CPU's used throughout the TM Station. (Seamless Environment)
2. Direct access from TM Station target processor to decommutated data on high speed bus
3. No proprietary processors on the TM Station.
4. All 6U VME form for design simplicity.
5. Ease of upgrade for more processing power. (Simple replacement of R3000a with R4000 CPU board more than doubles processing power)
DECOM 65k Meas.
1
2
3
4
A/DC
FM/FM (16)
Range Time UTC
Range Time Decoder
SGI Iris INDIGO
4D/V35 * R3000a
2 RS-232
64 Bits
4D/V35 * R3000a
2 RS-232
LaserJet 4
16 Mbps
4D/V35 ** R3000a
HSB (GME)
1.2 Gb Data Disk
VME
Ethernet
SGI Iris INDIGO
* = Ada Applications Software
** = ITAS OMEGA Software

Figure 1.

future growth potential. The Series-30's front-end Silicon Graphics R3000 (36 MIPS) VME processors provide real-time, data-driven processing. To provide superior reliability in adverse environmental conditions and to facilitate compliant operation in secure laboratories, the ITAS Series-30 front-end chassis operates as distress Ethernet nodes, booting from the Silicon Graphics Indigo workstation. When ITAS Series-30 operation is initiated, the front-end CPUs download their real-time operating systems from the workstation. The complete download/booting and self-check process takes less than four minutes.

Operating System Commonality

One of the most powerful features of the ITAS Series-30 architecture is that the front-end SGI CPU(s) execute the same real-time operating system as the SGI-based workstation in a seamless software environment. In fact, application programs can be developed and tested on the workstation and executed on the front-end CPUs with no cross compilation required. As an added feature, the user can create and debug an applications program at the workstation and elect to execute the application program either on a data-driven front-end CPU or at the CVT driven workstation. This mode of application program execution does not affect the front-end' s processing bandwidth and requires the developer to simply compile the application with the appropriate front-end or workstation flag enabled.

While many specifications require very simple front-end user-application processing capability, the power and flexibility of the Series-30' s multiple SGI processor architecture lets users develop extensive algorithms in a variety of languages, such as C, C + +, Fortran, and Ada. The ITAS Series-30 systems procured by the U.S. Air Force at Vandenberg Air Force Base for RSTS implements a full Ada-based range safety application on the front-end units in a real-time, data-driven fashion. The ITAS Series-30's use of common vendor CPUs and operating systems, for both the workstation and front-end processing, allowed software engineers to develop and demonstrate a prototype real-time range safety application in C in less than three days.

Processor Upgrade Path

The open architecture of the Series-30' s embedded processors allow replacement of the existing R3000 Silicon Graphics CPU modules with R4000 modules. This future upgrade would increase the processing performance of the ITAS Series-30 by 50 percent or more and will not require modification to any COTS or user developed software.

Diagnostics

The ITAS Series-30 software suite includes two levels of diagnostic operation. The first level occurs when the system is powered on. As the workstation is booting, the Silicon Graphics workstation initiates a firmware based diagnostic sequence to verify operational hardware. Once these tests complete, UNIX is automatically loaded. The ITAS front-end Silicon Graphics processors conduct the identical tests and also begin to boot via the LAN. If no CPU-based hardware malfunctions are detected, the ITAS Series 30 initiates the front-end telemetry module self-check diagnostic routine.

Shelf Check Diagnostics

The ITAS front-end telemetry module self check begins by consulting the hardware configuration file stored on the workstation. This file contains the hardware configuration of the front-end and the addresses of each of the front-end telemetry modules. One-by-one, the front-end setup and control CPU (P1) accesses each modules' memory and verifies individual modules' presence and memory integrity. Once all modules are present and accounted for, the diagnostic software advances to data throughput verification. The PCM simulator (if installed) can generate a fixed PCM stream which enables the bit synchronization, decommutation and processing to be monitored and verified.

LRU Maintenance Diagnostics

The second level of diagnostics permit trained users to examine individual ITAS telemetry modules (LRUs) for debug purposes. These diagnostics include commands to initiate specialized front-end processor routines which are used to pinpoint malfunctioning LRUs. The same routines are used by ITAS technicians during module repair at the factory.

Software Architecture

Task Dispatcher

The ITAS Series-30 OMEGA setup and control software is a third generation telemetry-specific software environment. The architecture mirrors the UNIX operating system on which it is built. A central task dispatcher module controls the activation of specific task modules based upon the user' s requests. The task modules are small, easily maintained, and provide specific functions to meet various telemetry processing requirements. A wide variety of task modules have been developed. Together, they provide a complete setup, control, display, and command processing environment.

Front-end and Workstation Communication

This real-time, multi-tasking operating system is the key to the system' s power and versatility. The core of the ITAS distributed architecture is network "daemons," or monitor processes, that reside on each front-end CPU and workstation. These processes are responsible for the inter-process communications (IPC) across the LAN. They communicate by transferring Ethernet packets that conform to an OMEGA-specific command and data protocol. The front-end daemon is initially in an idle mode, waiting for requests from the workstation to download a telemetry format, to process and distribute additional parameters, etc. The workstation daemon will monitor the LAN for messages and commands from the front-ends and master workstations, will maintain a list of active front-ends, and will load data into local current value tables for display.

Project Database Organization

The OMEGA Series-30 varies significantly from most telemetry and data acquisition systems in the manner by which a data stream is handled. For example, a typical PCM stream consists of a bit synchronizer and decommutator pair and a set of processors required for the stream In multi-stream systems such as the ITAS, multiple bit synchronizer/decommutator pairs are supported, but the processing and associated measurements reside in a single, format-parameter-list data base. The entire project is treated as a whole rather than as mini-data bases for each processing unit. In the ITAS, each project is made up of streams, parameters, and lists. Projects are created by first executing the project editor and then by adding components to the project with the stream editor, parameter editor, and list editor. Projects are referred to as either global or local projects. The project currently being executed for front end telemetry processing is referred to as the global project. Only one global project at a time can be loaded and executed per front end. Many projects, however, can be simultaneously active in the network as project engineers work with their data for analysis or for preparing for future tests.

List Database Structure

Selection of measurements for archive and display is accomplished by defining a "list" of measurements. The list contains a set of limits for the data values, a title, and a description. A complete, graphically oriented list editor is provided. A list provides an easy way to prepare a defined test. All measurements of interest can be stored into a data base for easy retrieval during run time. All archive and display tasks are list-driven; the list is sorted alphanumerically and can be edited during run time, which adds increased system flexibility.

The use of the list-based architecture, based on layered lists to allow simple access to data elements, is a key design feature of ITAS OMEGA software. The OMEGA accepts multiple data sources from any combination of telemetry, bus, discrete, and analog inputs and time orders all parameters on the system data bus. The full list of all raw, bit, and word-combined engineering units (EU) and derived parameters within the system is called the global list. From this, data groups may then be formed. For example, a structural engineer, test director, or safety officer can develop separate data lists that only contain the parameters in which they are interested for any given test scenario. These lists may include some of the same parameters. This effectively provides these individuals with separate telemetry systems. Combined data can be archived at the same time and to the same device, since they may be merged, or separation may be maintained for data security.

This innovative list-based architecture has an additional advantage in that in some projects, the global list may become extremely large. Engineers may find it difficult to locate the parameter that they require from 6,000 or more different entries contained in a single flat file. The use of lists allows each project and user to limit the parameters in the lists defined to only those that are required. This list-based technique can also be used to limit bandwidth to selected devices by creating sublists for specific archive, processing, and display duties and by manipulating the list as a unit.

STANDARDS USED

The RSTS is being developed using a UNIX environment with an open systems architecture allowing for the integration of off-the-shelf VME modules and external devices if the need arises. The system utilizes an Ethernet interface compatible with commercially available workstations and X-terminals that support TCP/IP protocols. The RSTS is being developed under MIL-STD-2167A for applications software documentation and Ada (MIL-STD-1815A) for the new missile specific software. The telemetry formats of IRIG-106, revised 92, can be supported by the RSTS.

APPLICATIONS

The RSTS real-time range safety applications being developed as enhancements to the Veda Telemetry System (ITAS) are for support of active ballistic missile and space programs such as TITAN, Peacekeeper, Minuteman, Pegasus, Taurus, Delta, Scout and Atlas. The added software will extract the required inertial navigation parameters from the telemetry stream, perform the necessary coordinate transformations and output data to the WRFSC 20 times per second. In addition, various missile specific analog, discrete and missile event data is processed for output on real-time displays within the WRFSC. Two of the three front-end CPUs will be allocated for processing of both TMIG and TDDS data in parallel providing redundancy of output. The third CPU operates the standard telemetry control, archive and display features of the ITAS Series 30 telemetry system.

CONCLUSION

The modern architecture of the ITAS allows significant processing to occur in the telemetry front-end using standard vendor software and minimizes the need for tailoring of software for each missile type. The RSTS will provide the U. S. Air Force Western Range with a modern range safety processing capability. The system provides a state-of-the-art architecture based on industry standards assuring upward growth in processing power as well as in quantity of resources. Future airborne systems arriving at Vandenberg AFB for testing should be easily accommodated using the modern standards based architecture provided by the RSTS.