EOS HIGH RATE TELEMETRY PROCESSING COMPONENTS

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ABSTRACT

The unprecedented volume of earth science data generated by NASA's Earth Observing System (EOS) will require significant advancements in the capability and scale of ground-based data acquisition and processing systems. In order to meet this challenge, NASA's Goddard Space Flight Center (GSFC) has initiated the development of key subsystem components for CCSDS front-end processing at 150 Mbps data rates. This effort is a continuation of the Functional Components Approach (1), an approach applied over the last eight years that uses modular, VMEbus subsystems based on Very Large Scale Integration (VLSI) technology to create pipelined, multi-processor telemetry data systems. The result of this development effort is the creation of four new functional component subsystems incorporating four new VLSI Application Specific Integrated Circuits (ASICs) and the augmentation of two existing subsystems to include elements for frame synchronization, Reed-Solomon error correction, CCSDS Service processing, and simulation at EOS data rates. This paper describes this development effort and provides initial functional and performance expectations .

INTRODUCTION

The Earth Observing System (EOS) is a NASA science research mission commissioned to provide a comprehensive understanding of global environmental change. The goal of the EOS is to systematically measure and study global change over at least a fifteen year period through remote observations from space. In order to obtain broad coverage of the numerous processes that affect the Earth's environment, eighteen spacecraft incorporating different onboard configurations of remote-sensing instruments are planned to fly over the life of the mission.

Each EOS spacecraft will incorporate a number of high resolution instruments which will be capable of generating enormous volumes of science data. Science data from

each instrument will be packetized, multiplexed, and telemetered at very high rates using standard protocols based on the CCSDS recommendations. Starting with the launch of the first spacecraft in 1998, EOS will transmit in excess of one Terabit (1012) of earth science data per day. Many of the EOS spacecraft will down link data at peak rates up to 150 Mbps. In order to accommodate this volume of high rate packetized data, EOS ground data acquisition and processing systems will require performance and functionality far beyond those commonly implemented today .

For the past eight years, the Data Systems Technology Division (DSTD) at Goddard Space Flight Center (GSFC) has developed high performance data acquisition and processing systems for a number of present and future NASA programs including Small Explorer (SMEX) (2), Deep Space Network (DSN), Hubble Space Telescope (HST) (3), Topographical Explorer (TOPEX) (4), and Space Station Freedom. These data systems have been implemented from a common set of low-cost hardware and software "building blocks", known as functional components. This *functional components approach* provides a technique to quickly and inexpensively build or configure data systems to meet changing mission requirements. Key characteristics of this approach include the use of open-bus system platforms, pipelined multiprocessing, and VLSI technology to lower component costs and increase system performance.

An effort is currently underway in the DSTD to create a new set of functional components for data systems meeting EOS performance requirements. These new low-cost subsystems include elements for frame synchronization, Reed-Solomon error correction, CCSDS services processing, and spacecraft data simulation at sustained data rates of up to 150 Mbps. The development of these CCSDS front-end processing subsystems is the subject of this paper. First, the objectives and approach of this effort are presented. Each of the six functional component subsystems under development are then described in detail.

EOS HIGH RATE COMPONENTS

The EOS High Rate Components development effort was initiated in 1992 to extend the functional components approach to EOS-era front-end processing systems. This effort is divided into three concurrent development activities, each of which demonstrates a different level of capability in front-end processing. The system block diagram in **Figure 1** illustrates these three capability objectives and their constituent subsystem elements. The shaded elements make up this development effort. The unshaded elements represent either existing subsystems or those that are being developed under a separate program for 150 Mbps Level Zero Processing (LZP).

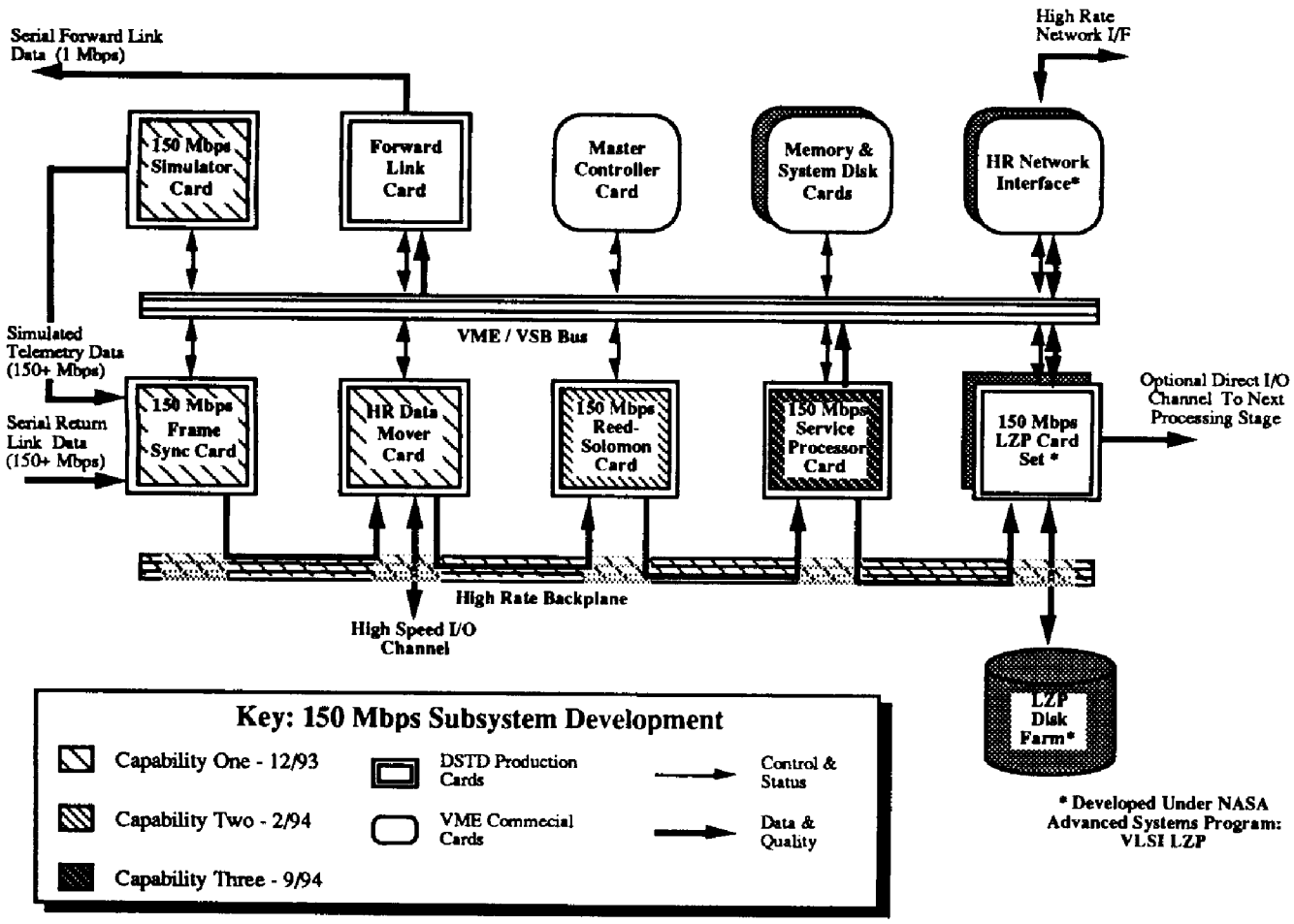

Figure 1 - EOS High Rates Component Development

Frame Acquisition and Simulation

The first demonstrated capability, scheduled for completion in December of 1993, targets functionality for system-level data handling, frame acquisition, and data stream simulation. Three VMEbus subsystems and a new telemetry bus for high rate data transfer are the result of this development. The new telemetry bus, known as the High Rate Telemetry Backplane, is a next generation version of the telemetry pipeline bus used in current functional component systems. Designed to handle up to 20 simultaneous data transfers, each at rates up to 300 Mbps; this bus is essential to the development of very high performance functional component systems because it provides for the concurrent transfer of high rate data between data processing elements.

The 150 Mbps Frame Synchronizer card (5) provides telemetry frame acquisition using a programmable acquisition strategy. Serial telemetry data input is correlated, synchronized, converted to parallel, and quality annotated before being output to the

High Rate Telemetry Backplane. This card is actually a minor augmentation of an existing subsystem (5) adding an interface to the new High Rate Telemetry Backplane.

The High Rate Data Mover card is also a minor revision of an existing subsystem to provide interfaces to the new telemetry bus. This card serves as a data transfer bridge between the three system busses and up to two external interfaces. External interfaces are defined by daughter card modules that plug into the motherboard. Both small computer systems interface (SCSI) and high speed interface (HSI) interfaces are currently supported, however, new interfaces can be readily created.

The 150 Mbps Simulator card is a new card designed to simulate realistic spacecraft data streams for ground system testing. The card combines a large amount of on-board memory (up to 128 Megabytes) and two different memory controllers that allow the simultaneous update and output of test pattern memory data. Update values are either stored on card, generated by the card's processor, or input through a daughter card interface compatible with High Rate Data Mover card. The output is controlled by a single chip Gallium Arsenide (GaAs) memory controller that was created specifically for this application. The GaAs Test Pattern Generator chip, developed using a 0.8 micron GaAs gate array, facilitates the formatting and output of high rate parallel and serial data streams. The Simulator card also contains on-board hardware for CCSDS Reed-Solomon, Cyclic Redundancy Check (CRC), and bit-transition density encoding.

Reed-Solomon Error Correcting and Virtual Channel Sorting

The second capability objective provides Reed-Solomon error correction and virtual channel sorting functionality by February of 1994. This functionality is accomplished through the development of a single VMEbus card subsystem. The 150 Mbps Reed-Solomon card performs both header and block error correction and can support mixed streams of CCSDS data requiring different grades of services. Data is input through the High Rate Telemetry Backplane interface and is deinterleaved prior to Reed-Solomon decoding. After correction, the card filters and sorts frames by Spacecraft and Virtual Channel ID. Corrected frames are routed for output to one of four channels on the telemetry bus.

Most of the functions on the 150 Mbps Reed-Solomon card are performed by a single VLSI ASIC component. The Reed-Solomon Error Correction chip, developed as part of this effort, is an 80K gate 0.6 micron semi-custom CMOS device (6). This component incorporates two Reed-Solomon decoders and a host of memory controllers that support the automatic input, deinterleaving, and correction of data. Quality annotation, cumulative quality accounting, and header look-up for routing are

also supported on-chip. A block diagram of the Reed-Solomon Error Correction chip is provided in **Figure 2**.

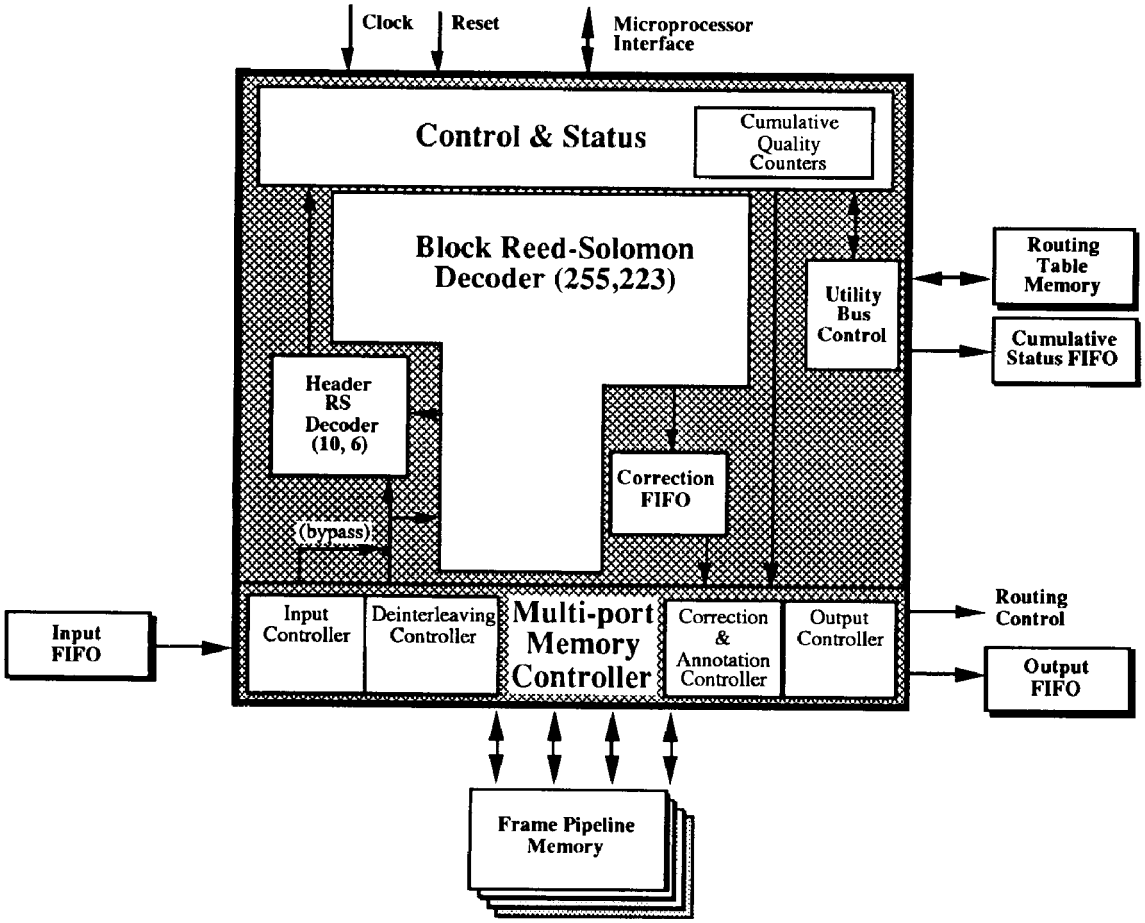

Figure 2 - Reed-Solomon Error Correction Chip Block Diagram

CCSDS Services Processing

The 150 Mbps Service Processor subsystem is being developed to meet the third capability objective. This single VMEbus card subsystem, scheduled for completion in October of 1994, performs the frame and packet data extraction services defined by the CCSDS conventional and Advanced Orbiting System (AOS) standards. Input frame headers and quality are first verified to determine frame status and required service. Data is then grouped by frame identifiers and reassembled prior to output. On output, reassembled packets are sorted by their packet identifiers and annotated with the results of quality checks performed on the data.

A key driver in this development is EOS's planned use of relatively small packets at high data rates. EOS spacecraft are expected to downlink data with worst case packet rates beyond 50,000 packets per second. The inclusion of lossless data compression on future EOS spacecraft could push these rates to 150,000 packets per second. Because

each packet requires a similar amount of protocol processing, increased packet rates have a much more dramatic impact on ground system development than increased data rates (7).

The 150 Mbps Service Processor subsystem design is based on an existing subsystem designed for data rates of 20 Mbps and packet rates of up to 5000 packets per second (8). The new Service Processor incorporates two new VLSI ASIC components that upgrade the current architecture to meet EOS data and packet rates. One of these, the MC680x0 Support chip, is targeted toward increasing real-time software processing performance. The original card design incorporates three loosely-coupled CPUs based on the Motorola 68020 microprocessor. These CPUs exist on the subsystem mother board as daughter card modules. These original CPU mezzanines, measuring about 3" by 3", owe their small size to an ASIC component that integrates all the interface and "glue" logic required for the CPU implementation. For the 150 Mbps Service Processor, a new version of this interface ASIC has been developed to support CPU modules using the state-of-the-art Motorola 68040 miroprocessor. This MC680X0 Support chip has enabled the development of a new generation of CPU mezzanines that increase processing performance to over four times the original with only a slightly larger footprint (3.4" x 3.7"). A physical diagram of this CPU module, referred to as the 68040 CPU Mezzanine, is shown in **Figure 3**. Since its development, the 68040 CPU Mezzanine has been incorporated into the current architecture to create a CCSDS services processing subsystem that meets performance levels of 50 Mbps and 20,000 packets per second.

The second VLSI component being developed for the 150 Mbps Service Processor is a 0.6 micron CMOS support chip targeted to off-load common CCSDS processing functions into hardware. This Service Processor Support chip replaces two ASIC memory controllers used in the original design to automate header extraction, frame sorting, error correcting, and packet reassembly. The Service Processor Support chip integrates and further automates these functions to decrease the subsystem's real-time software workload and, thereby, increase subsystem performance. In header extraction, for example, two new features decrease the software processing load. One is automatic packet header extraction that off-loads next packet location calculation and length checking into hardware. The second is a flexible header look-up controller that is used to automate frame and packet header verification and sequence checking. Additional areas targeted for hardware automation include quality annotation and cumulative quality accounting.

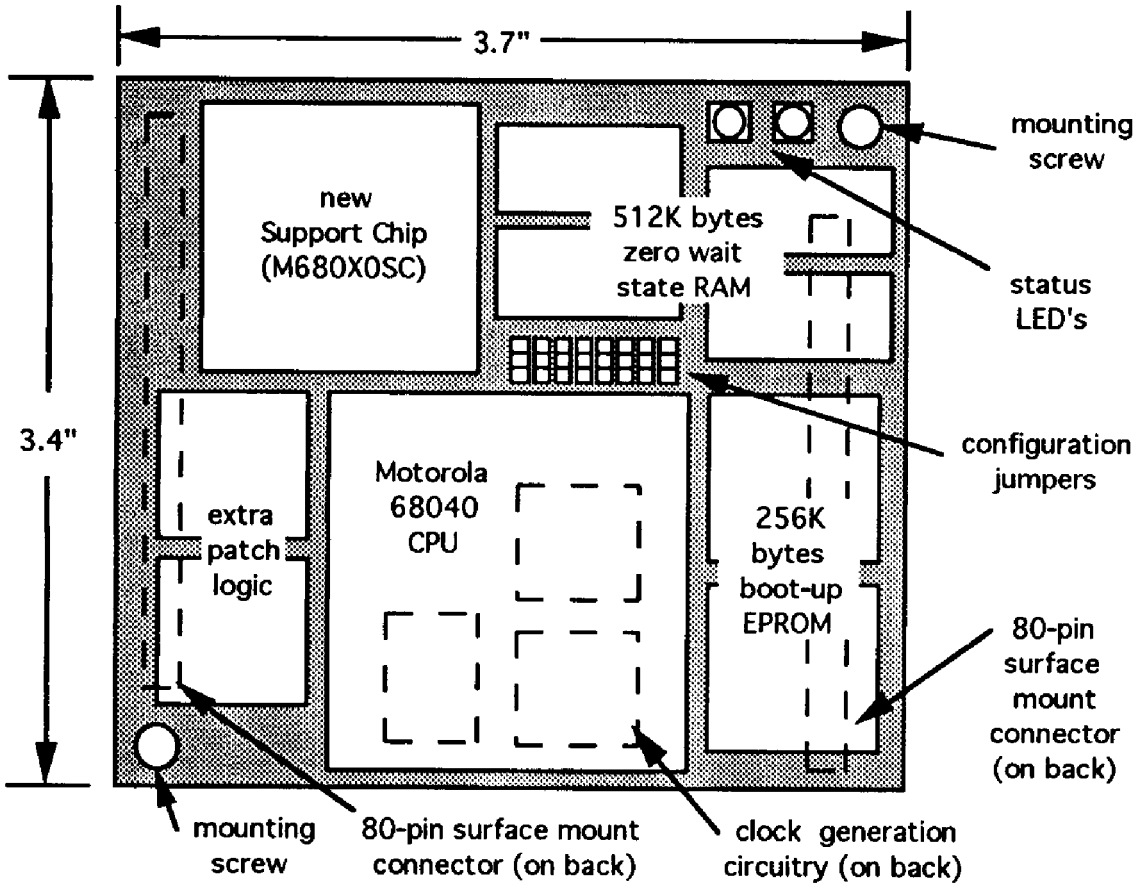

Figure 3 - 68040 CPU Mezzanine Card Physical Diagram

CONCLUSION

NASA's Earth Observing System will play a major role in defining high performance space telemetry processing requirements beyond the 21st century. The design, development, and availability of effective solutions which meet these requirements will determine the real success NASA will have in the fulfilling the mission of the EOS program. CCSDS based ground telemetry data systems which meet EOS requirements must also provide a flexible, cost effective solution which is accessible to the vast numbers of scientist preparing for the EOS era. These scientist will make the next great breakthroughs in understanding our global environment and man's effect on it.

Recent success at Goddard Space Flight Center in the design and development of 20 Mbps ground telemetry systems and system elements, has prompted an effort to evolve these system elements to much higher functional and performance levels. This effort has resulted in a number of key silicon level (ASICs) and board level engineering innovations and designs which promise to provide the solutions needed by

the EOS programs. With potential solutions to such fundamental EOS problems in ground telemetry processing as Frame Acquisition, Reed-Solomon decoding, and CCSDS Service Processing, NASA can expect to meet its EOS mission goals.

NOMENCLATURE

ASIC	Application Specific Integrated Circuit
CCSDS	Consultative Committee for Space Data Systems
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DSTD	Data Systems Technology Division
DSN	Deep Space Network
EOS	Earth Observing System
EDOS	EOS Data Operations System
FIFO	First-In First-Out
GaAs	Gallium Arsenide
GSFC	Goddard Space Flight Center
HSI	High Speed Interface
HST	Hubble Space Telescope
Mbps	Megabits per second
NASA	National Aeronautics and Space Administration
SCSI	Small Computer System Interface
SMEX	Small Explorer
TOPEX	Topographical Explorer
VCDU	Virtual Channel Data Unit
VLSI	Very Large Scale Integration
VME	Versabus Module Eurocard

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