Replacement of the Hubble Space Telescope (HST) Telemetry Front-End Using Very-Large-Scale Integration (VLSI)-Based Components

Charles Scaffidi  
Mission Operations Division

Richard Stafford  
Loral AeroSys

Mission Operations and Data Systems Directorate  
NASA, Goddard Space Flight Center  
Greenbelt, MD 20771

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ABSTRACT

The Hubble Space Telescope (HST) Observatory Management System (HSTOMS), located at the Goddard Space Flight Center (GSFC), provides telemetry, command, analysis and mission planning functions in support of the HST spacecraft. The Telemetry and Command System (TAC) is an aging system that performs National Aeronautics and Space Administration (NASA) Communications (Nascom) block and telemetry processing functions. Future maintainability is of concern because of the criticality of this system element. HSTOMS has embarked on replacing the TAC by using functional elements developed by the Microelectronics Systems Branch of the GSFC. This project, known as the Transportable TAC (TTAC) because of its inherent flexibility, is addressing challenges that have resulted from applying recent technological advances into an existing operational environment.

Besides presenting a brief overview of the original TAC and the new TTAC, this paper also describes the challenges faced and the approach to overcoming them.
INTRODUCTION

The Hubble Space Telescope (HST) Observatory Management System (HSTOMS), located at the Goddard Space Flight Center (GSFC), provides telemetry, command, analysis, and mission planning functions in support of the HST spacecraft. HSTOMS is a large, complex system that is comprised of numerous hardware and software subsystems. Originally developed in the early 1980s, HSTOMS has supported the HST spacecraft since its launch in April 1990. From its inception, HSTOMS has progressed through numerous evolutionary changes and upgrades, reflecting changes to mission requirements, the needs of the flight operations team (FOT), and technological advancements.

The Telemetry and Command System (TAC) was originally developed in the late 1970s for other GSFC programs and was later adapted for use by the HST Mission Operations Center (MOC). In general, the TAC's design is typical of other systems developed in that timeframe. The TAC consists of a set of custom hardware/firmware and a PDP-11 processor. The custom logic consists mostly of transistor transistor logic (TTL) small-scale integration (SSI)/ medium-scale integration (MSI) logic with some large-scale integration (LSI) components. The circuit cards plug into custom backplanes that interface to the PDP-11 via the PDP's UNIBUS. In total, the TAC is contained in three standard 19-inch equipment cabinets. The components used in the custom hardware (and the PDP-11) are aging, and maintainability is an issue. In addition, the PDP's resources are saturated.

Recently, a study was performed to identify the requirements for a replacement TAC and to evaluate various implementation approaches. Eight options were evaluated and included several new custom designs and several software-based solutions based on commercial-off-the-shelf (COTS) or modified COTS hardware.

The selected option was a design based on the available functional components developed by the Microelectronics Systems Branch, Code 521, at GSFC. This approach, referred to as the functional components approach, has been extensively documented since the late 1980s (Reference 1). The main advantages provided by the functional component approach are that existing components already provide most major hardware functions and that the open architecture provides flexibility. These factors lead to a highly cost effective solution.

Despite these benefits, the application of the functional component approach came with its own set of challenges. These challenges have included the following:
Identifying the "hard" requirements (design characteristics of the original system tend to be considered as hard requirements)

Integrating the multiple groups, responsible for parts of the design, into a cohesive team

Keeping pace with a constantly evolving environment

Integrating the replacement system into an operational environment that is online 24 hours a day

This paper discusses these challenges and how they have been addressed.

**TAC FUNCTIONAL OVERVIEW**

The TAC provides the interface to the NASA Communications (Nascom) network and the HSTOMS. It provides six bidirectional interfaces for telemetry receipt, command transmission, and general receipt and transmission of data formatted in the Nascom "standard" block format. The major functions of the TAC are as follows: (1) network interface, (2) protocol processing, (3) data extraction and staging, and (4) data routing.

The first two of these functions are generally provided by the custom hardware while the latter two are performed in software on the PDP-11. The network interfaces are divided into A channels and B channels as shown in Figure 1.

The A channel provides full telemetry processing functions while the B channels provide more robust block processing capabilities but no telemetry processing. The system utilizes hard disk storage for staging data for later routing. Dual Ethernet interfaces transport telemetry, spacecraft commands, and configuration/status data to other HSTOMS elements. Control and status reporting is provided by either a local terminal or from a remote host via the Ethernet local area network (LAN).

**TTAC FUNCTIONAL OVERVIEW**

Although primarily applied to packet telemetry applications (Reference 2), the very-large-scale integration (VLSI)-based functional components developed by the GSFC Microelectronics Systems Branch provide all the basic functions required by a more classic time division multiplex (TDM) system. These basic functions include: (1) synchronizing the serial data stream with the telemetry frames; (2) checking, correcting, and accounting for errors; (3) storing and processing the captured frames; and (4) providing interfaces for the delivery of the resulting data. In addition, the
functional components approach allows for an integrated command system that receives, processes, formats and transmits command data to the spacecraft.

**Figure 1. Current TAC System**

The TTAC, implemented with this VLSI-based technology, provides a relatively open system based on the Versa Module Eurocard (VME) bus. Figure 2 presents a block diagram of the prototype TTAC configuration.

Processing is distributed across the VME bus with multiple processors running concurrently. Commercial processors and support cards (i.e., network interfaces, disk controllers, memory) are utilized extensively. The architecture also incorporates a high performance, custom pipeline bus. This bus is available to transfer high-rate data between system elements without loading the VME bus.

Custom functions, such as the frame synchronizer, are implemented by using a combination of commercial and custom designs in a 9U VME form factor. A 3U commercial processor, which resides on the VME bus, is connected to a custom 6U assembly. The custom cards used in the TTAC include the following:

- Synchronizer card—Provides Nascom block processing and frame synchronization functions
Figure 2. TTAC Configuration

- Multiplexer card—Provides a bridge between the VME bus and the custom pipeline bus; provides a serial interface capable of outputting Nascom type blocks of variable length

- Nascom interface card—Provides two bidirectional serial interfaces capable of transmitting and receiving standard length Nascom blocks

- Simulator Card—Generates simulated data to test the TTAC

The TTAC software is primarily implemented in 'C' under a real-time operating system. There are two layers of custom system software layered on top of the operating system. The first layer is the Base System Environment (BaSE) that provides a generic, consistent environment for integrating commercial and custom processing cards into the system. BaSE provides tools for multiprocessing and allows the target system to also act as the development system. The second level of system software, the Modular Environment for Data Systems (MEDS), supplies a basic shell on which the applications are built. MEDS supports intertask and intercard message passing and communications over Ethernet via Transmission Control Protocol/Internet
Protocol (TCP/IP). MEDS also boots the system, automatically identifies the installed cards, supports system configuration, control, and status reporting on the custom cards, and provides both a local and a remote operator interface. Applications programs reside on top of the MEDS software and are isolated somewhat from the operating system and from the hardware (interrupts, configuration registers, etc.). In the distributed environment, each processor executes its own image of the operating system, BaSE, and MEDS.

Although the existing functional components implement most of the capabilities required for the HST TAC, several new hardware and system-level software functions were added. Changes to both the hardware and system software were performed by the Microelectronics Systems Branch. It should be noted that these functions were incorporated as revisions to the existing hardware and software components and will thus be available to other users. Backwards compatibility with previous revisions is also maintained.

The major items added to the synchronizer card included pseudonoise decoding and byte-to-bit conversion. These changes were incorporated into the custom VLSI gate arrays contained on the synchronizer card. The multiplexer card was modified to provide the capability to format Nascom data blocks with variable, nonstandard data lengths.

The system software elements were also modified to reflect the hardware changes and to add new functionality. This new functionality included the capability to reconfigure individual channel elements and to open multiple data buffers on disk. These software modifications were required because of HST operational procedures. Previous implementations using the GSFC functional components were normally configured before a satellite pass and were left in that configuration throughout the pass. The HST, on the other hand, will normally reconfigure multiple times during a pass.

At the applications level, HST-specific software will be written and integrated by the HSTOMS contractor. This software will control the HST-specific system configurations, will provide higher level processing functions, and will provide a command and control interface that is compatible with other elements within the HSTOMS. Some of the HST-specific processing functions include the following: (1) repackaging data for distribution, (2) extracting specific data types from the full telemetry stream, (3) staging high-rate data for later playback, and (4) playback at variable rates.
IMPLEMENTATION CHALLENGES

In many ways, implementing the TTAC by using VLSI functional components did not present a technical challenge. Most of the hardware designs existed, and the rated performance of these components far exceeded the TTAC data rate requirements. The real challenges were in the application of an established, albeit flexible, technology, rather than that technology itself. This section will discuss the challenges and how they are being addressed.

REQUIREMENTS DEFINITION

The TAC functional and performance requirements, along with other elements of the HSTOMS, were documented at the time of development and have had periodic, minor updates. Because the existing TAC design has been in operation for many years, many design-level attributes and operational characteristics essentially became requirements on the TTAC development. Where they were not major cost drivers, these characteristics were incorporated into the TTAC. However, some requirements, such as hardwired, discrete status indicators, did have cost and schedule implications as they were not easily incorporated into the existing designs. These requirements were challenged as to their validity and against available alternatives. In the cited example, it has been proposed that the hardwired displays be replaced by periodic status messages that are available over the Ethernet interface. Thus, the status can be made available over workstation-based displays.

MULTIPLE DEVELOPMENT GROUPS

The TTAC design is being based on a common set of functional and performance requirements. The design's infrastructure is the GSFC-developed functional components and associated software. The GSFC Microelectronics Systems Branch is responsible to the GSFC HSTOMS manager to provide these elements, modified to the TTAC requirements. Software development and system integration are the responsibility of the HSTOMS support contractor.

Two steps were taken to ensure that the GSFC Microelectronics System Branch and the HSTOMS support contractor worked together as a unified team. First, regular working group meetings were established for technical interchange. Formal action items were maintained to track open issues. Second, the schedule was based on early hardware builds. Because of the similarities between the existing available hardware, the first hardware delivery consisted of a multichannel system, minus the HST unique modifications. This system allowed the software developers and systems engineers to
become familiar with the TTAC hardware and software development environment early in the design phase. This early exposure allowed feedback into the hardware design cycle. Later deliveries will incorporate hardware and software changes and will allow additional input to the final design.

Evolving Environment

As mentioned above, the HSTOMS is a constantly evolving system. A major upgrade of the HSTOMS, known as the Payload Operations Control Center (POCC) Operations Real-Time Support (PORTS) Replacement System (PRS), is in progress, and there are many other, ongoing, smaller initiatives. This changing environment requires that the TTAC development team consider both the existing and future operational environments. However, the opportunity also exists to positively affect the configuration of these other systems.

One area of change is in the network configuration. The PRS is introducing more distributed processing on workstation-class machines. Engineering telemetry will be multicast via Ethernet. Individual workstations will then ingest only the data required to perform their assigned function.

Currently, the HSTOMS networks are based on the DECnet protocol because the functional component approach is based on TCP/IP. To solve this problem, a second-source TCP/IP package, Multinet, will be installed on the virtual address extension (VAX) hosts within HSTOMS. The compatibility and performance of Multinet with the TTAC was tested in the Microelectronic Systems Branch development laboratories before selection. In this approach, alternatives to the original PRS design had to be considered. Using TCP/IP will provide compatibility with other institutional facilities that are primarily UNIX based. Thus, the TTAC presented an opportunity to begin phasing TCP/IP into the HSTOMS.

At the time of writing, the inclusion of a dual ring Fiber Distributed Data Interface (FDDI) interface instead of the dual rail Ethernet is being considered. The current TAC cannot support the FDDI interface while the systems based on the functional component approach are already incorporating FDDI interfaces. The bandwidth provided by FDDI will allow more capability in terms of concurrent operations, that is, satellite support, test, and maintenance and may facilitate interoperability with the HSTOMS development facility. Network reliability should also be improved.
INTEGRATION

The HSTOMS provides 24-hour-per-day support of the HST spacecraft as well as a busy schedule of tests and simulations. Thus, the integration of a new system must be performed without impact to those operations. The HSTOMS has a history of prototyping new equipment, testing the equipment in parallel with operations, and slowly phasing out the old equipment. The old equipment is typically retained for a period of time as a fallback.

Because they are involved in all phases of operations, including the basic data capture, the TACs are considered especially critical. The technical risk associated with the TTAC development is considered to be greater than that of the average project of a similar size within the HSTOMS. The technical risks include the use of custom hardware elements and the use of distributed microcomputers.

Several approaches are being used to mitigate these risks. The first method is the phased development approach already described. Early hardware deliveries have built confidence in this development approach. These deliveries will be integrated into the HSTOMS development facility. Development and test activities can then proceed without impact to ongoing HST operations. Current plans include running the early TTAC in parallel with real-time operations in a test mode.

Phased parallel operations with the current TACs will also be used to minimize the risk in integration. Once proven in the development environment, including thorough independent testing, the first TTAC will be phased into the operational facility. Here, too, the TTAC will be operated in parallel with the current systems. Once a full complement of TTACs are in place, the older system will be taken out of service.

CONCLUSION

The VLSI-based functional components developed by GSFC provide a high-performance, effective approach to solving unique telemetry processing problems. These components are relatively mature and can be adapted to new applications relatively easily. However, using these components still presents challenges to the implementer. These challenges can be overcome through careful requirements analysis, close interaction between development organizations, coordination with other ongoing development activities, the use of early hardware builds, and a phased integration strategy.
REFERENCES


NOMENCLATURE

BaSE Base System Environment
CPU central processing unit
DEC Digital Equipment Corporation
DECnet DEC network
FDDI Fiber Distributed Data Interface
FOT night operations team
GSFC Goddard Space Flight Center
HSTOMS HST Observatory Management System
HST Hubble Space Telescope
LAN local area network
LSI large-scale integration
MEDS Modular Environment for Data Systems
MOC Mission Operations Center
MSI medium-scale integration
NASA National Aeronautics and Space Administration
Nascom NASA Communications
POCC Payload Operations Control Center
PORTS POCC Operations Real-Time Support
PRS PORTS Replacement System
SSI small-scale integration
TAC Telemetry and Command System
TCP/IP Transmission Control Protocol/Internet Protocol
TDM time division multiplex
TTAC Transportable TAC
TTL transistor transistor logic
VAX virtual address extension
VLSI very-large-scale integration
VME Versa Module Eurocard