SOLID STATE DATA RECORDER (SSDR)

FOR

AIRBORNE/SPACE ENVIRONMENT

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ABSTRACT

VME bus has been widely accepted as an industry standard for control and process computers. The MSTI (Miniature Sensor Technology Integration) series of satellites employ a VME bus based data acquisition and control system. This system requires a ruggedized, high-speed, compact, low power and light weight data recorder for storing digital imagery from payload video cameras, as well as health and status data of the satellite. No commercial off the shelf systems were found which meet MSTI specifications. Also, a solid state device eliminates certain reliability and spacecraft pointing control problems which are encountered when using rotating (disk or tape) storage systems. The SSDR was designed to meet these requirements and it also has built-in flexibility for many general purpose applications. The electronic hardware design, which conforms to the VME bus specifications [1], can also be configured as stand-alone system. Modular memory array design allows expandability of capacity up to 320 MBytes.

This paper will describe the design features of the SSDR. Performance capabilities and system implementation will be discussed. Special approaches required for application of the SSDR in space or harsh environments are also discussed.

KEY WORDS

Recorder, Solid State, Memory, Versabus Moduli Europa (VME)

SYSTEM ARCHITECTURE

The block diagram of the SSDR is shown in Figure 1. The SSDR consists of a motherboard and a set of memory array boards. The motherboard includes VME bus interface module, Error Detection And Correction (EDAC) module and also an independent interface for receiving the external data. The SSDR is in full conformance of the VME bus specification. Each of the memory array boards includes 32 Mbytes of SRAM arrays for data and 12 Mbytes for check codes.

EDAC

The EDAC accepts a 32 bit word and generates a 12-bit check code (two 6-bit check codes, one for each higher and lower 16-bit segments of the data word). The 32-bit data word and 12-bit check code are both written to SRAM arrays. When the data word along with check code is read back, a new check code is generated and compared with the received check code. If these codes match, no error has been detected. If a single bit error has been detected for each 16-bit segment of the data word, it will be corrected before being communicated to the VME bus. If a multiple bit error is detected it cannot be corrected and an error signal will be generated and communicated to the VME bus.

VME BUS INTERFACE CIRCUIT

The VME bus interface circuit and the control logic are implemented using a radiation tolerant field programmable gate array (FPGA) and buffers. The buffered data and address conform to the requirements of the VME bus specification.

During a write, the 32-bit data words from the VME bus or external interface are buffered and sent to the EDAC. During a read operation the 32-bit data pass through EDAC and then get stored into registers. The data can be then selectively read in 32-bit, 16-bit or 8-bit formats over the VME bus. Also, all possible data transfer operations per VME bus specifications are supported.

The VME CPU (Central Processor Unit) can address or select and control each of the memory array boards. This is achieved by decoding the assigned address of each memory array board. The operating power requirement is significantly reduced by power management controls in which SRAM arrays are partitioned in to banks and the only bank which is to be written or read is switched to operating mode while the remaining banks go in to standby mode.

APPLICATIONS

The SSDR is designed using radiation tolerant components, however, it can also accommodate the radiation hardened parts. The radiation tolerant devices are inherently latch-up free and are cost effective compared to fully radiation hardened parts. The SSDR bare circuit cards can be populated with commercial components to achieve a low cost system for commercial applications. Up to ten memory array boards can be employed as required. This provides an excellent flexibility for sizing the SSDR. Also, the identical design of memory array cards provides the interchangeability. The SSDR can store external data autonomously through external interface. The solid state design eliminates any problems related to pointing accuracy and inertial balancing which are present in the rotating memory systems. The SSDR requires less power and it is lighter in weight compared to a rotating memory system. Also, the SSDR can tolerate tougher vibrations and shocks than the rotating storage devices. The SSDR is not required to be housed in a separate sealed box. Battery backed SRAM arrays provide non-volatile memory .

FUTURE DEVELOPMENT

Continued advancement in research and development of faster, higher density and high reliability SRAMs will allow designing of larger capacity memory array boards. This will further enhance the space, power and weight requirements. Development of higher density, faster EEPROMS (Electrically Erasable Programmable Read Only Memory) and flash memory in future could replace the battery backed SRAMs to provide non-volatile SSDR.

CONCLUSION

The SSDR has eliminated the mechanical problems and mitigated the environmental problems that are found in the rotating memory systems like tape drives and hard disks for application in the space environment of MSTI satellite. The design of SSDR meets the requirements of a radiation tolerant data recorder for spaceborne applications for a reduced cost, less space and less power. The VME bus based design of SSDR provides built-in flexibility for use in any general purpose commercial as well as military applications. There is possibility of enhancement in the design of SSDR with continued improvement in the components utilized for SSDR.

REFERENCES

[1] The VMEbus Specification, ANSI/IEEE STD 1014-1987.

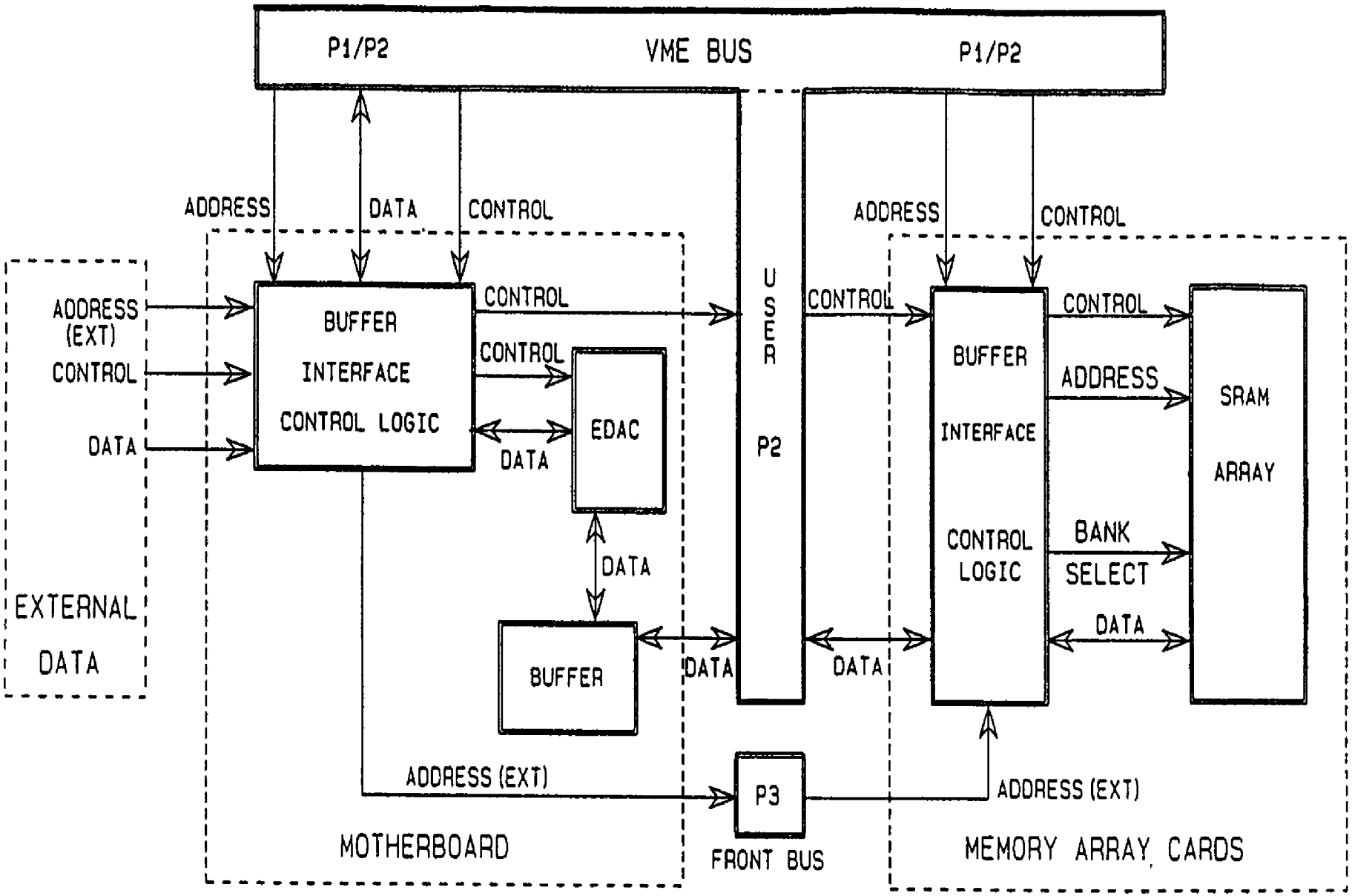

FIGURE-1. SSDR BLOCK DIAGRAM