

A BRIEF LOOK AT DELTA MODULATION

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ABSTRACT

The principle behind delta modulation systems is introduced. Having developed the principles of delta modulation systems, a system that performs delta modulation is developed and tested to see how well the system performs by using sinusoids and speech as the input to the system. This is then followed by a comparison of delta modulation and pulse code modulation to show that, overall, delta modulation is better than pulse code modulation.

INTRODUCTION

In this report, the concept of delta modulation will be discussed. The design and implementation of a delta modulation system will be discussed along with the results of the implementation of such a system. Put simply, delta modulation achieves the digital transmission of baseband signals (voice) without the use of conventional analog to digital and digital to analog systems found in pulse code modulation which require a high degree of sophistication where hardware is concerned. Results will be based on the systems performance when test signals of different frequencies are used as the input and ultimately, when a voice signal is used as the input.

DELTA MODULATION

Figure 1 shows a signal to be transmitted along a communication channel via a digital signal. Conventional methods such as pulse code modulation thus far have proven to be expensive and cumbersome. These drawbacks have led some engineers toward a method of digitally transmitting a signal of interest without the drawbacks of conventional systems.

By oversampling the signal of figure 1 and comparing it to a signal that is a close approximation to it, an output pulse train can be generated that contains information concerning the rate of change of the input signal and its amplitude. For example, figure 1 also shows an approximation of the signal of interest. As this approximation is being constructed, it is also being compared to the input signal. The binary output corresponds to a “one” if the input signal is greater than the approximation and an output of “zero” occurs if the approximation is greater than the input signal. Each time a “one” is output, the

approximation signal is increased by “delta” units. When the output is “zero”, the approximation signal is decreased by “delta” units; hence, the term “delta modulation”. This toggling between the approximation signal and the input allows the approximation signal to track the rate of change of the input signal through the use of a pulse train. This pulse train is used to construct the approximation and is also the transmitted signal.

This signal is then used at the receiver to reconstruct an approximation of the input signal using a decoder identical to the one at the transmitter; incrementing the approximation by “delta” units if a “one” is received and decrementing the approximation by “delta” units if a “zero” is received. A long sequence of “ones” would correspond to a high rate of increase while a long sequence of “zeros” would correspond to a high rate of decrease. Subsequent low pass filtering removes unwanted noise in the signal and provides a smoothing effect on the overall output signal at the receiver. Figure 2 shows the output pulse train that would occur if a small constant signal were input to the system. The pulse train would idly toggle between “one” and “zero” since at one point, the input would be greater than no “delta” units resulting in an output of “one”. This would be followed by an increase of “delta” units in the approximation which when compared to the input, results in an output of “zero” and a decrement of “delta” units in the approximation and the process continues as fast as the sampling frequency.

A condition that can occur which is an inherent problem in delta modulation is slope overload. This condition occurs when the amplitude of the input signal changes at such a high rate that the system cannot keep up with it and cannot generate an approximation to this high rate of change. This happens because the system is designed to only be able to change “delta” units per clock interval while the input signal could change many more units in positive or negative direction per clock interval so that the slope of the input “runs away” from the slope of the system. This condition can be treated by using double integration schemes or by using adaptive reconstruction schemes that allow the approximation signal to increase or decrease by more units than the original scheme.

DESIGN AND IMPLEMENTATION

THE ENCODER

The final block diagram design is shown in figure 3 so that reasons for the design of each stage could be cited. At the very beginning, research in the field led to the use of a unipolar binary signal instead of a bipolar signal since the decay of voltage from a capacitor is similar to the charging of a capacitor to a negative voltage. The results of using this scheme were a decrease in complexity and a more positive dc offset in the output which is easily taken out with the use of a dc block capacitor. The 555 timer was used as part of the sampling network of the system. It was designed to be operated as an astable multivibrator

with a clock pulse frequency of approximately 60 kHz and an 80% duty cycle so that it could properly trigger the D-flip flop. At first, a half-rectified square wave with a frequency of 60 kHz. was to be used but “ringing” at the transitions from high to low of the pulse had the effect of triggering the D-flip flop more than once. Since one of the aims of the project was to promote the simplicity of the system, the 555 timer was chosen to satisfy part of this requirement. The D-flip flop completes the sampling network of the system. In a sense it samples the semi-continuous difference signal provided by the comparator. It samples the difference signal, be it a “one” or a “zero”, and holds it until the next clock pulse.

The comparator at the front end performs the differencing of the input signal and the reconstructed signal to give a sense of the rate of change of the input signal. It is compatible with TTL logic and outputs a “one” if the input is greater than the approximation, and it outputs a “zero” if the input is less than the approximation. The RC network operates as the local decoder of the system. It is used as an integrating network with a small time constant of about 500 microseconds to provide fast charging and discharging of the capacitor as the output pulse passes through it.

Since the approximated signal output of the RC integrator has a dc offset from the use of a unipolar scheme, it was necessary to add the right amount of dc bias to the input signal so that the approximation may not always be greater than the input signal by the dc offset of the unipolar scheme. At first a small bias was added to the input signal by using an operational amplifier as a summing network which only partially solved the problem because the dc level of the reconstructed signal tended to increase with the increase of frequency. This would sometimes cause the comparator output to go high because either too much dc bias was added to the signal or because the input frequency was too low so that its dc offset was less than the dc bias that was purposely added to the input signal.

Some more time was spent on investigating this problem in which later designs were found that addressed this problem. These designs called for the use of another RC network that was tied to the output of the sample and hold network. This network however, could only charge to the approximate dc value of the reconstructed signal so that it could then be coupled to the input signal. In this fashion, the input signal and the reconstructed signal were forced to have approximately the same dc offset. In the circuit in figure 3, one can easily see that the Q output and the Q-bar output should have the same relative dc offset value when put through an RC network. Resistors R_1 , R_2 and capacitor C_1 serve as this network with a one second charging time constant between R_1 and C_1 , and a two second discharging time constant between R_2 and C_1 . This network found in the literature is called an idle channel stabilizer since it stabilizes the output of the pulse train by adding the approximate dc bias of the approximation signal to the input signal so that a proper comparison of the signals at the comparator could be made. Capacitor C_2 serves as a dc

blocking capacitor so that the dc value of input signal is only the one supplied to it by the stabilizing network. Satisfying the requirement of simplicity, most of the elements in the encoder turned out to be passive.

THE DECODER

The decoder at the receiver consists of an RC network identical to the local decoder at the transmitter with a time constant of approximately 500 microseconds. This causes the same approximation signal to be generated at the receiver. This approximation signal is then input to a low pass filter with a cutoff frequency of approximately 3.2 kHz. which is where many communication engineers agree that most speech content essentially ends. Figure 4 shows the design used for the decoder and figure 5 shows the frequency response of the RC low pass filter used in the decoder. Note that again, all the elements are passive and the requirement of simplicity is satisfied.

One could also make the observation that the reconstruction network is also a low pass filter with a cutoff frequency of about 320 Hz. This means that at the output, signals with components of frequency greater than 320 Hz. will become attenuated simply because of the way in which they are reconstructed and that the same could be said about the input decoding scheme. This problem has been addressed and can be treated with the use of an emphasis filter at the encoder and the decoder. This would have the effect of keeping the same overall amplitude response over the voice spectrum so that reconstruction won't have the effect of distorting the input signal. However, these filters would have called for active elements in the encoder and decoder and would not have met the requirement of simplicity as well as the passive filters.

SYSTEM PERFORMANCE

When the design was finally completed, a series of tests were performed to give an idea as to how well the delta modulation system was performing. The tests consisted of using several sinusoids of different frequencies as input to the system and observing the overall output of the system and making meaningful measurements on the output such as total harmonic distortion.

200 HZ. SIGNAL

Figure 6 show the first test signal used and the output of the system directly underneath it. The reconstruction of the 200 Hz. sinusoid has the same frequency as the input signal and is also scaled down. Figure 7 shows a section of the input signal along with a section of the transmitted pulse train. Note that the pulse density is directly proportional to the rate of change of the input signal. occasional dips in the pulse train correspond to areas where the

reconstructed waveform was greater than the input and it was necessary to lower the value of the approximation so that it could track the input as closely as possible.

800 HZ. SIGNAL

Figure 8 shows the input with the reconstructed output directly underneath. The output signal also has the 800 Hz. frequency of the input. At this point one can see that the reconstructed waveform is beginning to look more like the charging and discharging of an RC network since that is precisely how signal reconstruction is occurring. Figure 9 shows some cycles of the 800 Hz. input along with a section of the transmitted pulse train. Note that since the rate of change is more prominent, the density of the pulse train is more pronounced. This causes the RC network to display the charge-discharge characteristic seen in figure 8.

1200 HZ. SIGNAL

Figure 10 shows a 1200 Hz. input signal along with the reconstructed output of the system. Again the charging-discharging behavior is observed in the output. Due to the greater rate of change of the signal, the output pulse train seen in figure 11 is a little more pronounced with less dips to provide for better approximation of the signal. Solid pulse trains with no occasional dips would be characteristic of a system experiencing slope overload which would call for a decrease of input voltage level or low pass filtering at the front end so the signals with a high rate of change may be slightly attenuated or removed. Figures 6, 8 and 10 show the scaling effect on the output caused by the filtering effects of the reconstruction RC network which were mentioned earlier. At this point, an emphasis filter can be inserted so that the amplitude of the output signals may be kept almost constant.

TOTAL HARMONIC DISTORTION

With satisfactory visual results accomplished, it was decided that some qualitative measurements should be made. Figure 12 shows the display of a dynamic signal analyzer when used to make total harmonic distortion measurements. Figure 12 shows that with a sinusoidal input signal with a frequency of about 200 Hz. the output signal of the system had harmonic distortion of about 3%. Since some of the harmonic markers did not land exactly where the harmonics were located when the measurement was performed, this measurement could in actuality be about 5 or 6% keeping in mind that prior experience with the characteristics of the function generators has shown that their signals output also have some harmonic distortion of about 2%. Figure 13 shows the same display for an input sinusoidal signal with a frequency of about 400 Hz. At this frequency, the output signal is calculated to have about 7% harmonic distortion which is relatively good for recognition. Similarly, figure 14 shows the same display for an input sinusoidal signal with a frequency

of about 900 Hz. It shows that the calculated harmonic distortion at this frequency is about 9% which is also good for signal recognition. These qualitative measurements helped to determine that under test conditions, the system was working satisfactorily.

SPEECH TESTING

Having performed all of these measurements which showed that the system was operating satisfactorily, it was ultimately decided that since the system was designed to digitally transmit voice, then a voice signal should be put into the system and listened to at the other end. Therefore, the electrical signal from a microphone was amplified to a reasonable level, from millivolts to volts, and fed into the system. The output was fed into a loss amplifier to scale down the output signal and was subsequently fed into an amplifier system with a loud speaker so that the voice message could be listened to. Despite the researcher's skepticism, the output message signal was quite intelligible. The system was working beautifully although a slight hiss could be heard in the background which the inventor of the system calls "granular noise" due to the "sandy" or "grainy" quality of the output speech message.

DELTA MODULATION VS. PULSE CODE MODULATION

SIGNAL TO NOISE RATIO

Thus far, this report has shown with what ease delta modulation is performed and how well one of the systems operates. However, another standard for comparison is needed. Therefore, delta modulation will be compared to the conventional method of digitally transmitting signals; pulse code modulation (PCM) which is quite a bit more complex. Figure 15 shows the signal-to-ratio (SNR) versus output bit rate for pulse modulation, theoretical delta modulation and experimental delta modulation. One can easily see that at low bit rates, SNR for delta modulation is greater than the SNR for pulse code modulation and that the two intersect at about 40 kilobits per second where the SNR for PCM begins to exceed the SNR for delta modulation. Voice intelligibility is good for output bits greater than 40 kilobits per second for delta modulation with little change in intelligibility past this value.

GENERAL CHARACTERISTICS

Due to the large amount of samples needed for delta modulation, time division multiplexing is not well suited to this type of system as it is to pulse code modulation where the sampling rate is significantly lower. PCM has no dependence on the frequency of the input signal while delta modulation systems can go into slope overload at high frequencies and high amplitudes. Delta modulation requires no synchronization between

the transmitter and the receiver where synchronization is at the heart of PCM systems. It also has high tolerance to errors. If 4 bits are lost during transmission in a delta modulation system, the effects may go unnoticed, if the same thing were to happen in a PCM system, the transmitted message would be of no use. Therefore, PCM systems require expensive hardware to ensure that the probability of bit error is very low which also drives the cost of such systems to high levels. It has been shown that by using some resistors and capacitors, a clock circuit, a comparator and a D-flip flop, excellent results could be obtained from delta modulation at little expense. Filter requirements for the systems are also very different. PCM systems call for active filters with sharp roll offs which also have a high price tag while delta modulation systems call for simple filters with simple requirements and no sharp roll off requirements to meet.

CONCLUSION

The principle of delta modulation was presented to give an idea as to how this principle may be implemented and used effectively for the digital transmission of speech. The development of a delta modulation system over the period of four months was then presented along with its visual, qualitative and audio performance with test signals such as sinusoids of different frequencies and human speech. The system was shown to operate satisfactorily under all tests and was shown to be an excellent communication system. Subsequent comparisons with pulse code modulation systems were made and also showed that, in many respects, delta modulation was superior to pulse code modulation, the “conventional” scheme of digital communications.

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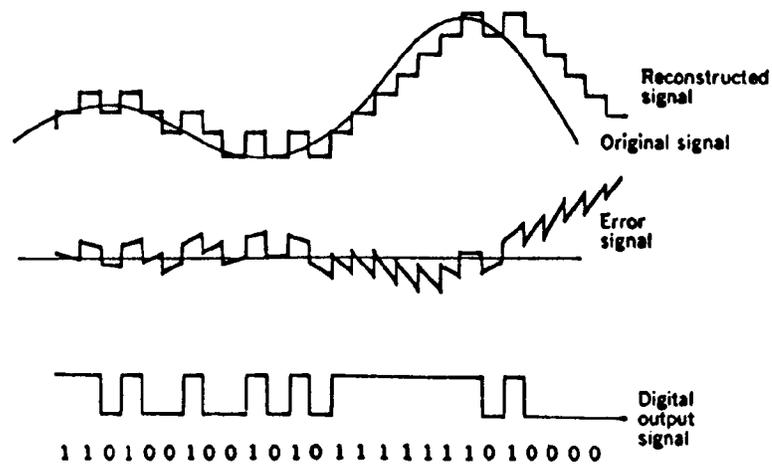


Figure 1

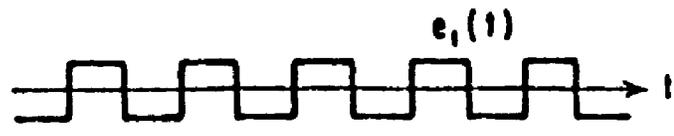


Figure 2

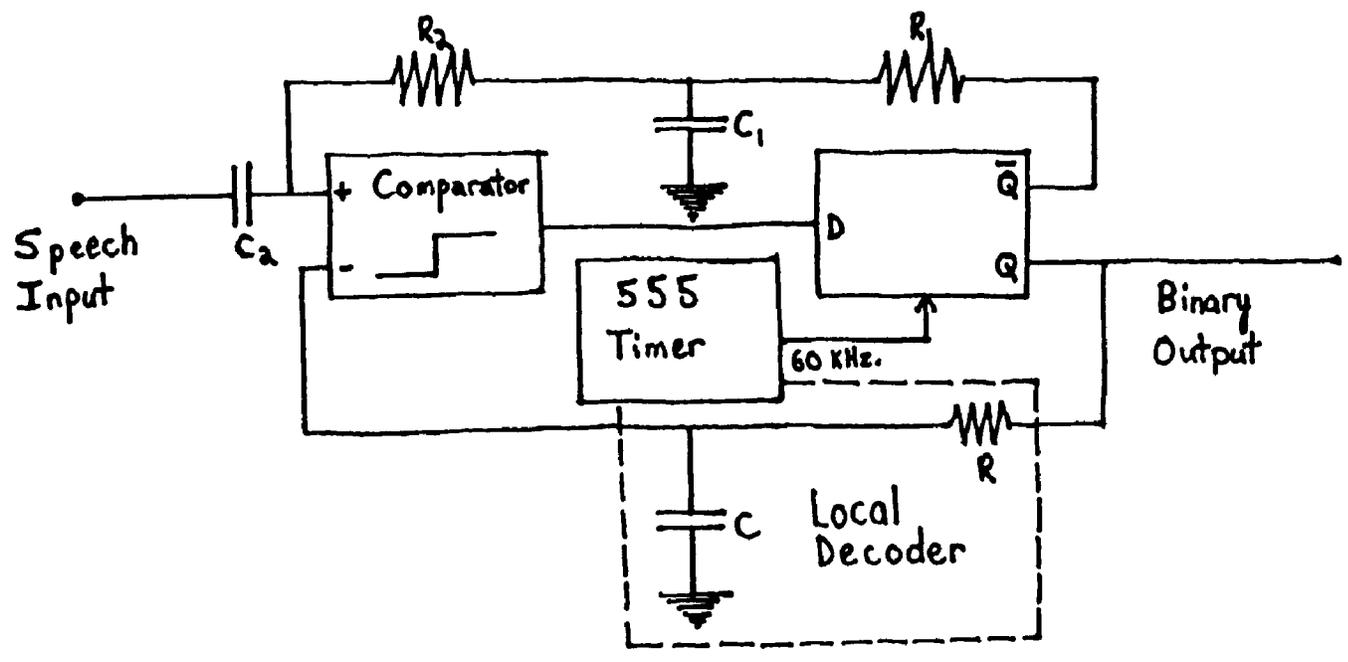


Figure 3

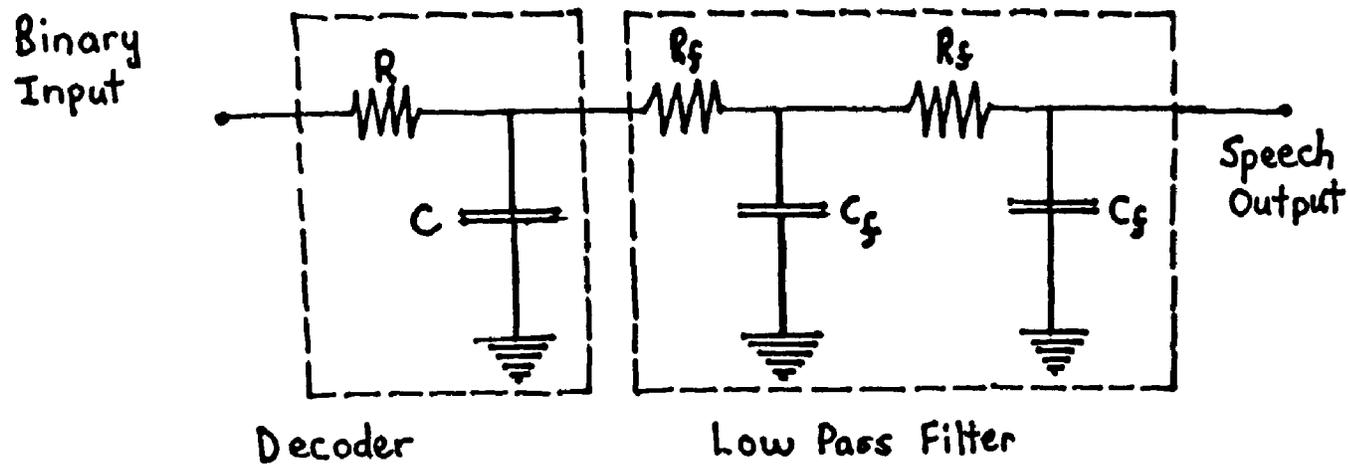


Figure 4

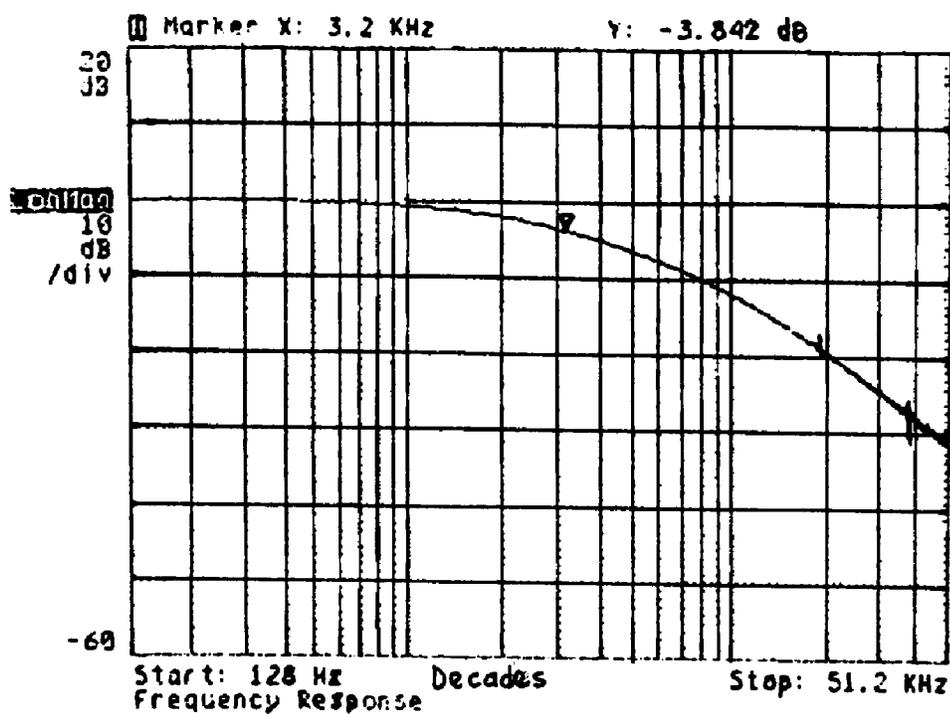


Figure 5

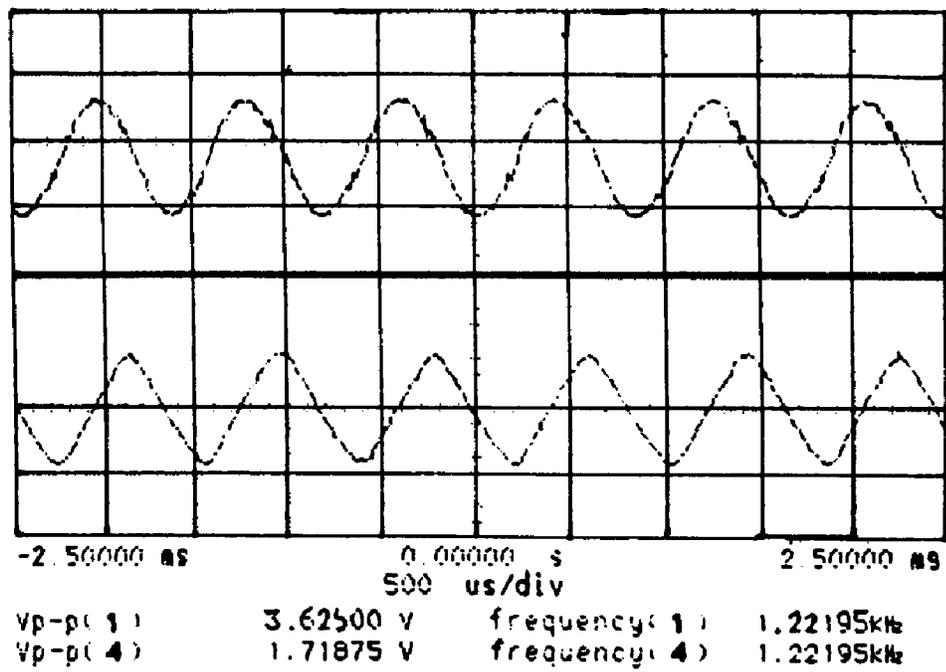


Figure 10

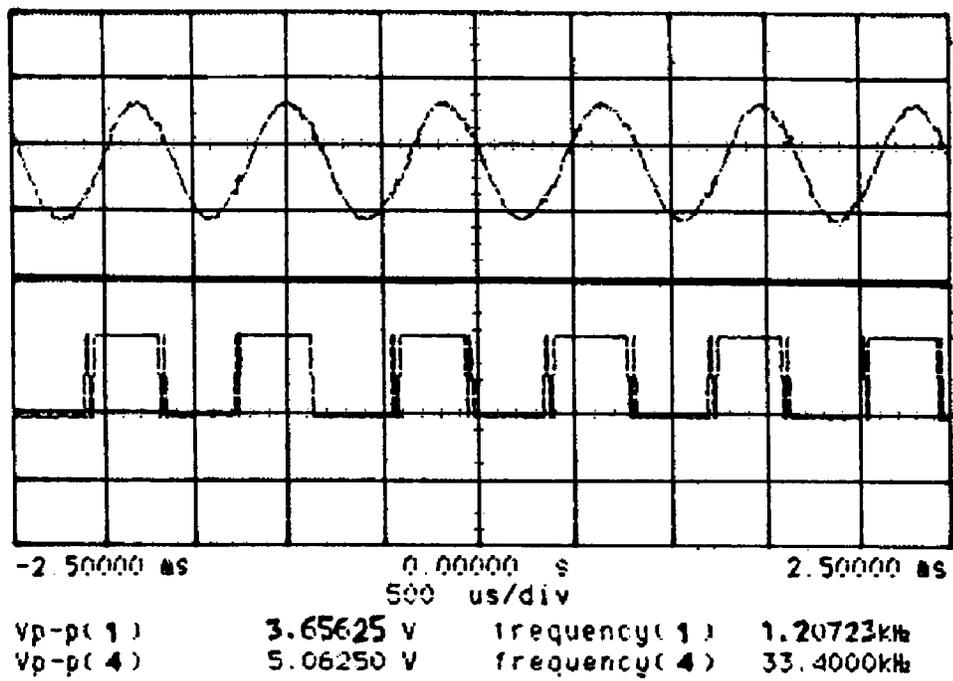


Figure 11

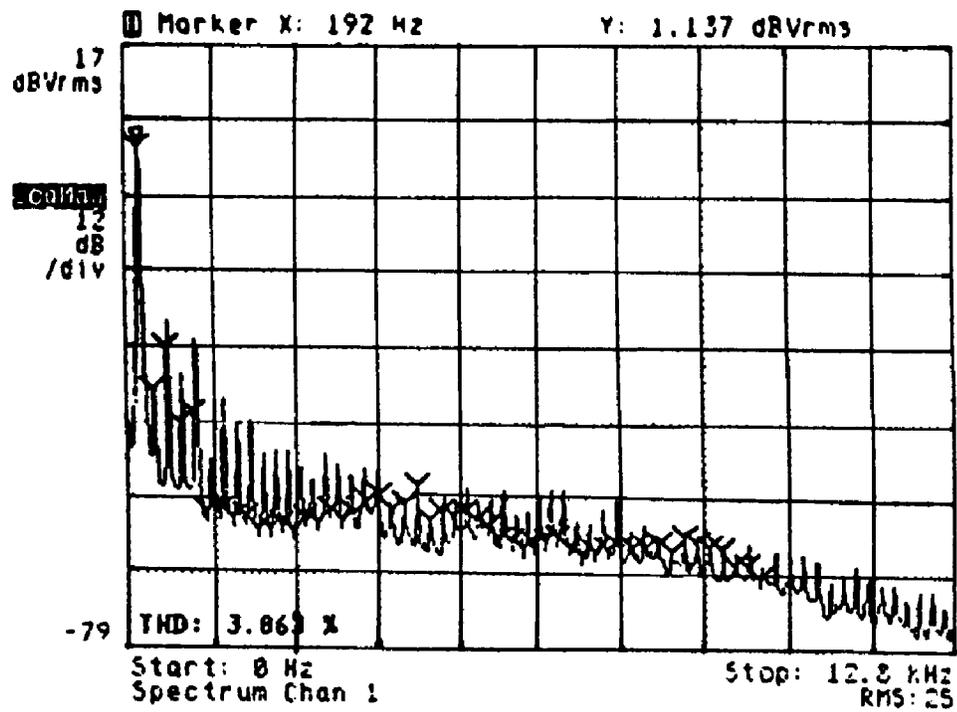


Figure 12

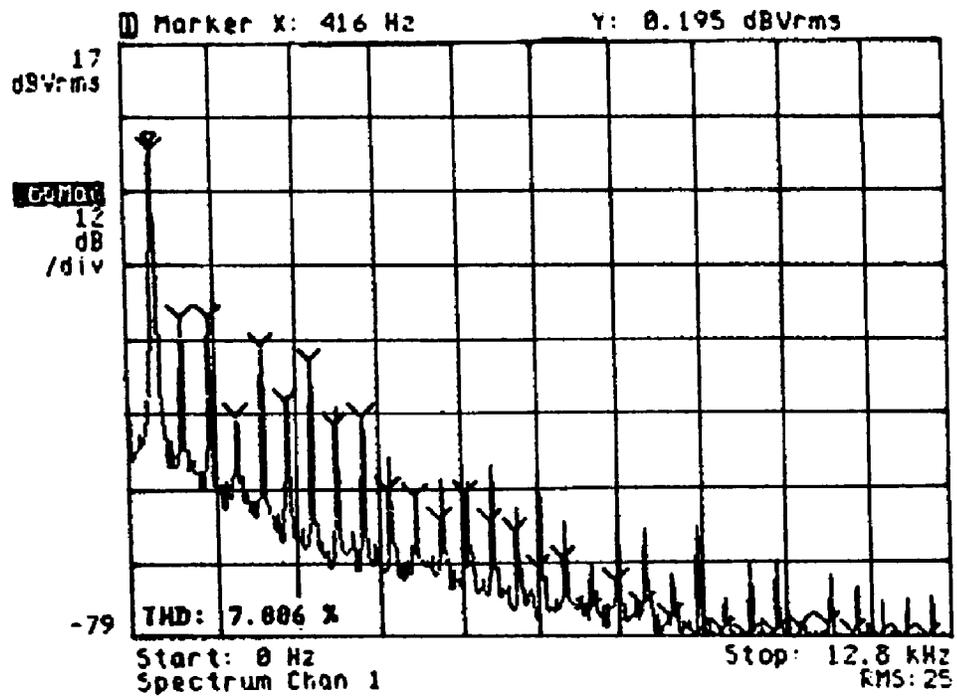


Figure 13

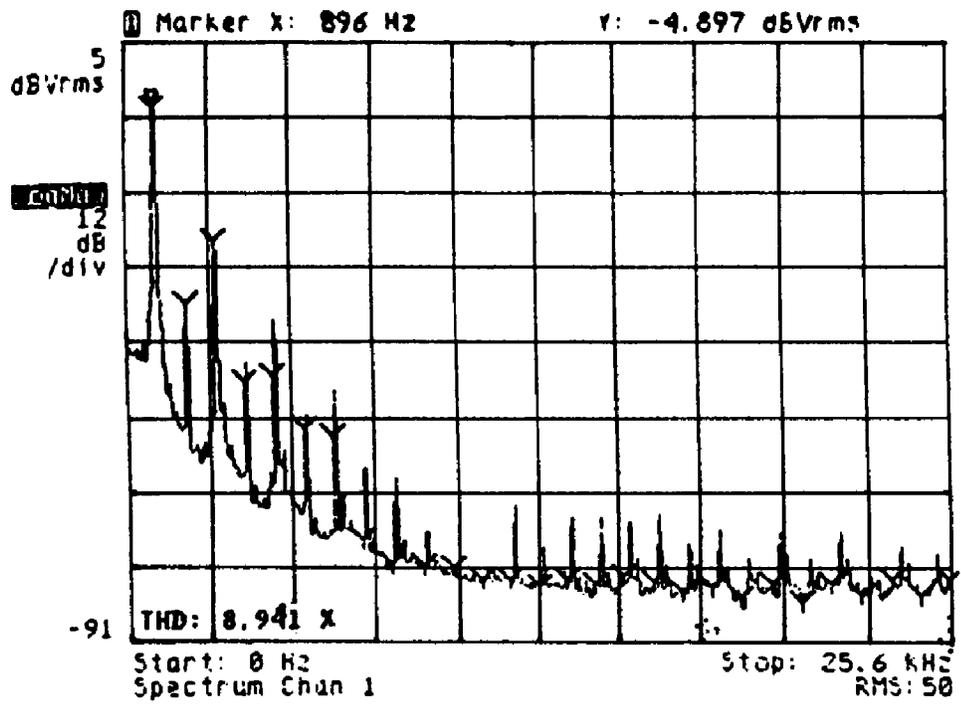


Figure 14

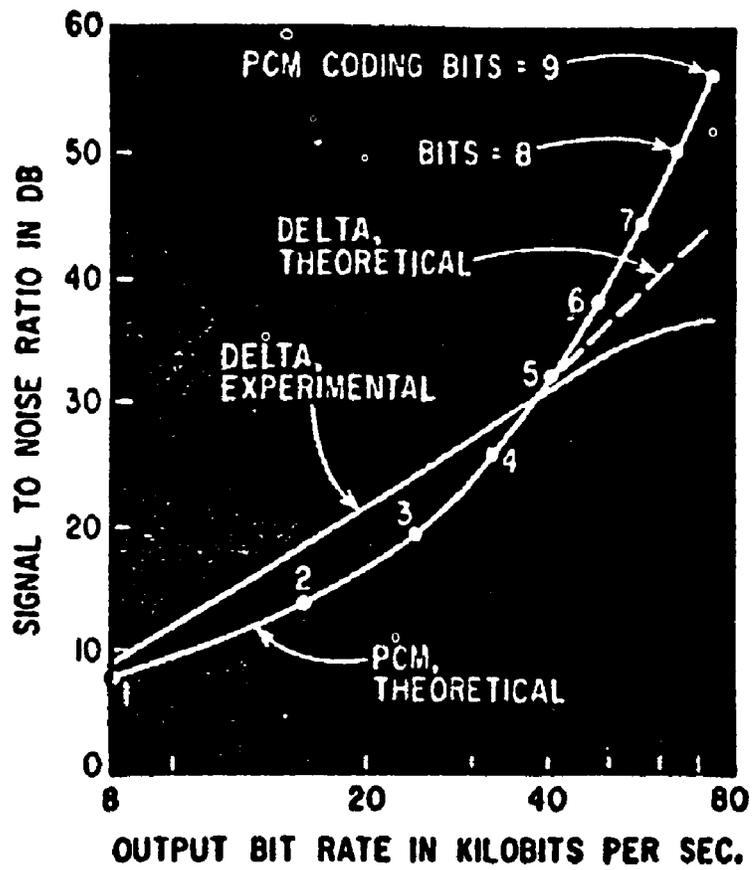


Figure 15