S-BAND CIRCULARLY POLARIZED MICROSTRIP PHASED ARRAY

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ABSTRACT

A highly efficient circulary polarized S-band microstrip planar phased array is described. The array is:

- Electronically steerable in elevation and azimuth
- Highly efficient at the subarray level (greater than 60 percent)
- Well matched for active impedance with a near cos a scan performance
- Designed for optimum G/T performance
- Designed to have a thin profile but be extremely strong

The microstrip elements, phase shifters and combiner network are described in detail and their operation is explained.

KEY WORDS:

Phased Array
Microstrip Antenna
PIN Diode
Phase Shifters
G/T Figure of Merit
LNAs (Low Noise Amplifiers)

INTRODUCTION

Highly efficient phased array antennas with thin profiles that can be produced at low cost will be needed for many current and future ground fixed, ground mobile and airborne communication links.

The development of a S-band electronically scanned phased array was undertaken to demonstrate state-of-the-art efficiency performance over a wide range of scan angles and to develop a configuration which has a thin profile and can be produced in a production environment using robotics.

The requirements for this phase are listed below:

- Operation from 2.2 to 2.3 Ghz
- Right-hand circular polarization with axial ratio less than 3 dB
- Scan volume ±50° in elevation and ±10° in azimuth
- Efficiency greater than 60 percent at midband and greater than 50 percent at the band edges
- Scan performance with less than 2 dB of loss out of 45° elevation scan angles
- Able to operate in a ground mobile environment
- Producible in quantity at reasonable cost

These requirements have been satisfied in a development and antenna production program at Ball Aerospace.

APPROACH

A microstrip phased array design approach was chosen for this application because of the need for a low profile and high efficiency. Figure 1 shows an exploded view of the all microstrip phased array concept. The elements are teflon fiberglass round microstrip elements. The phase shifter layer consists of PIN diode microstrip phase shifters and a 64-way microstrip corporate feed all etched from a single copper laminated teflon fiberglass substrate. The outboard element layer and the phase shifter layer are separated by a common ground plane structure which supplies stiffness and strength to the phased array. Figure 2 shows a rear view of two 64 subarrays built into one integral frame.

Figure 3 shows how the elevation and azimuth element spacings are chosen in order to satisfy the grating lobe equations over the required scan volume. The microstrip radiating element layer shown in Figure 4 is fed with a quadrature hybrid branch line coupler in order to provide circular polarization. The quadrature hybrid couplers are located on the output of each element phase shifter.

The element phasing for each of the beam position was obtained by using a 3-bit phase shifter at each individual element. For each beam position, the element phase shift state for the upper left-hand most element is computed along with the incremental azimuth and elevation phase shifts between each successive column and row elements. The beam steering controller then ships the data out serially to all 128 phase shifters drivers.

Although the phase shifter settings are computed with 16-bit accuracy, the actual phase setting of each element is latched into the closest of eight phase settings (0°, 45°, 90°, 135°, 180°, 225°, 270° and 315°) which can be achieved with a 3-bit phase shifter.

PHASE SHIFTER DESIGN

Figure 5 shows the 3-bit PIN diode phase shifter. The 90° and 180° bits are reflection phase bits which are made by loading the 0° and 90° ports of a quadrature hybrid coupler with high reflection coefficient loads with the appropriate phase angle differences between the ON and OFF states for each phase bit. This approach was chosen because only two diodes per bit are required and only one DC bias control line is needed per bit.

The 45° bit is a narrow band loaded line bit. This bit has a limited bandwidth in the ON condition as can be seen by the performance data at 2300 MHz for the 45°, 135° and 315° phase state shown in Table I. A broad band loaded line approach could have been built by having the diodes shunted to ground at the end of each stub. However, this configuration would have required using blocking capacitors at the input and output side of this bit and it also required more real estate.

Axial leaded glass package PIN diodes were used for the active phase shift devices. A package PIN diode was selected because it will survive a high humidity environment and they proved to be easily installed using robotics. During the production phase of this program, it was demonstrated that all 128 phase shifters could be populated with PIN diodes by a programmed robot within an 8-hour period. Our robotic capability helped reduce the assembly cost and provided consistent solder joints that needed very little rework. Figure 6 shows the robot soldering in a PIN diode in the 90° bit of one phase shifters. Figure 7 shows the entire robotic station populating an entire 128-element phased array panel with PIN diodes and bias choke capacitors.

G/T OPTIMIZATION

In order to optimize the G/T performance of an array of several phased array panels shown in Figure 1, Low Noise Amplifiers were integrated into the array at each 64 element level. By integrating high gain LNAs ahead of the array combiner losses, a lower system noise temperature can be established. An array of thirty-six 64-element subarrays was built with 36 LNAs integrated into the aperture. This array achieved a remarkable G/T performance of ±14 dB/°K. An additional 3 dB improvement could be achieved by integrating Low Noise Amplifiers at the element level. However, since the cost of these amplifiers is relatively high, this approach was not a cost effective and was not considered for this program.

Another important consideration in optimizing the G/T performance is to reduce the losses in front of the subarrays LNAs. Figure 8 shows the gain and the efficiency of a 64-element subarray. The maximum area gain of a lossless array that size is 25.3 dB. The measured CP gain was ≅23.5 dBi at the center of the band. A loss of less than 2 dB was achieved by having a low loss phase shifter (.95 dB average), a low loss microstrip corporate feed board (.65 dB) and a very efficient microstrip element (.2 dB).

SCAN PERFORMANCE

The aperture was designed so that smooth scanning performance would be achieved from broadside out to 50° scan angles in elevation. Ideally the perfectly match aperture will give a cos θ scanning performance for all scan angles. Figure 9 shows a peak of beam mapping of several beams from broadside out to 50°. Notice that the scan loss degradation in dB closely matches a 10 log (cos θ) function and that there are no coverage drop outs. This data indicates that the active element impedance is very well matched at all scan angles.

Figure 10 shows a measured broadside elevation pattern of the 128-element array shown in Figure 2. This pattern is almost text book perfect for a uniformly excited aperture. Notice the 13 dB first sidelobe levels and the sin u/u sidelobe roll off performance. Figures 11 and 12 show the ±25° and ±45° elevation beams respectively. Again these beams are well formed and agree reasonably well with computer predicted patterns.

CONCLUSIONS

An S-band phased array has been developed which is very efficient, has excellent scanning performance can be steered electronically in both azimuth and elevations planes, and is very thin. The design concepts developed on this program can be used to satisfy the performance requirements of future ground mobil, ground fixed, and airborne communication terminals. The panels can be arrayed together to satisfy several different combinations of gain and beamwidth requirements. Integration of LNAs at the subarray level can provide a receive communications terminal with a very good G/T figure of merit.

Installation of PIN diodes and capacitors in the phase shifter circuitry by robotics has demonstrated both lower cost assembly techniques and more reliable solder joints (see Figure 6).

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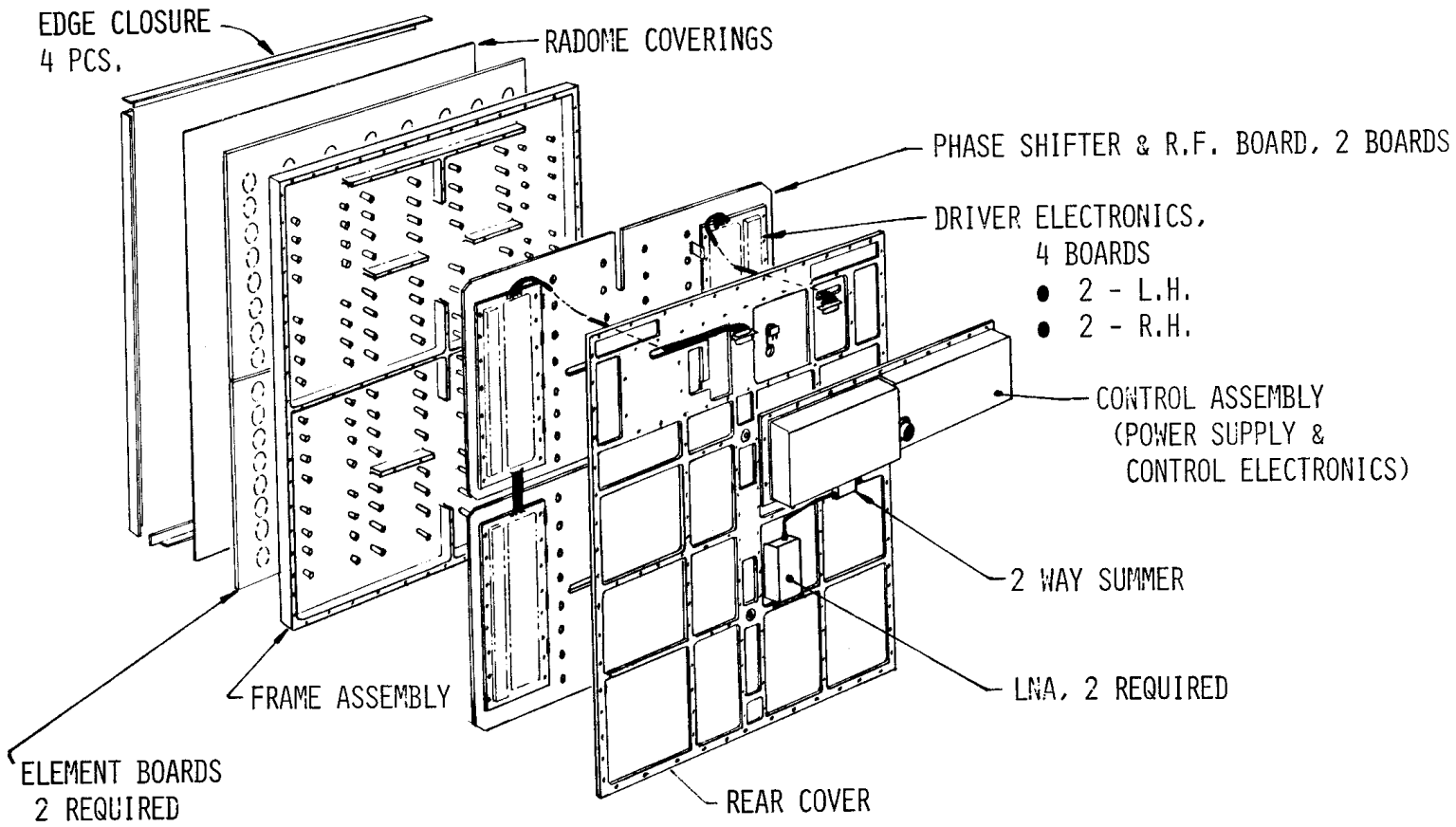


FIGURE 1. SUBARRAY ASSEMBLY

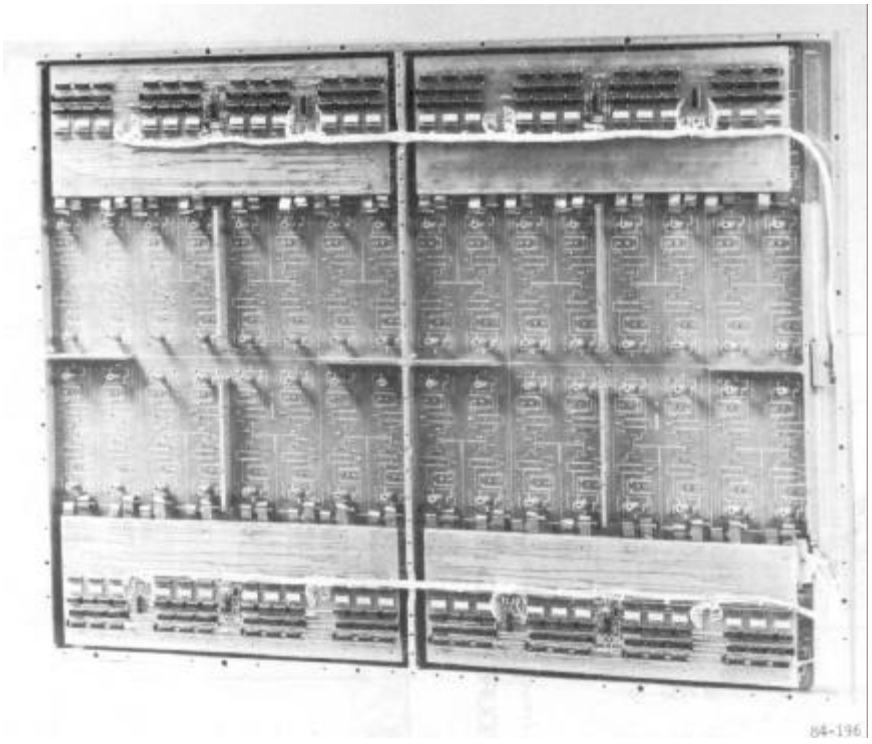


FIGURE 2. 128-ELEMENT SUBARRAY REAR VIEW

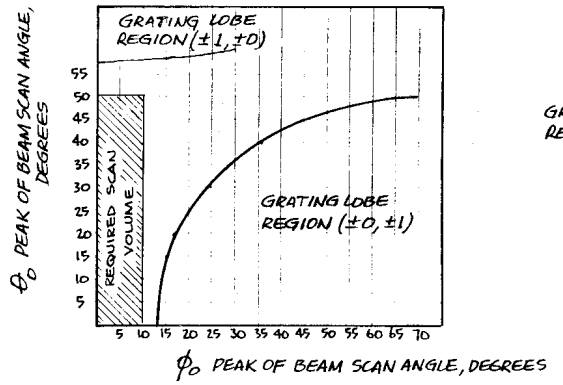
GRATING LOBE EQUATION RECTANGULAR GRID *

$$\sin\phi\cos\theta = \sin\phi_o\cos\theta_o + q(\lambda/a_x) \quad q = 0, \pm 1, \pm 2$$

$$\sin\theta = \sin\theta_o + p(\lambda/a_z) \quad p = 0, \pm 1, \pm 2$$

$a_z = .54\lambda$ (FREQ = 2300 MHz)

$a_x = .82\lambda$ (FREQ = 2300 MHz)



GRATING LOBE REGIONS (0, ±2) (±2, 0) (±1, ±1) DO NOT EXIST

* K.H. HERING, JAN 1971 THE MICROWAVE JOURNAL, PAGES 41-51

FIGURE 3. SCAN VOLUME/GRATING LOBE REGIONS

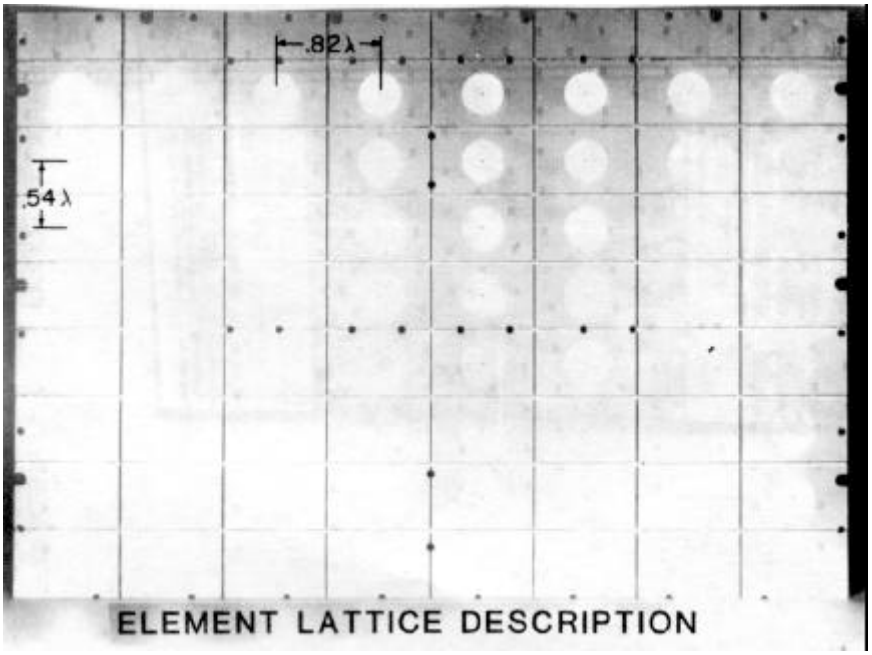


FIGURE 4. ELEMENT LAYER

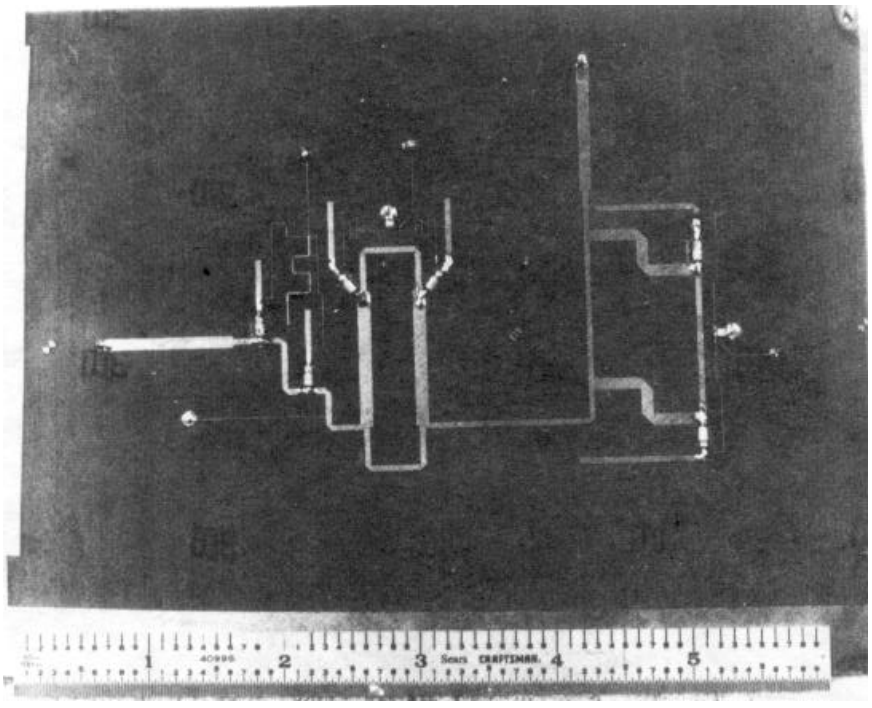


FIGURE 5. PHASE SHIFTER

TABLE I.

MEASURED PHASE SHIFTER INSERTION LOSS PERFORMANCE

	FREQUENCY (MHz)				
	2200	2222	2232	2242	2300
0^0	.65DB	.6 DB	.6 DB	.6 DB	.7 DB
45^0	.85DB	.85DB	.85DB	.85DB	1.05DB
90^0	.85DB	.85DB	.85DB	.8 DB	.9 DB
135^0	1.05DB	1.1 DB	1.1 DB	1.15DB	1.55DB
180^0	.90DB	.85DB	.85DB	.85DB	.85DB
225^0	1.05DB	1.1 DB	1.1 DB	1.1 DB	1.2 DB
270^0	1.05DB	1.0 DB	1.0 DB	.95DB	1.0 DB
315^0	1.25DB	1.3 DB	1.3 DB	1.35DB	1.65DB

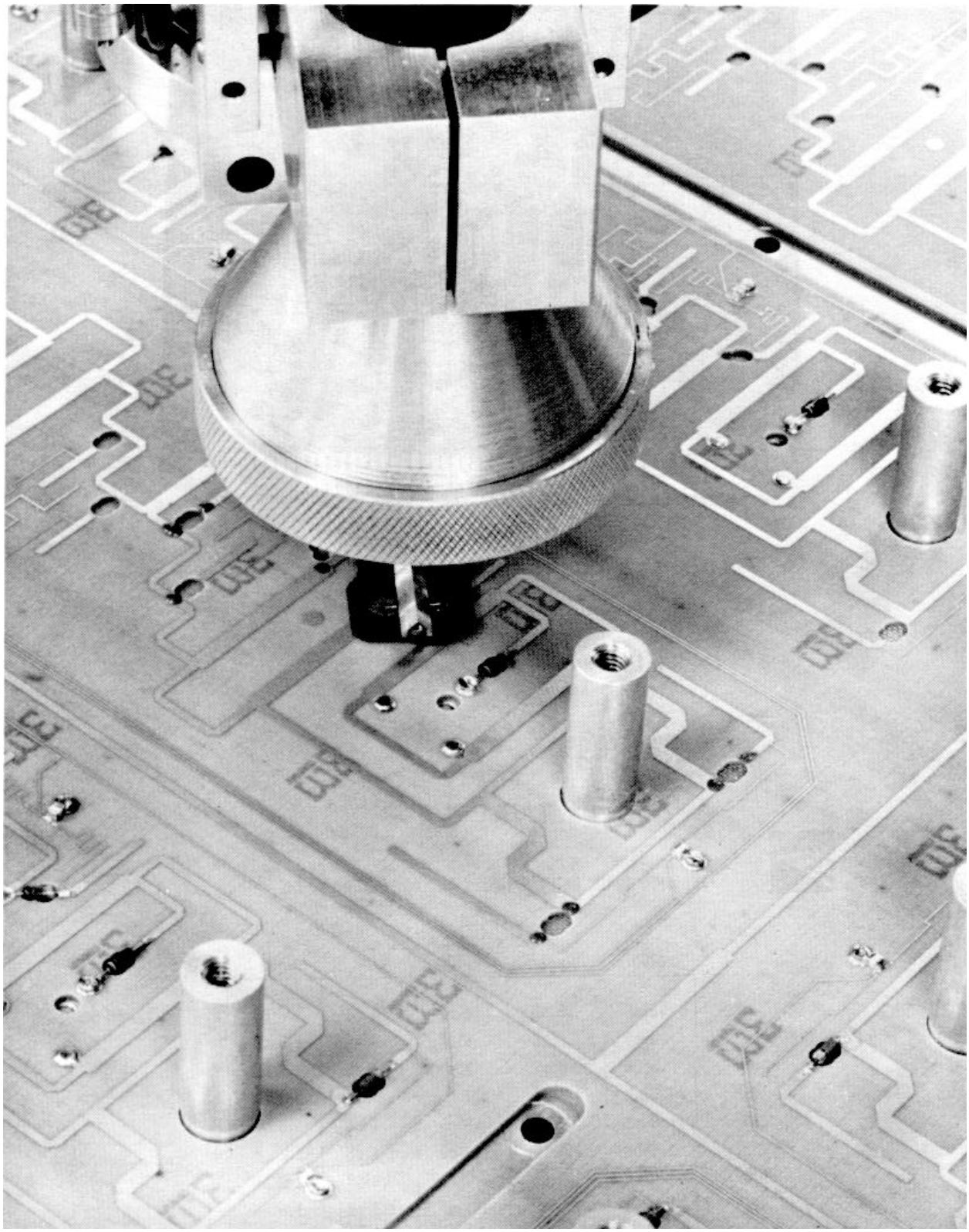


FIGURE 6. ROBOTIC DIODE INSTALLATION

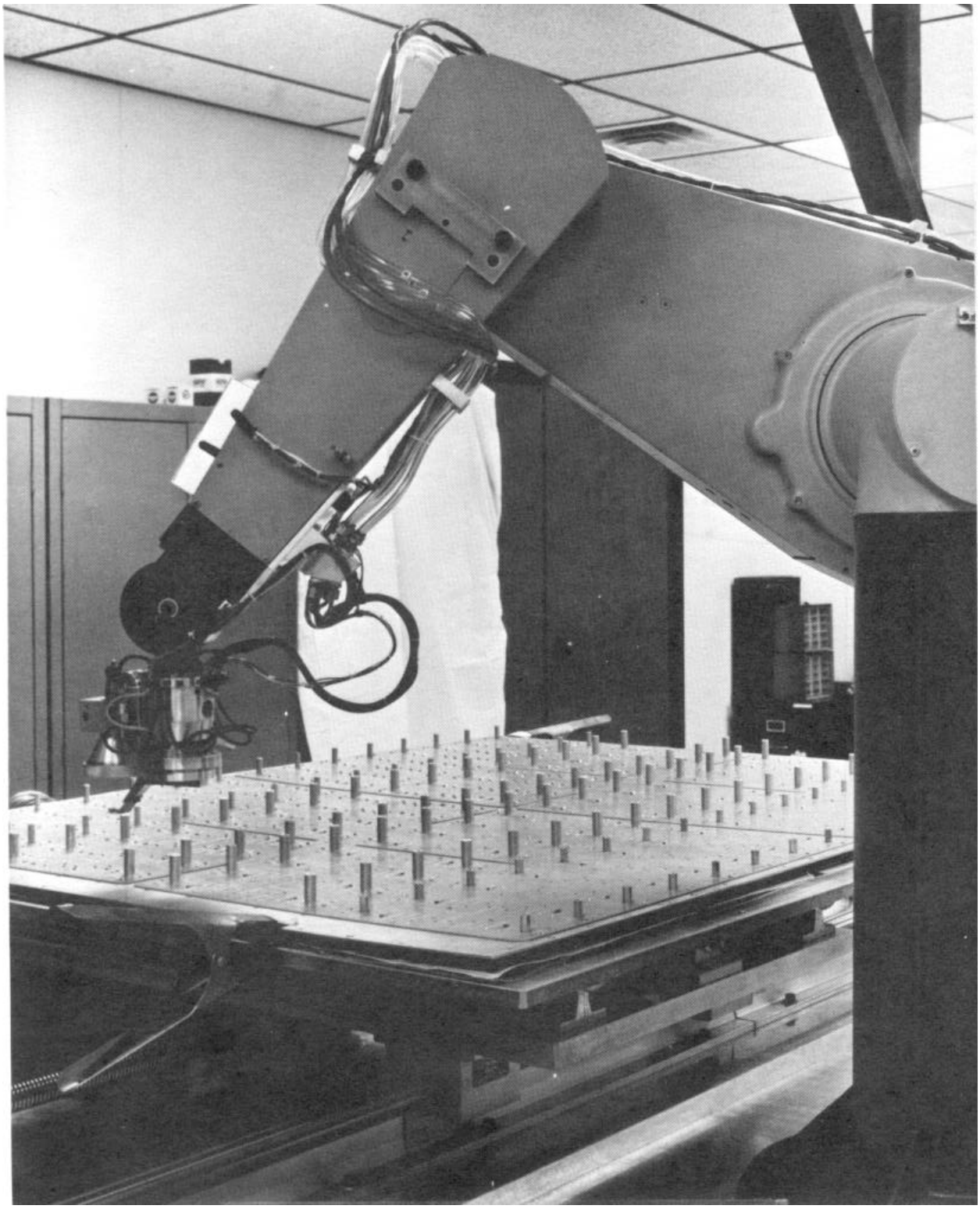


FIGURE 7. ROBOTIC STATION

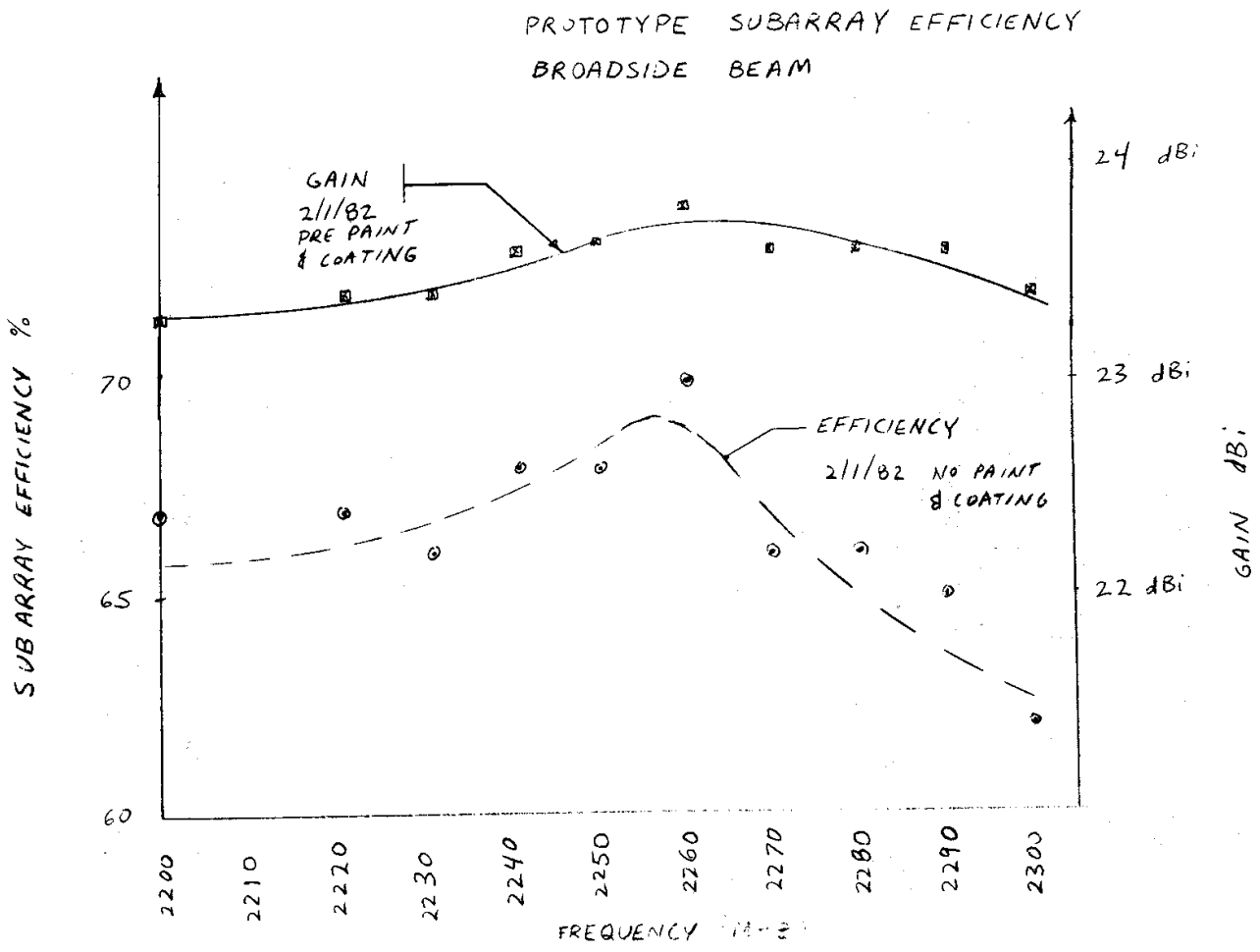


FIGURE 8. 64-ELEMENT SUBARRAY GAIN AND EFFICIENCY

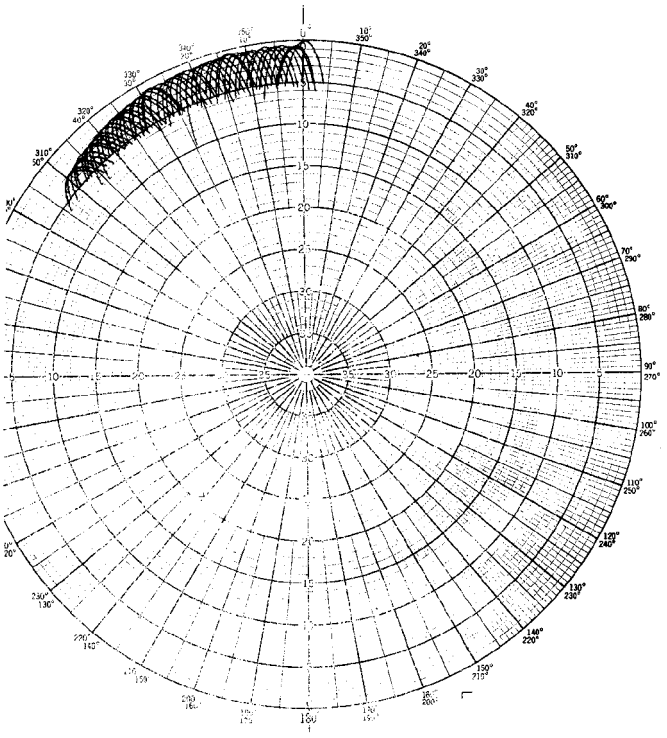


FIGURE 9. ELEVATION SCAN COVERAGE

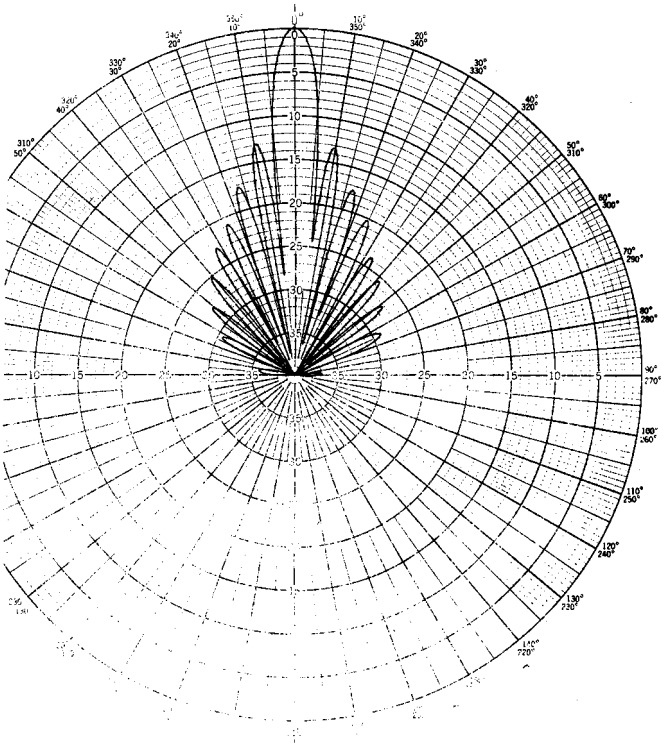


FIGURE 10. BROADSIDE ELEVATION BEAM

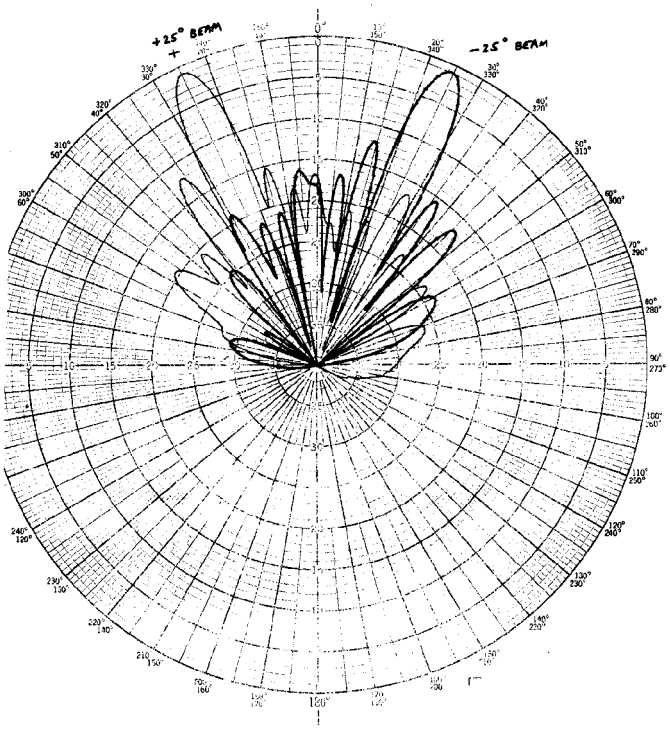


FIGURE 11. ELEVATION SCAN BEAMS ± 25 DEGREES

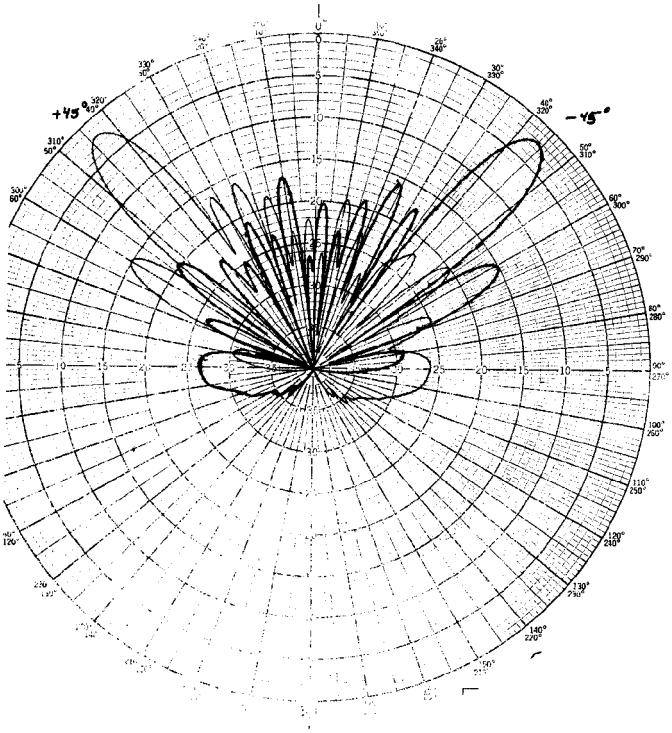


FIGURE 12. ELEVATION SCAN BEAMS ± 45 DEGREES