BIT SYNCHRONIZATION IN THE PRESENCE OF ASYMMETRIC CHANNEL NOISE

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ABSTRACT

Bit synchronization in the presence of asymmetric channel noise has not appeared in the open literature. It is the purpose of this paper to study the performance of a popular digital clock synchronizer, the Digital Data Transition Tracking Loop (DTTL), in the presence of asymmetric noise. A comparison of the DTTL and Cross Spectrum Synchronization Loop (CSSL) is also provided for special parameter values of greatest interest. Numerical results are presented for design of bit synchronizer in this environment.

1. INTRODUCTION

Complex channels may give rise to noise asymmetry, such as asymmetry in probability density function [2], and asymmetry in noise power level. Examples of channels with noise asymmetric in power level include channels with multipath effects, and the optical channels. Channels which have multipath effects, e.g., sonar channels, will experience asymmetric power level noise. If a pulse is transmitted through a multipath channel, the strength of the interference due to the random diffractions of paths other than the direct path will depend on the signal pulse strength. For the time when no pulse is transmitted, this signal dependent interference does not exist.

A bit synchronizer is an essential component of a coherent digital receiver. Accurate clock timing required for bit detection should be generated with good reliability and under a large dynamic range of signal-to-noise ratios. The synchronizer chosen in this study is the well known Digital Data Transition Tracking Loop (DTTL) [3-5]. Besides the digital nature, the structure the the DTTL can be shown to be motivated by the Maximum A Posteriori (MAP) criterion [6].

Although the performance of the DTTL under certain circumstances is known, its behavior under asymmetric noise in the presence of data asymmetry and varying transition density is still to be investigated. It is the purpose of this paper to study the tracking

performance (clock jitter and cycle slip rate) and the acquisition performance (frequency acquisition time) for these cases. Performance comparison between DTTL and CSSL is also presented.

2. SIGNAL MODEL

The DTTL is perceived to operate in wideband channels, ie., zero intersymbol interference. NRZ signaling format is used in this study. Data asymmetry is introduced as part of the signal model. It arises from the signal generator in the transmitting end which is caused by unequal rise and fall times of the logic gating circuits [7]. This "imperfect" data transition timing is expected to increase the receiver clock jitter. The normalized data asymmetry, η, is defined to be

$$\eta = \frac{\text{long bit interval - short bit interval}}{\text{long bit interval + short bit interval}} = 2\Delta \tag{1}$$

where Δ is defined in Fig. 1, and p and q are the a priori probabilities of the data taking on values 1 and -1 respectively. The transition density is defined as $p_t = 2pq$ for independent data bits. The effect of the asymmetry noise, along with the data asymmetry and transition density, will be of interest to bit synchronizer design.

3. ASYMMETRIC POWER LEVEL NOISE

The asymmetric channel noise is modeled as a product of a cyclostationary process and white Gaussian noise $n_w(t)$. The cyclostationary process is a function of the signal pulse waveshape, which leads to yield a signal dependent noise. Let the noise $n_w(t)$ be zero mean white Gaussian and has a two-sided power spectral density of 1 watt/Hz. Let $N_1 \geq 0$, $N_2 \geq 0$ and define the quantities

$$v_1 \triangleq \sqrt{N_1/2}, \qquad v_2 \triangleq \sqrt{N_2/2}, \qquad \Delta(k) \triangleq \begin{cases} 1 ; & k = 0 \\ 0 ; & k \neq 0 \end{cases} \tag{2}$$

The asymmetric noise for MRZ signaling format is defined as

$$n_A(t) \triangleq f_A(t) n_w(t) \tag{3}$$

where

$$f_A(t) \triangleq \sum_i z_1(a_i) q_T(t-iT) \tag{4}$$

$$z_1(a_i) \triangleq v_1 \Delta(a_i - 1) + v_2 \Delta(a_i + 1) \tag{5}$$

and

$$q_T(t) \triangleq \begin{cases} 1 ; & 0 < t < T \\ 0 ; & \text{otherwise} \end{cases} \tag{6}$$

The mean of $n_A(t)$ is zero since $n_w(t)$ is zero mean and $f_A(t)$ and $n_w(t)$ are assumed statistically independent. The autocrrelation function of $n_A(t)$ is

$$E[n_A(t)n_A(t+\tau)] = \frac{1}{T}\int_0^T E_s[f_A(t)f_A(t+\tau)]E_n[n_w(t)n_w(t+\tau)]dt \tag{7}$$

The subscripts s and n in the expectation sign represent the average over signal and noise respectively. Substituting (4) and (5) into (7) and simplifying, we obtain

$$E[n_A(t)n_A(t+\tau)] = (pv_1^2+qv_2^2)\,\delta(t) \tag{8}$$

The process nA (t), besides cyclostationary, is also wide-sense stationary in an interval [8]. This is clear since within $iT \le t \le (i+1)T$, $n_A(t)$ is simply a white Gaussian noise. From (8), we see that the linear system theory applies to $n_A(t)$.

4. THE DTTL MODEL

Consider the DTTL shown in Fig. 2. Its equivalent mathematical model, in terms of a PLL, is given by Fig. 3. If the samplers in Fig. 2 are replaced by sample-and-hold circuits, then the error signal e_k will become a continuous staircase type waveform e(t). Its statistical mean conditioned on the normalized timing error λ, is the phase detector characteristic $g(\lambda)$, which is also commonly termed the loop S curve . Its power spectral density conditioned on fixed λ is denoted by $S(\omega, \lambda)$ which is a function of radial frequency ω and timing error λ. Here $\epsilon(t)$ is the random epoch to be estimated. The equivalent additive noise $n_\lambda(t)$ is assumed to have a zero mean and two-sided spectral density $S(\omega, \lambda)$. For tracking, in which the timing error λ is small, linear analysis is usually sufficient for performance measure. Therefore, the loop filter is assumed to be a constant K_p, and T is the symbol period. For most practical interests, the symbol time-loop bandwidth product is assumed to be much less than 1, i.e., $W_L T << 1$. In the steady state the bit synchronizer operates at $\lambda \cong 0$, therefore $S(\omega, \lambda)$ can be approximated by S(0,0). Under these situations, the steady state probability density function is given by[6]

$$p(\lambda) = C \exp\left[\frac{-2}{KS(0,0)}\int_0^\lambda g(u)du\right] ; \quad -\frac{1}{2} < \lambda < \frac{1}{2} \tag{9}$$

with $K = K_V K_p$ and C is a normalization constant chosen such that the total probability that $\lambda \epsilon [-1/2, 1/2]$ is unity. For small $|\lambda|$, we have

$$g(\lambda) \cong g(0) + g'(0)\,\lambda \tag{10}$$

Define the nominal loop bandwidth W_{LO} to be

$$W_{LO} = W_L \Big|_{\substack{R_s \to \infty, p=0.5 \\ \eta=0, \ell=0}} = \frac{1}{2} K K_2 A \tag{11}$$

where A is the signal amplitude of the PCM signals, and K_2 is the gain in the lower arm of the DTTL. Also define the signal-to-(thermal) noise ratio to be

$$R_s = A^2\, T/N_0 \tag{12}$$

where N_0 is the one-sided thermal noise power spectral density.

5. DTTL PHASE DETECTOR CHARACTERISTIC

The procedure in generating the phase detector characteristic g (λ) for DTTL with data asymmetry, transition density, and asymmetric noise can be generalized from the one in [4]. Due to the complexity of the procedure g (λ) is found by numerical method. Typical results are provided in terms of the parameters of interest. The normalized S-curve is defined as

$$g_n(\lambda) = \frac{g(\lambda)}{g(0)\Big|_{\substack{R_s \to \infty, p=0.5 \\ \ell=0, \eta=0}}} = \frac{E_{n,s}[e_k \mid \lambda]}{K_2 A} \tag{13}$$

where $E_{n,s}[\ ]$ represents expectation over the signal and noise.

6. DTTL LOOP EQUIVALENT NOISE SPECTRUM $S(\omega, \lambda)$

The additive noise $n_\lambda(t)$ in Fig. 2 is defined to be

$$n_\lambda(t) \triangleq e(t) - g(\lambda) \tag{14}$$

$n_\lambda(t)$ has zero mean and spectral density $S(\omega, \lambda)$,

$$S(\omega, \lambda) \triangleq F.T.\{\langle R(t, \tau; \lambda) \rangle\} \tag{15}$$

$$R(t,\tau;\lambda) \triangleq E_{n,s}\{n_\lambda(t)n_\lambda(t+\tau)\,|\,\lambda\} \tag{16}$$

where F.T. is the Fourier Transform operator, and < > is the time average operator. Since n_λ (t) is conditionally cyclostationary, i.e., its autocorrelation function $R(t,\tau;\lambda)$ is periodic in t with period T, given fixed τ and λ, we have

$$\langle R(t,\tau;\lambda)\rangle = R_0(m,\lambda) + \frac{1}{T}(\tau - mT)[R_0(m+1,\lambda) - R_0(m,\lambda)]$$

$$mT \le \tau \le (m+1)T, \quad m = 0, \pm1, \pm2, \ldots$$

where

$$R_0(m,\lambda) = E_{n,s}[e_k e_{k+m}\,|\lambda] - g^2(\lambda) \tag{17}$$

The additive noise $n_\lambda(t)$ is independent for each t, and the data d_k, is assumed to be independent for different k. Since e_k depends on b_k, c_k, and c_{k+1} which in the presence of data asymmetry depends on d_{k-2}, d_{k-1}, d_k, and d_{k+1}. Similarly e_{k+m} depends on d_{k+m-2}, d_{k+m-1}, d_{k+m}, and d_{k+m+1}. In order that e_k and e_{k+m} are uncorrelated, it requires k+m-2 > k+1, or m > 3. In this case $R_0(m,\lambda)=0$. For $|m| > 3$. Then (15) becomes

$$S(\omega,\lambda) = \int_{-4T}^{4T} \langle R(t,\tau;\lambda)\rangle \cos\omega\tau\, d\tau \tag{18}$$

It is assumed that the symbol time-loop bandwidth product is much less than 1, i.e., $W_L T \ll 1$, practically it is sufficient to approximate $S(\omega, \lambda)$ at zero frequency. Therefore,

$$S(\omega,\lambda) \cong S(0,\lambda) = T\left[R_0(0,\lambda) + 2\sum_{m=1}^{3} R_0(m,\lambda)\right] \tag{19}$$

A normalized noise spectrum can be defined as

$$h(\lambda) \triangleq \frac{S(0,\lambda)}{S(0,0)\Big|_{\substack{R_s\to\infty,\,p=0.5,\,\ell=0\\ \eta=0}}} = \frac{S(0,\lambda)}{\frac{1}{4}K_2^2\xi_0 N_0}$$

$$= Q(0,\lambda) + 2\sum_{m=1}^{3} Q(m,\lambda) - \frac{28R_s}{\xi_0} g_n^2(\lambda) \tag{20}$$

where

$$Q(m,\lambda) \triangleq \frac{E_{n,s}[e_k e_{k+m}|\,\lambda]}{(K_2 A)^2 \dfrac{\xi_0}{4R_s}} \quad ; \quad m = 0,1,2,3 \tag{21}$$

The quantity $Q(m,\lambda)$ is to be evaluated numerically.

7. DTTL CLOCK JITTER

During the operation of the bit synchronizer, $|\lambda| \cong 0$, the probability that $|\lambda| < 1/2$ is close to unity. Under this condition, (9) is approximately Gaussian, and the clock jitter, defined as the standard deviation of λ, is given by

$$\sigma_\lambda = \left[\frac{W_{LO} T \xi_0 h(0)}{4 R_s g_n'(0)} \right]^{1/2} \tag{22}$$

where $g_n'(0)$ is the first derivative of $g_n(\lambda)$ at $\lambda = 0$.

8. DTTL CYCLE SLIPPING RATE

The cycle slipping rate for DTTL in the presence of thermal and asymmetric noise can be derived similarly as in [9]. Let

$$\rho \triangleq \frac{2g'(0)}{KS(0,0)} = \frac{[g'(0)]^2}{W_L S(0,0)} \tag{23}$$

where $W_L = Kg'(0)/2$ is the loop bandwidth of the DTTL. The normalized average slip rate $\overline{S}/W_{LO}$ is given by

$$\frac{\overline{S}}{W_{LO}} = \frac{1}{\gamma \int_0^{1/2} \exp[-\gamma \int_0^{\lambda} g_n(x)dx]d\lambda \int_0^{1/2} \exp[\gamma \int_0^{\lambda} g_n(x)dx]d\lambda} \tag{24}$$

where $\gamma = \rho/g_n'(0)$.

9. FREQUENCY ACQUISITION TIME FOR A SECOND ORDER LOOP

This section summarizes the expression for the frequency acquisiton time for a second order PLL in the absence of noise. The derivation is generalized from [10] to incorporate an odd function of phase detector characteristic.

The development assumes a second order PLL with an ideal integrating filter $F(s) = 1 + a/s$. The input is assumed to have a frequency error $\Delta\omega$. The linear closed loop transfer function is given by

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{25}$$

Then the frequency acquisition time T_f for a PLL having a phase detector characteristic $g(\phi)$ ($g(\phi)$ is assumed to be an odd funution) is given by

$$T_f = \frac{\pi\left(\frac{\Delta\omega}{\omega_n}\right)^2}{2\zeta\omega_n \int_{-\pi}^{\pi} g^2(\phi)\,d\phi} \tag{26}$$

For a designed circuit, ζ and ω_n are fixed to be the design values ζ_0 and ω_{n0}. Realizing that the period of $g(\lambda)$ of DTTL is 1, the effect of the data asymmetry and transition density on T_f can be found relative to the designed values by

$$\frac{T_f(\Delta,p_t)}{T_f(0,0.5)} = \frac{\int_0^{1/2} g^2(\lambda)\,d\lambda\Big|_{p_t=0.5,\,\eta=0}}{\int_0^{1/2} g^2(\lambda)\,d\lambda} \tag{27}$$

It can be shown that for the special case $\eta=0$, (27) is reduced to

$$\frac{T_f(0,p_t)}{T_f(0,0.5)} = \frac{1}{4p_t^2} = \frac{1}{[4p(1-p)]^2} \tag{28}$$

10. THE CSSL MODEL

The CSSL [1,11] is modeled in Fig. 4. It is an analog, narrowband, and nondata-aided synchronizer. For the purpose of performance comparison, numerical results of CSSL are provided. The detail system analysis can be found in [1]. Self noise, which is significant in narrowband and high signal-to-noise ratio, is also included in the results.

The prefilter H(s) is modeled as a low pass filter with 3 dB single-sided bandwidth f_0 Hz. The postfilter G(s) works as a zonal filter to pass the harmonic component to be tracked by the phase-locked loop. It can be neglected in the analysis. The relative timing error, normalized to a symbol period, is defined as

$$\lambda_n \triangleq \frac{\phi_n}{2n\pi} \tag{29}$$

where ϕ_n is the phase error of the nth harmonic sinusoid to be tracked by the PLL. The clock jitter σ_{λ_n} is defined as the standard deviation of λ_n. For NRZ signaling format, the first harmonic, n=1, is to be tracked, while for Manchesier format, n=2.

11. DTTL AND CSSL PERFORMANCE

The performance of the DTTL for the NRZ format in the presence of asymmetric noise is given. Of equal importance, numerical results for thermal noise are also provided. Other DTTL performance can be found in [3,4].

The clock jitter as a function of data asymmetry (via Δ) is shown in Fig. 5. We see that the data asymmetry degrades the performance as it effectively redues the signal-to-noise ratio. Figs. 6 and 7 plot the clock jitter versus the signal-to-(thermal) noise ratio for different values of a and *l*. The clock jitter in the presence of asymmetric noise is plotted in Fig. 8 as a function of transition density (via p). The degradation due to decrease of transition density is expected since the number of zero crossings (NRZ case) decreases. However, in the high R_s region, the clock jitter is insensitive to this parameter.

Fig. 9 shows the effect of data asymmetry on cycle slip rate with thermal noise only. Figs. 10 and 11 show the effect of asymmetric noise on cycle slip rate.

The relative frequency acquisition time T_f / T_{f0} in the absence of noise for DTTL, NRZ format is illustrated in Fig. 12. The time is relative to the case T_{f0} when $p = 0.5$ and $\Delta = 0$. For a fixed Δ, T_f increases as the transition density decreases. Since for the case of NRZ format, the number of zero crossings decreases as transition density decreases, which in turn will lengthen the frequency acquisition time. The data asymmetry causes an imperfect timing of the data pulses, which in turn decreases the magnitude of the first harmonic and gives rise of higher harmonics. The increase of frequency acquisition time in the presence of data asymmetry is expected.

Figs. 13 and 14 are CSSL clock jitter performance in the presence of asymmetric noise. They can be compared to Figs. 6 and 7. The window ξ_0 for DTTL can be decreased and optimized to yield better performance. The delay α is optimized for each signal format.

Finally, a comparison of the acquisition time in the absence of noise for DTTL and CSSL is given. The T_f of DTTL can be found by substituting $g(\phi) = \sin(\phi)$ in Eq. (26). The relative time is found to be

$$\frac{T_f(\text{DTTL})}{T_f(\text{CSSL})} = \frac{1}{6}$$

In other words, to within the approximations made the time required for DTTL to acquire is only about 1/6 of that for CSSL when frequency detuning is present.

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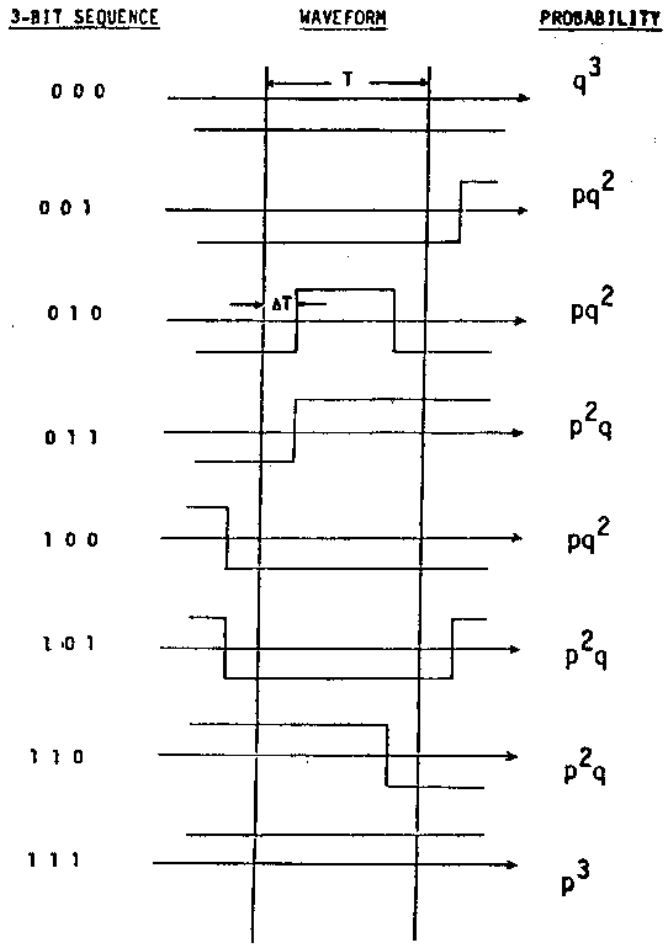

Figure 1. 3-Bit Data Pattern Showing the Effects of Data Asymmetry.

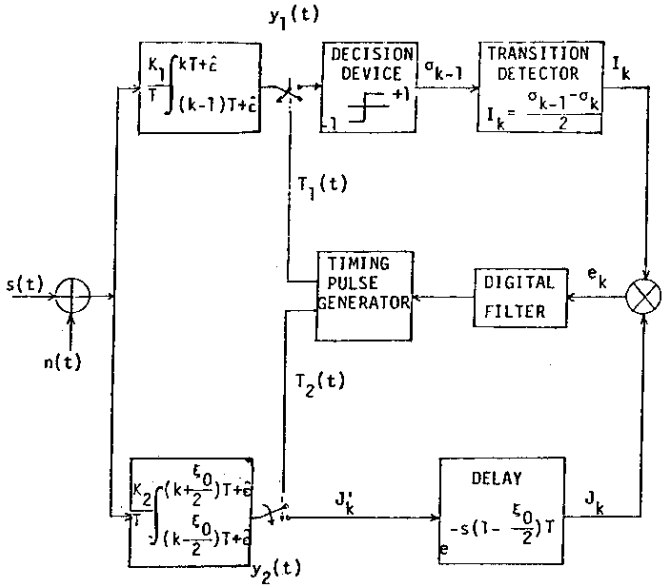

Figure 2. The Digital Data Transition Tracking Loop (DTTL).

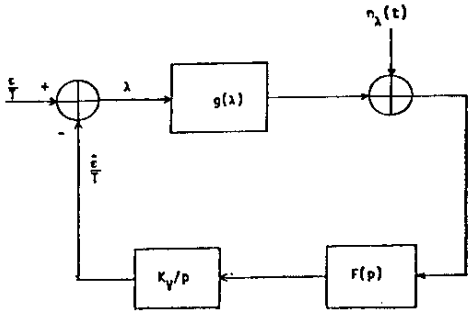

Figure 3. Equivalent Mathematical Model of DTTL in the Form of a PLL.

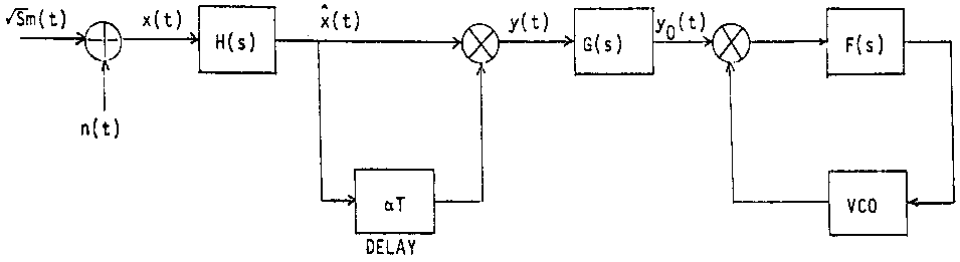

Figure 4. Cross-Spectrum Symbol Synchronizer.

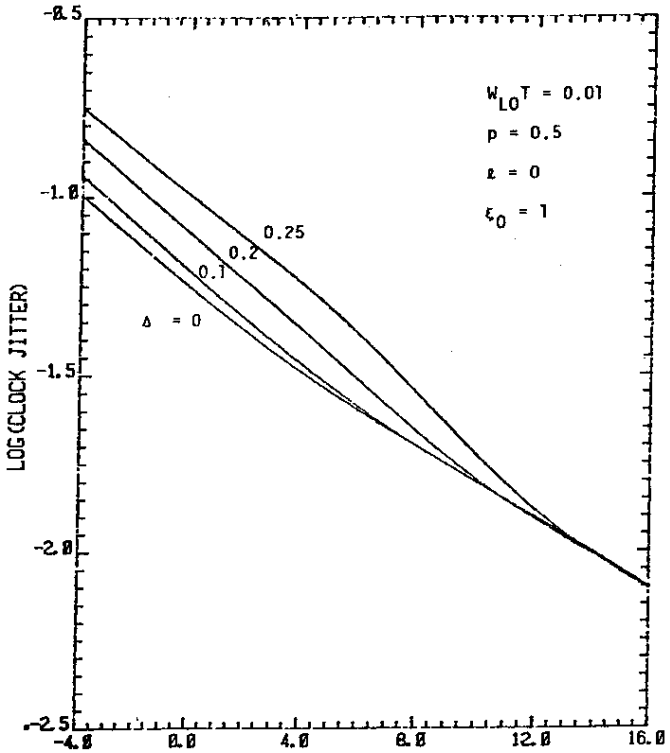

Figure 5. Clock Jitter for DTTL NRZ Format with Data Asymmetry, Thermal Noise Only.

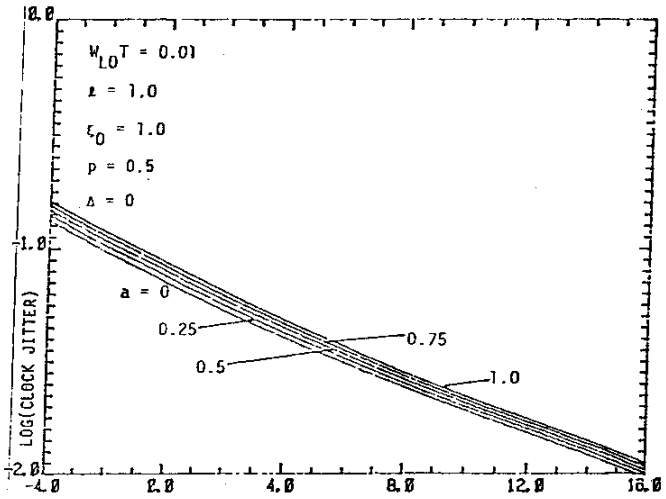

Figure 6. Clock Jitter for Various a, NRZ Format with Thermal and Asymmetric Noise.

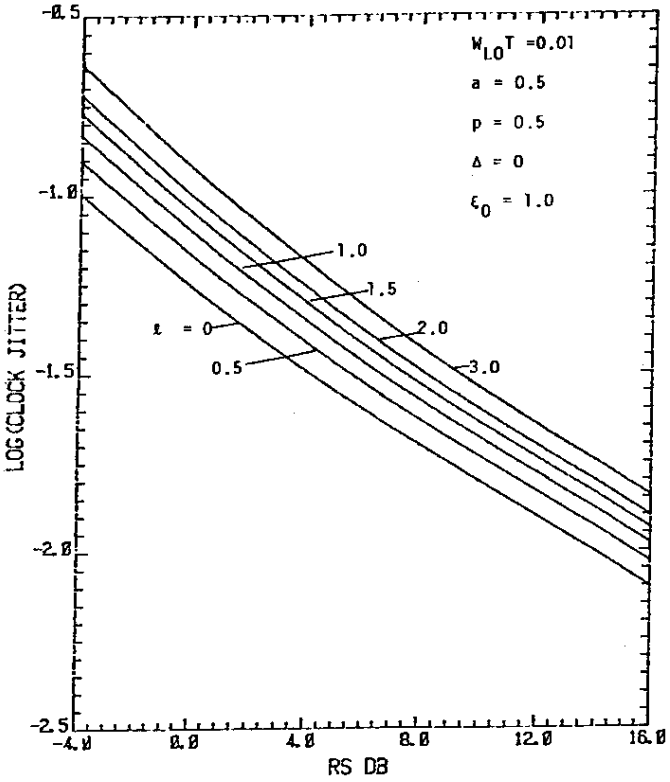

Figure 7. Clock Jitter for Various *l*, NRZ Format with Thermal and Asymmetric Noise.

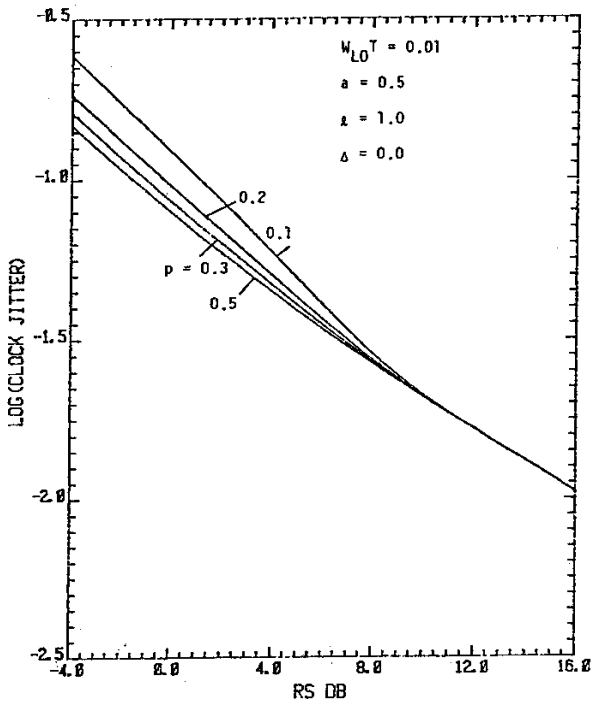

Figure 8. Clock Jitter for NRZ Format, Transition Density, Thermal and Asymmetric Noise

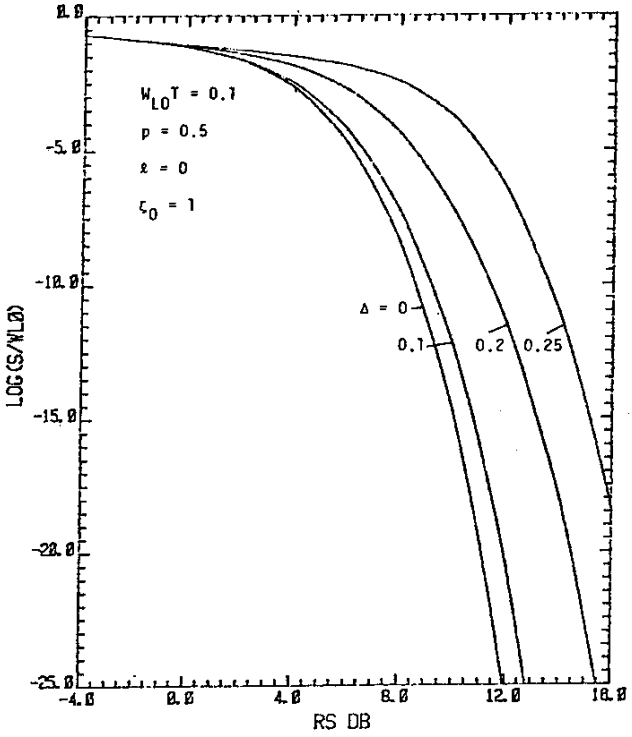

Figure 9. Normalized Slip Rate for DTTL with Data Asymmetry, NRZ Format, Thermal Noise Only.

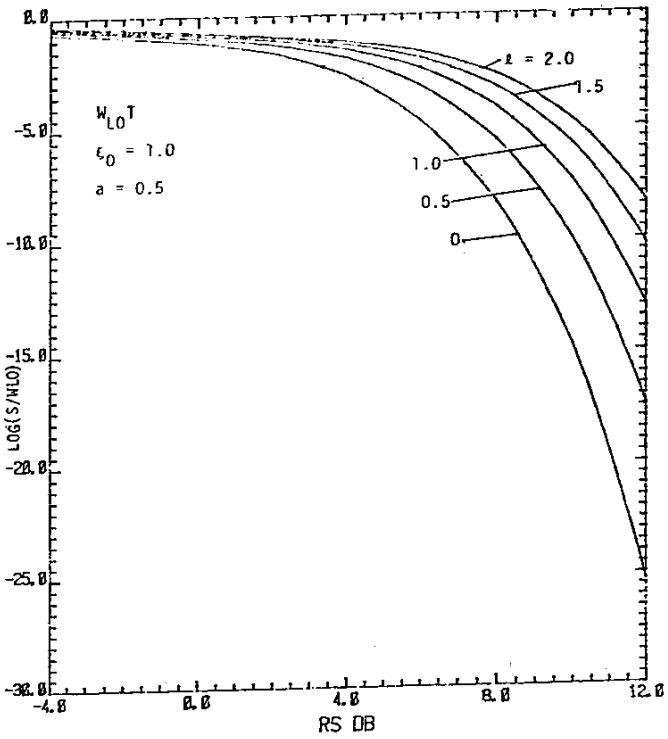

Figure 10. Normalized Slip Rate for DTTL, NRZ Format with Thermal and Asymmetric Noise.

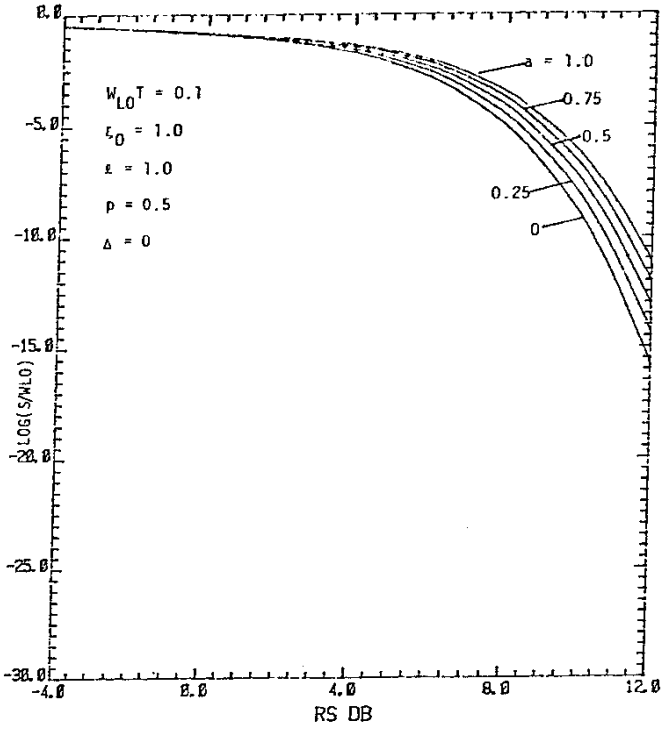

Figure 11. Normalized Slip Rate for Various a, NRZ Format with Thermal and Asymmetric Noise.

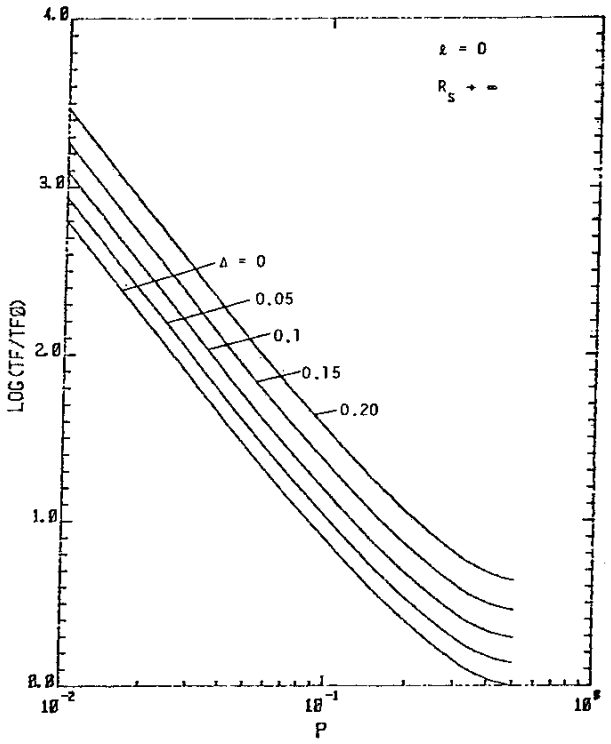

Figure 12. Relative Frequency Acquisition Time in the Absence of Noise for DTTL, NRZ Format.

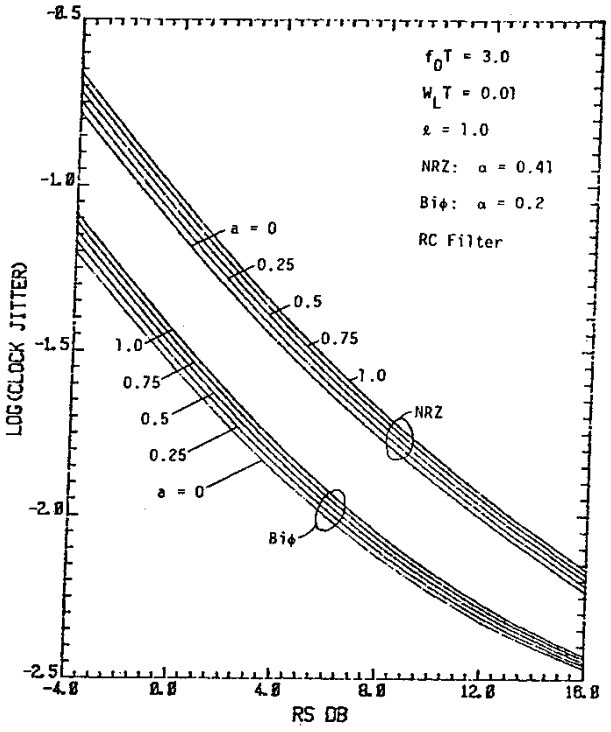

Figure 13. Clock Jitter vs. Signal-to-Noise Ratio for CSSL with a as a Parameter.

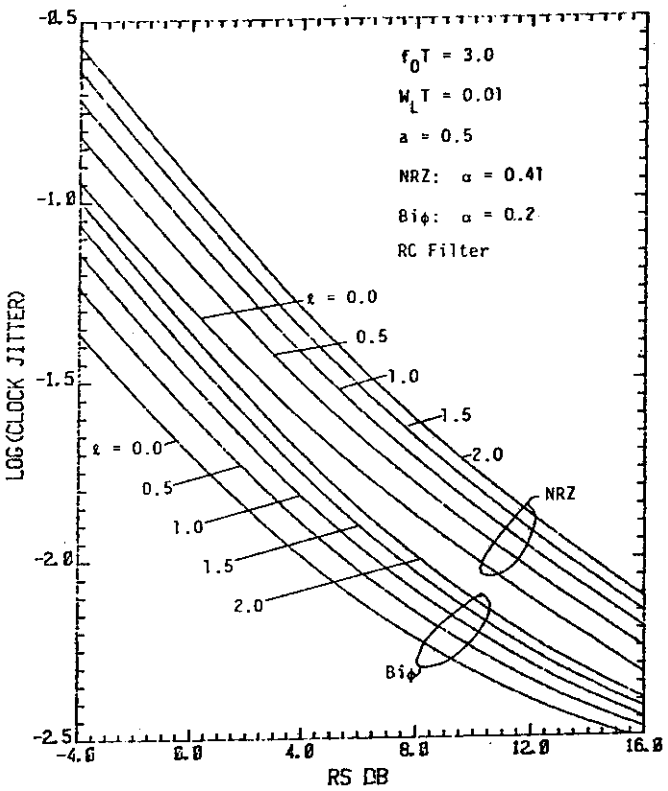

Figure 14. Clock jitter vs. Signal-to-Noise Ratio for CSSL with *l* as a Parameter