USE OF FORWARD ERROR CORRECTION IN A GROUND-TO-AIR-TO-GROUND TELEMETRY AND CONTROL LINKS

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1. Abstract

A forward error correcting (FEC) codec/interleaving system has been developed to improve the signal to noise ratio of a full duplex channel composed of a low rate command and control uplink and a high rate telemetry downlink. The system includes two MIL spec airborne 20 square inch cards and a ruggedized modified LINKABIT standard LV7017HS Convolutional Encoder Viterbi Decoder Ground Unit.

The coding parameters used are code rate 1/2, constraint length K=7, 8 levels of soft decision and data rates of up to 20 Kbps for the command link and up to 10 Mbps in the telemetry downlink.

Since Viterbi Decoders work best on memoryless Gaussian Noise channels, interleaving is used to randomize the effects of fading, jamming or other bursty types of noise making them appear like white Guassian additive noise to the decoder.

A coherent binary PSK modem will ideally provide 10^{-5} bit error rate (BER) with E_b/N_o = 9.6 dB (bit energy per noise ratio). The use of the FEC codecs in the sort decision mode achieves the same BER with 5 dB lower E_b/N_o, meaning either an increase of the communication range with the same RF equipment or substantial decrease of RF power or antenna size for the same communication range.

The same system could be used in a hard decision mode and still provide a gain of more than 3 dB at BER of 10^{-5}. The coding gain increases as the required BER decreases.

The described system could be easily adapted to any command and control link or telemetry link at the above mentioned data rates.

2. Introduction

In recent years the use of forward error correction coding to improve link performance has evolved from a theoretically possible but rarely used solution to a commonplace one for PSK modulated satellite channels. The success of such devices in this scenario has resulted in increased interest in F.E.C. for other channels, such as phone lines, FSK modulated channels, and other channels with non-Gaussian statistics. The needs of such an application are often best met by an integrated Viterbi codec/interleaver, in which the interleaving "randomizes" the noise so that the Viterbi decoder can provide maximum performance increase. This technique has often been used for PSK channels corrupted by burst noise, and is often the most cost-effective means to provide increased performance on other channels as well.

In this paper the use of F.E.C. with interleaving is discussed for air-to-ground/ground-to-air telemetry of control links. Uplink transmission or control data occurs at a relatively low data rate, 19.2 kbps, whereas downlink telemetry data is at a high rate, greater than two mbps. Downlink data may be corrupted by burst noise due to unintentional or intentional sources. The tradeoffs made in designing an F.E.C. system suited to this application are discussed, and some performance results are given.

3. Channel Characteristics

The system in which the error correction equipment is to be integrated is shown in figure 3-1. Low rate command data is transmitted on the uplink, with high data rate telemetry information on the downlink.

3.1. Uplink Coding

The uplink is a Gaussian memoryless channel, and as such requires little effort to find a good coding scheme for link improvement. There are two classes of codes to consider; block codes and convolutional codes. More literature exists on block codes, but high performance block decoders are difficult to build primarily because of the difficulty in making use of "sort decision" inputs to the decoders Soft decision input data may be thought of as the input symbol stream accompanied by some extra data giving the likelihood that the modem made the correct decision on the associated symbol. The likelihood may be extracted from the magnitude of the sample size, and is directly proportional to the log-likelihood function. Using just two such soft decision bits associated with each "hard decision" symbol output by the modem can improve decoder gain by 2 dB in the E_b/N_o required for a specific bit error rate. Soft decision block decoding algorithms have been considered, but they are very difficult to implement. Additionally, synchronizing a block decoder is a cumbersome task, since the number of sync states to search through is equal to the block length.

Convolutional decoders, especially those based on sequential or Viterbi decoding, lend themselves quite readily to soft decision decoding at the expense of only a minor increase in complexity. In addition, a rate n/m convolutional code has just m sync states to search, thus requiring a much less sophisticated synchronization machine than block decoders.

Given large amounts of power and space, no requirement for short throughput delay, and no need for a short synchronization acquisition time, a long constraint length sequential decoder would probably be the best solution, since such decoders are currently available off-the-shelf on a single board providing coding gains of up to 6 dB at BER 10^{-5} and data rates or 100's Kbps. The application here has a number of constraints; power and space must be minimized, and short throughput delay and acquisition time are both significant.

Sequential decoding is a powerful tool for use in systems where these parameters are not crucial because although it is a sub-optimal decoding technique, it allows the implementation of very long constraint length codes. Since the power of the code increases with the constraint length, such a technique can be made to outperform a maximum-likelihood (i.e. Viterbi) decoder operating at a shorter constraint length. In addition, sequential codecs have greater error correcting capability at low data rates where computational capacity is not exceeded. Unfortunately, the sequential algorithm does not lend itself to fast synchronization, and because it requires buffering of large amounts of data for computing, the decoder will insert a delay of thousands of bits. Powerful sequential decoding chips do exist, which allow reduction of the decoder to ten or so IC packages.

It is possible, however, to design a low data rate Viterbi decoder in as few as 35 or so IC chips in which decoder computations are done in a serial fashion. A rate 1/2 constraint length 7 decoder of this type can provide as much as 5.2 dB of coding gain (at 10^{-5} BER), which is only slightly less than the constraint length 36 sequential decoder currently on the market. In addition, the Viterbi algorithm lends itself to very fast synchronization; less than 500 bit times. It also exhibits a throughput delay of less than 40 bits, and can be designed for very low power consumption. As the data rate for this application is 19.2 kbps, such a decoder is an excellent solution.

3.2. Downlink Coding

The downlink from the aircraft to ground provides digital telemetry information at a rates or 2.5 Mbps and above. The link is corrupted by noise from two sources; AWGN at the receiver front end, and burst noise due to unintentional or intentional jammers, multiplath, fading, pops noise, etc. Exact burst statistics are not known, but the maximum burst length is estimated in this case to be as much as 100 code symbols.

Fewer tradeoffs are available for coding on this channel. Block codes are again rejected for the same reasons as in the uplink, although here there may be less weight given to arguments about synchronization, the reasons for which will become clear when interleaving is discussed below. Previous work has shown that for short length bursts, adequate burst protection may be achieved by the use of longer constraint length codes. The bursts encountered on this link are far too long for this to be a practical solution. The alternative approach is to use interleaving and deinterleaving to disperse the effects of the burst. To be effective, the interleaver size must be the product of the burst length and the decoder memory length. This rules out sequential decoding, since the decoder memory is very long, thus requiring a very large interleaver. High data rate Viterbi decoders or constraint length 7 are available off the shell with memory length of 32 information bits, with the added attraction that such decoders are easily integrated with the deinterleaver to quickly acquire deinterleave and decoder synchronization.

3.3. Interleaver Design

The function of the interleaver in the high data rate link is to provide a means to disperse or randomize the effects of burst errors. This is done by ‘shuffling’ the encoded data symbols prior to transmission and deshuffling them at the receiver prior to decoding. Since the noise is added to the shuffled symbol stream, deshuffling disperses the burst.

Most interleaver designs can be modelled as a buffer into which data is written according to some pattern of addresses and out of which data is read in some other pattern as shown in figure 3-2. Such an interleaver is called a convolutional interleaver, since the read and write process are occurring continually and there is no block structure to the resulting data. Good block interleaving structures also exist, but generally require twice the buffer size for the same performance as a convolutional interleaver, since the buffer must be filled entirely before it can be read out.

The most commonly used type of interleaver is the periodic convolutional interleaver. Such an interleaver writes data into its buffer using the address sequence

$$a_i = \mathrm{mod}_N 2_D \;\; i\,(ND+l)$$

where N is the decoder memory length and D is the smallest integer such that ND is greater than the burst length. The buffer size is then N^2D. The symbols are read out of the buffer with a sequential address. When this is done, for any two symbols within a group of N that are consecutive prior to interleaving (and hence within the memory of the decoder) there will be some integer multiple of ND symbols between them on the channel. Thus an error burst on the channel of ND symbols can only affect one symbol from any span of the decoder memory, and the decoder thus receives the appearance of random errors when the symbols are deinterleaved.

3.4. Interleaving With Intelligent Jamming

When the burst source is generated by a source specifically intended to obstruct transmission or existing in the area (radars for example), a periodic interleaver may not be the most effective means to combat the interference. The reason for this arises from the repetitive nature of the interleaver. If the jammer is able to jam every NDth symbol, for example, the deinterleaver will construct a burst of N bits to present to the decoder; exactly the phenomenon it is meant to prevent!

The most cost effective solution to this problem is often to use “random convolutional interleaving”. Here the interleaver still uses a sequential address to read from the buffer, but the write address is generated according to some pseudorandom pattern upon which only one requirement is placed; that each address can only occur once each M symbols, where M is the buffer size.

In this case, the interleaver/deinterleaver are no longer matches to a particular burst length, and many bursts will result in more than one affected bit being within the memory length of the decoder. This results in a small degradation in performance for the dumb jammer case, but in the case of the smart jammer, if the pattern is chosen carefully the only successful jammer strategy is one in which a very long burst is generated. If M is chosen to be large enough, this is usually impractical.

4. Airborne Equipment Design

The airborne equipment for this telemetry system consists of a high data rate integrated encoder/random convolutional interleaver and a low data rate soft decision Viterbi decoder. Both encoder and decoder use the same constraint length 7 rate 1/2 code. A wire-wrapped breadboard of both encoder/interleaver and decoder is shown in figure 4-1.

4.1. Encoder/Interleaver

The encoder/interleaver occupies one 20 square inch printed circuit board (PCB) and is implemented in standard LS ana S TTL. The encoder is easily implemented using a shift register and a read only memory (ROM) to compute the appropriate parity symbols. The interleaver consists of a RAM buffer with an address multiplexer which selects between a sequential address and one generated by a lookup table stored in ROM. Including circuitry for self test, the total IC count is less than 30 chips for an interleaver buffer size of 4K symbols. (See block diagram in figure 4-2.)

4.2. Soft Decision Viterbi Decoder

The decoder is built on a PCB of the same dimensions as the encoder. It uses a variety of LS TTL and CMOS logic, as well as a custom LSI IC for performing the add-compare-select trellis operation that must be executed 64 times per bit. The decoder accepts three bit quantized soft decision data; i.e. the demodulator provides the decoder with information about the quality or its samples as well as the samples themselves. This added information is easily extracted from the demodulator and provides 2 dB more coding gain than decoding with just the raw samples. (See block diagram in figure 4-3.)

Because the data rate of the decoder is low, the architecture can perform the 64 trellis computations required in serial fashion. This means that computations for each of the 64 states can be performed using the same logic provided an adequate memory organization is used to store results. This architecture results in an great savings in complexity over high data rate designs. The hardware makes extensive use of lookup ROMs to produce branch metrics and perform other functions needed for decoding.

The decoder is able to provide the system with a measurement of link quality. It does this by re-encoding the decoded data and comparing it to the received symbol stream. Since the bit error rate (BER) of the decoder output is at least two orders of magnitude better than the channel error rate (CER), most of the disagreements between re-encoded data and received data are caused by errors on the link. The result of this comparison is thus an accurate measurement of link quality, and can be used for a variety of applications, such as deciding to request retransmission.

Synchronizing the decoder requires the ability to properly pair up symbols associated with the same information bit input (symbols are in pairs because the code is rate 1/2). Obviously, there are two sync states to try. The decoder is able to reject incorrect sync states by observing the results of its internal computations. A synchronized decoder should perform at least one computation with a small result during each bit time; when all computations are yielding large results, the decoder tries the other sync state.

The circuitry required to perform all of these functions is implemented in about 40 ICs requiring less than 3 watts.

5. Ground Equipment Design

The ground equipment is considerably more complex than the airborne equipment, using far more parts and power. This is primarily due to the complexity of the high data rate Viterbi decoder, but is also due in some measure to the difficulty in implementing a fast synchronization strategy for the deinterleaver. The ground hardware is shown in figure 5-1.

The uplink portion of the ground equipment is a simple rate 1/2 convolutional encoder requiring four or five chips. The uplink is of almost no consequence in considering complexity in the ground equipment.

The deinterleaver hardware is almost identical to the interleaver logic except that the soft decision bits must be deinterleaver along with the received symbols, requiring a buffer that is 4Kx3 in size. The read and write addresses used for interleaving are exchanged for deinterleaving, but the sequences or addresses are identical.

Because there are 4K sync states in a random deinterleaver such as this, a fast sync search machine is needed. LINKABIT has developed a design capable of rejecting false states in as little as 50 bit times. Using this design, interleaver sync is typically acquired in a million bits or so with no special sequences or start of message patterns. The bits lost due to acquisition time are not critical for video, thus a sync time on the order of a half second are easily tolerated.

The decoder is based on an existing 10 Mbps Viterbi decoder design (LV7017 series). The decoder achieves its high data rate by performing trellis computations in parallel; all 64 trellis computations are performed in one clock cycle. Management of the path memory and decision output are also very difficult at this speed, but clever memory management makes it possible to implement the trellis computer and path memory on two PCB's. The entire ground FEC system requires only 3 cards in a ruggedized chassis 7"x8"x18".

6. Performance

The AWGN performance of the interleaved system is identical to that of the non-interleaved system. This is intuitively satisfying, since the interleaver is transparent to Gaussian noise. Measured performance results are plotted in figure 6-1. The curves show BER plotted against energy-per-bit to noise ratio (E_b/N_o) for three cases; an ideal PSK modem with no FEC, an ideal PSK modem with hard decision K=7 Rate 1/2 Viterbi decoding, and an ideal modem with soft decision decoding. At a BER of 10^{-5} the modem alone requires 9.6 dB, but with soft decision decoding, this figure is reduced by 5.1 dB. This allows the system to operate with an antenna reduced in area by a factor of three, or to reduce transmit power by a factor of 5.1 dB, or to operate at a much better BER.

The most commonly used type of interleaver is the periodic convolutional interleaver, used to combat arbitrary burst interference. Interleaved performance in the presence of a jammer is much more difficult to characterize. Many assumptions must be made about the jammer with regard to average and peak power, duty cycle and repetition rate. In addition, the effects of the jammer on the modem AGC must be considered, since the jammer can affect the accuracy of the soft decision information associated with unjammed bits, which further degrades performance.

Some data has been accumulated for the case where the link is jammed by a periodic interferer such as radar, where the burst length is relatively short (5 code symbols), but the repetition rates are high. In this scenario, the unjammed E_b/N_o is assumed to be about 11 dB; a very benign level. A plot of BER vs. jammer duty cycle is shown in figure 6-2.

7. Conclusions

The use of forward error correction is an effective means to improve Link quality for telemetry of control links. Small, low power decoders can easily provide 5 dB or more of link margin over the uncoded channel. Interleaving techniques make forward error correction a valuable tool for non-memoryless channels, and can be designed to provide increased perfromance even in the presence of intentional interference. The technology for such equipment is currently quite mature, with many types of equipment available off-the-shelf or easily modified for a particular application.

8. References

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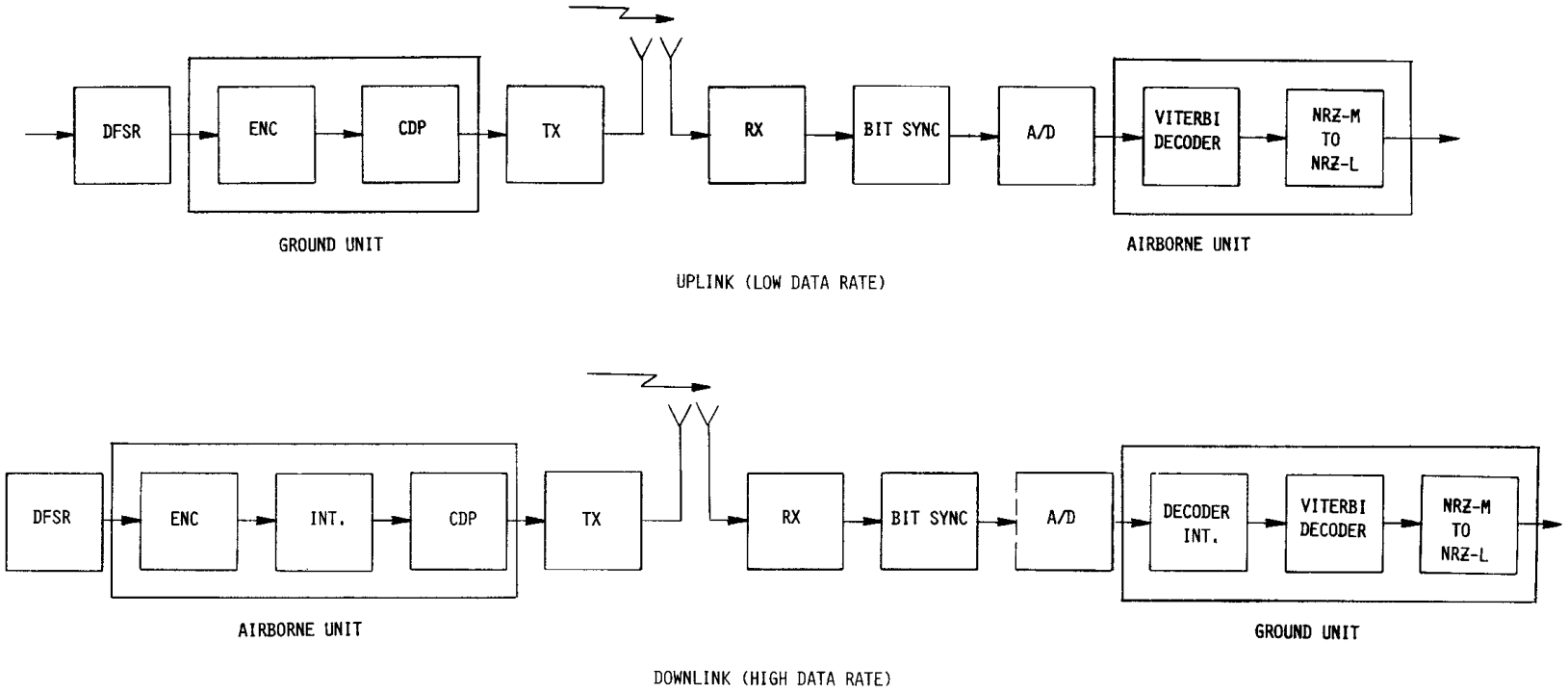

Figure 3-1. System Block Diagram

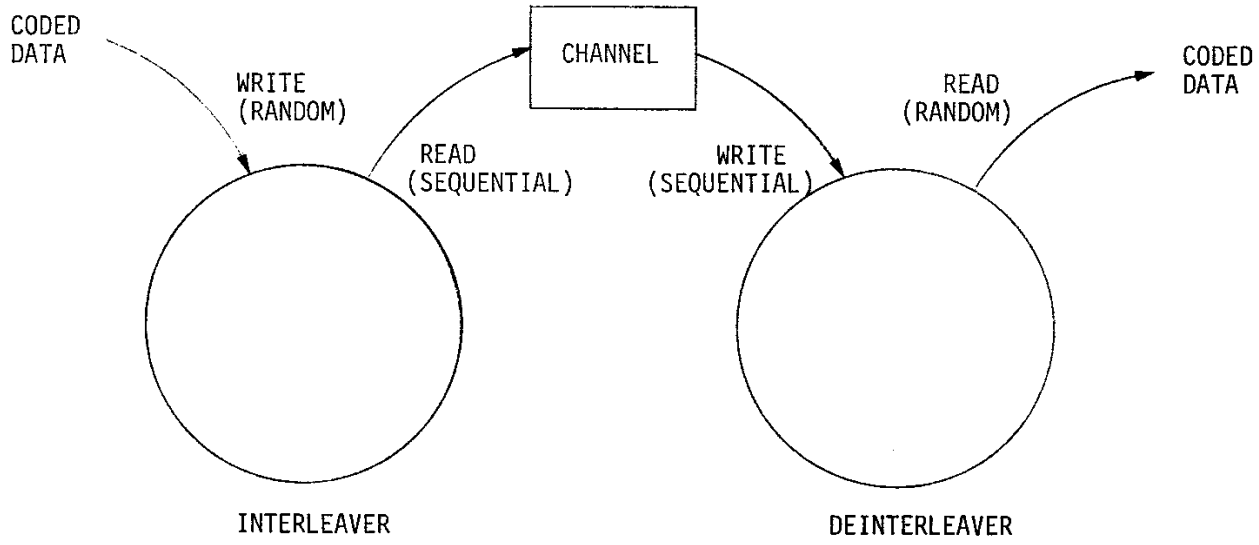

Figure 3-2. Interleaver/Deinterleaver

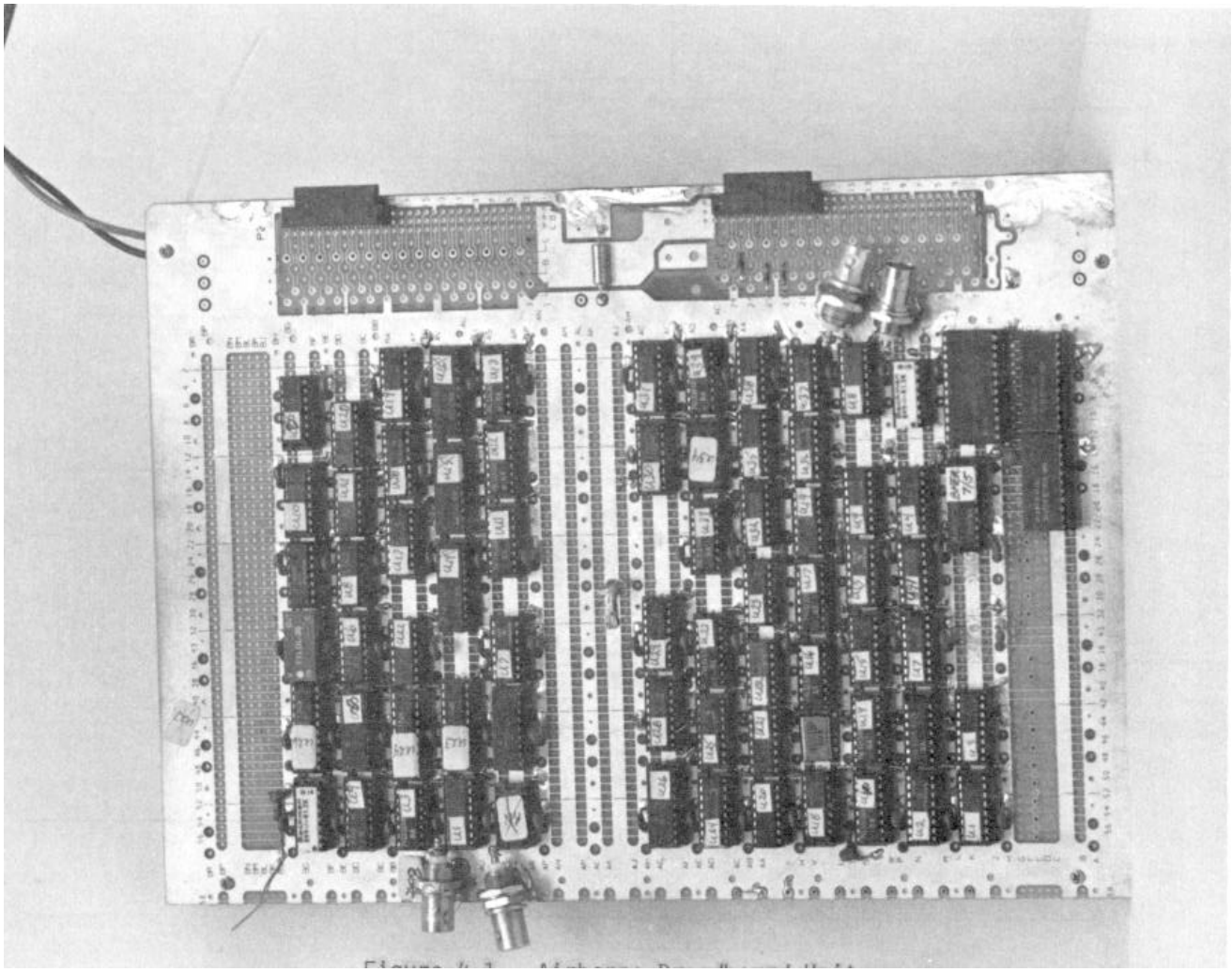

Figure 4-1. Airborne Breadboard Unit

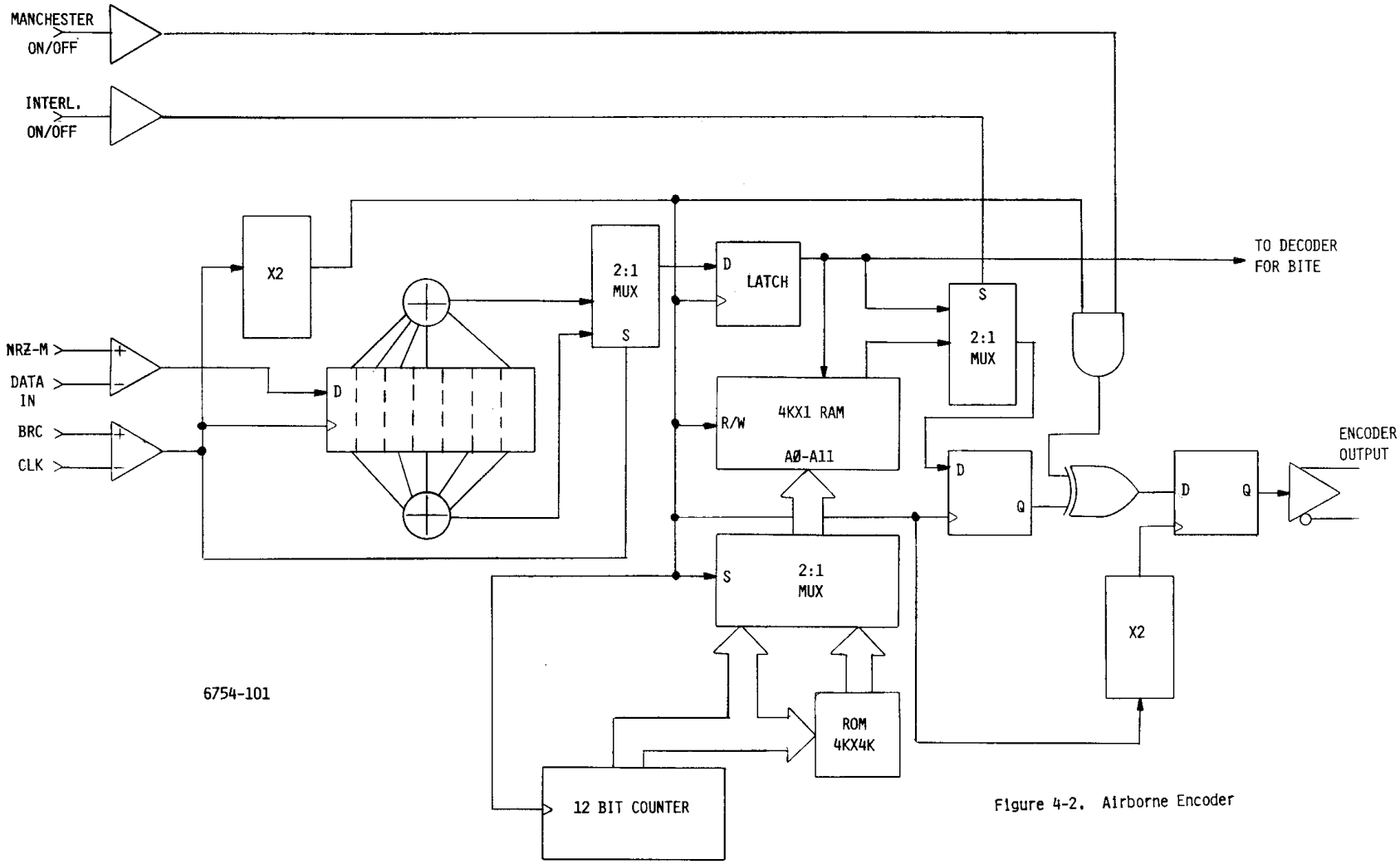

Figure 4-2. Airborne Encoder

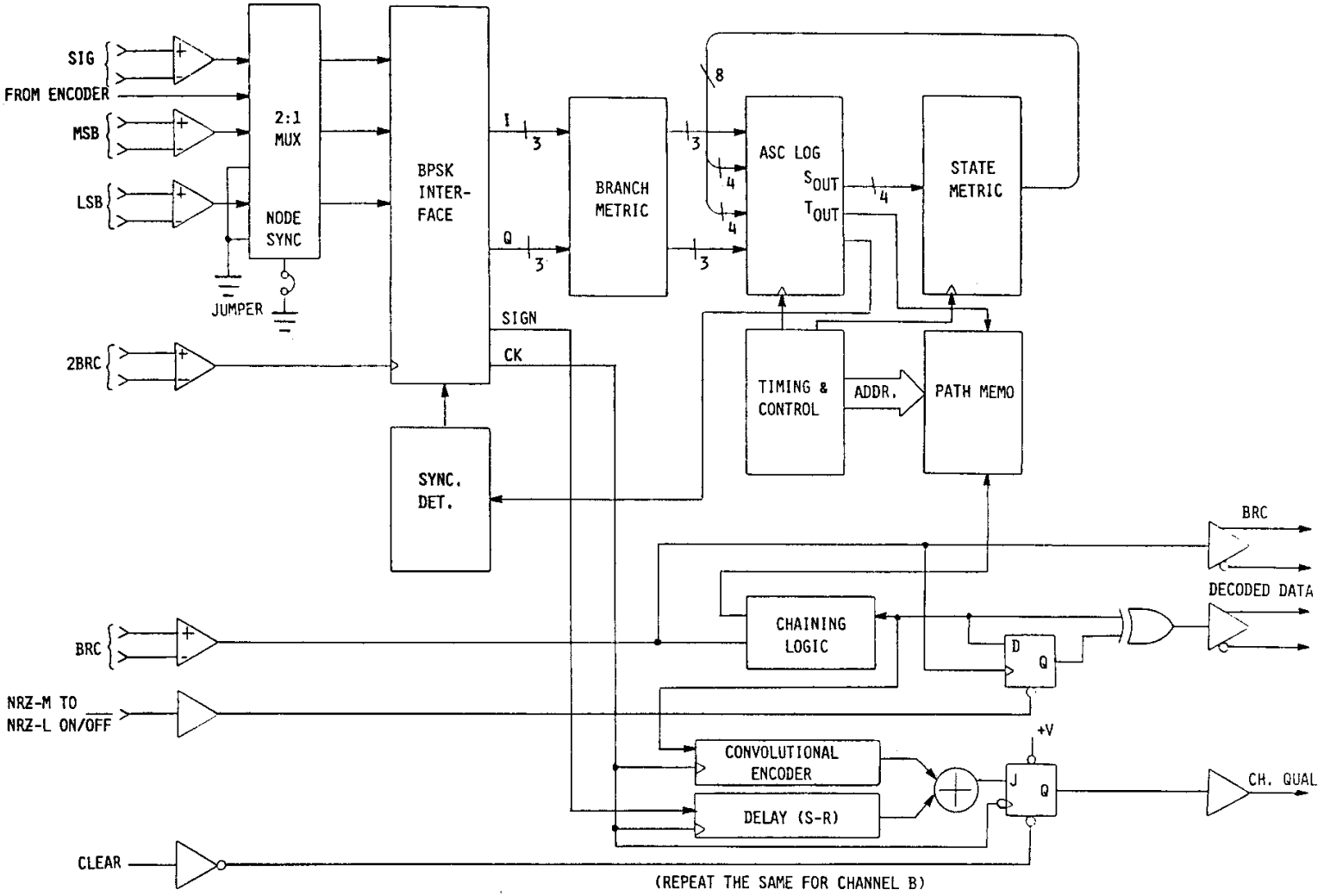

Figure 4-3. Airborne Decoder (Low Data Rate)

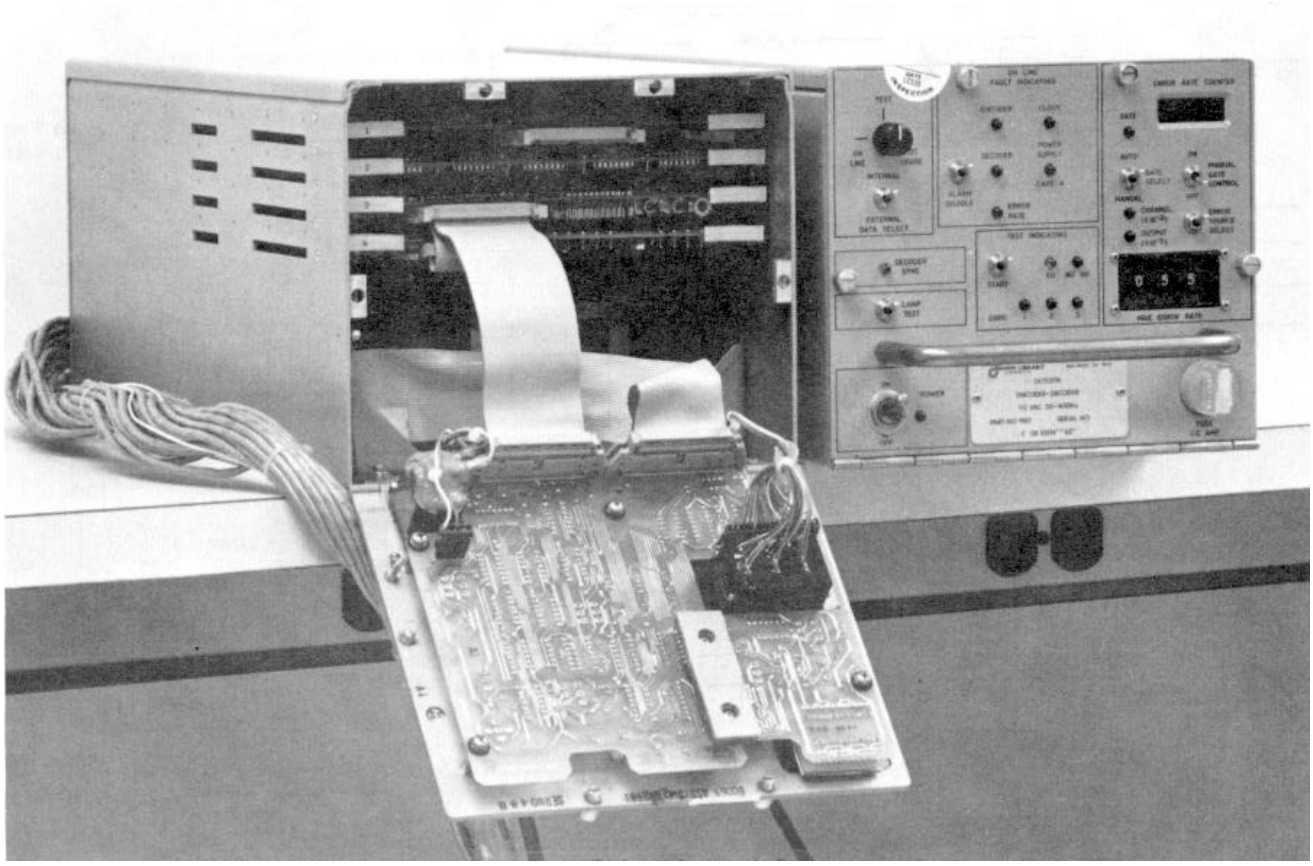

Figure 5-1. Ground Codec

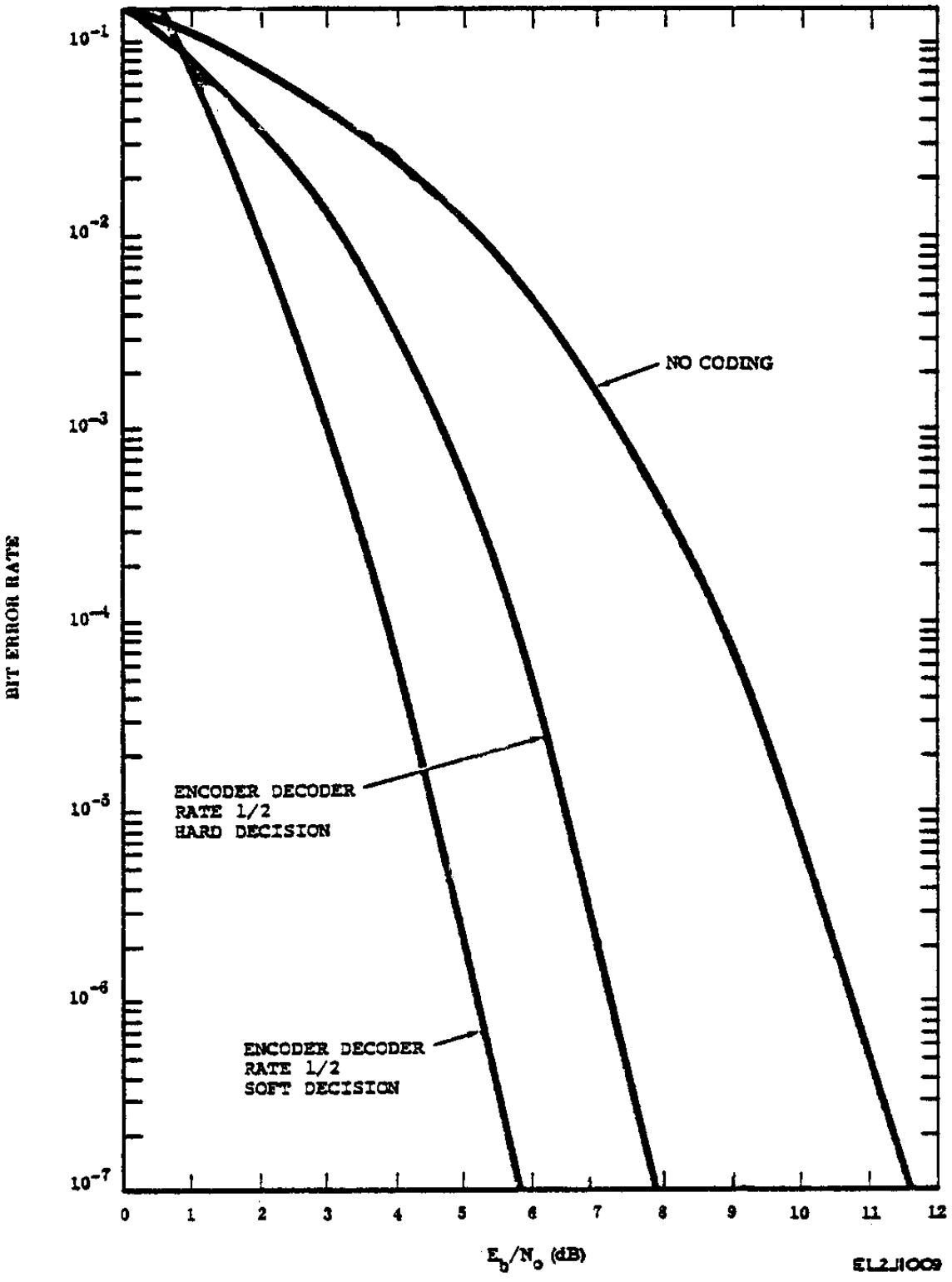

Figure 6-1. Measured PSK Modem Bit Error Rate Performance for Various Coding Configurations. No Differential Coding

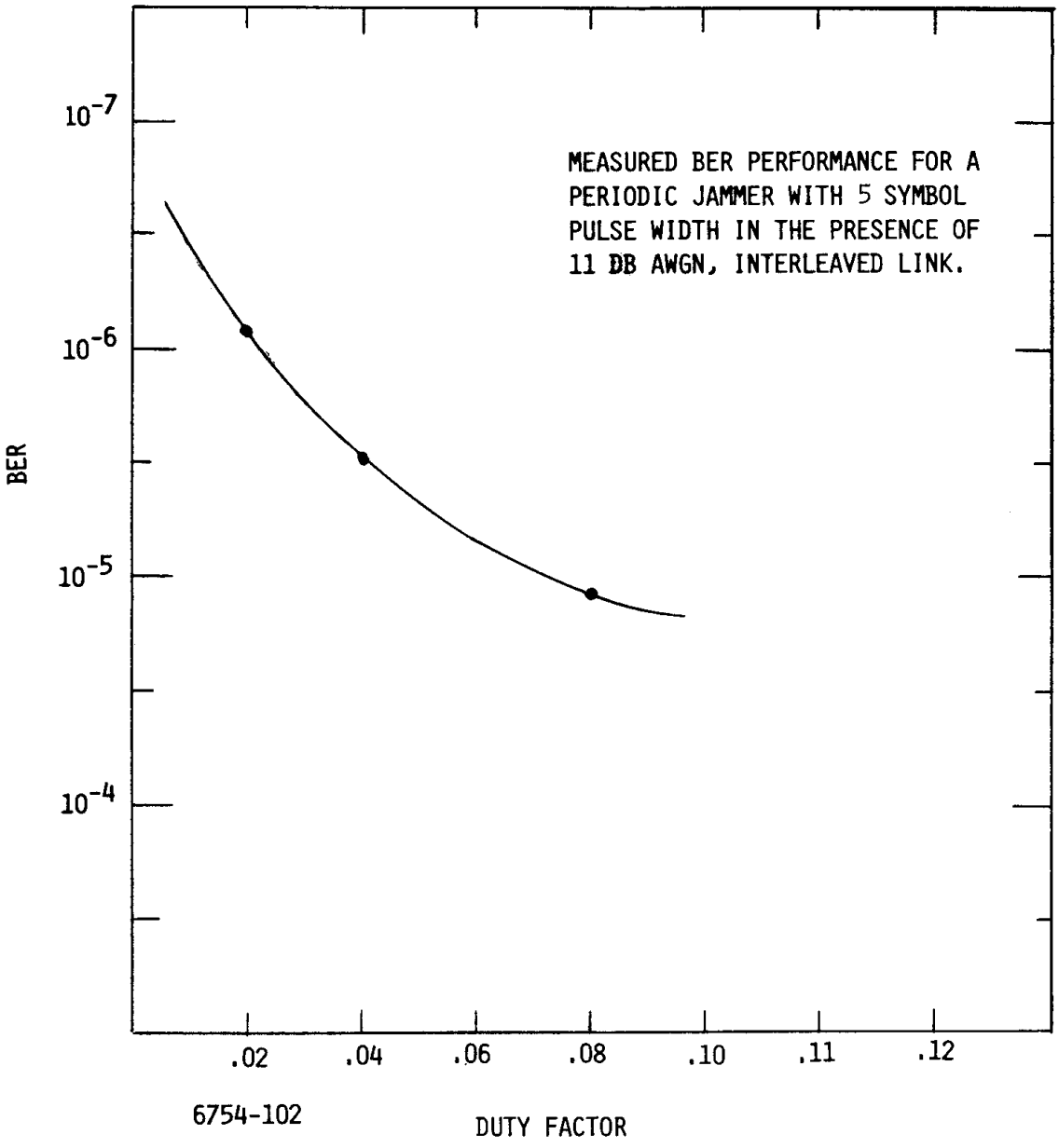

Figure 6-2. Measured BER Performance for a Periodic Jammer with 5 Symbol Pulse Width In the Presence of 11 dB AWGN, Interleaved Link