LOW-POWER FAULT-TOLERANT MICROPROCESSOR-BASED DISTRIBUTED ARCHITECTURE FOR ON-BOARD SIGNAL PROCESSING

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ABSTRACT

Numerous future space-based systems are being conceived that will require the on-board processing of a volume of data many orders of magnitude greater than the current state-of-the-art. Such systems must in addition be extremely low power and autonomously fault recoverable. This paper describes a microprocessor-based distributed architecture that has been evolving as a solution to this problem. This proposed architecture features three sub-architectures: synchronous pipeline, dedicated-channel microprocessor array, and multiple-bus oriented microcomputer array; as well as internal data compression, distributed control and self testing, and a building block approach to system implementation. Emphasized is the roll of microprocessors in this architecture and the challenge of reducing the overhead required by fault-tolerant processing.