APPLICATION OF A STATE-OF-THE-ART PROGRAMMABLE MULTIPLEXER IN A GUN LAUNCH ENVIRONMENT

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ABSTRACT

This paper will deal with the application of a fully programmable multiplexer in a gun launch environment. The multiplexer utilizes an electrically erasable memory to allow gain and offset scaling on a channel by channel basis and to control sampling sequence and subcommutation. Special emphasis will be given to the thick film hybrid construction technique utilized to withstand the harsh environment.

INTRODUCTION

When designing a telemetry system to be used in a gun launched projectile, the system engineer is presented with many restrictions due to the environment which will be encountered. The first major restriction is in the space available which is typically a cylinder 3.25 inches in diameter with an overall length of 4.5 inches. In this area provisions must be made for a transmitter, signal conditioning, a battery pack and, if multiple parameters are to be measured, some method of multiplexing data channels. To accomodate all of the above in the space allocated, it is essential to reduce the complexity of the circuitry and the power consumption to a minimum. In an effort to provide the most system performance in the space provided Microcom developed a Programmable Multiplexer which integrates the functions of the multiplexer and the signal conditioning circuits. The multiplexer also provides full format programmability. This paper will explain how the multiplexer functions, how its' construction is designed to withstand the environment and demonstrate that the fully programmable multiplexer is the most appropriate system for many applications.

CIRCUIT DESCRIPTION

The Programmable Multiplexer is an 8 Bit Pulse Code Modulator with full subframe/ supercommutation capability combined with a high speed programmable gain amplifier and offset generator all operating under the control of the central processor. The Bi-Phase Pulse Code Modulator format is the best for use in High-G application as it allows the use of a phase modulator transmitter which is far superior to a true FM transmitter in shock induced incidental modulation. The Bi-Phase Code also provides a clock transition in every bit period to allow better tracking of any shock induced shifts in bit rate. In the multiplexer, the raw data signals are connected directly to the input gates. The input gates are designed to sample the input signals with minimal loading effect from the telemeter. The gates also feature a proprietary signal blanker circuit to reduce crosstalk between channels with high source impedance. Since the gates are able to directly sample data accurately from high impedance sources and do not load the monitored system, external impedance buffering amplifiers are not required. When a signal is sampled, the gates complete the analog data path from the input to the programmable signal conditioning amplifier.

The programmable signal conditioning amplifier consists of four (4) major elements: The offset generator, offset amplifier, gain amplifier, and feedback network. The offset generator is a precision voltage source feeding a bank of precision attenuators which provide sixteen (16) voltages with a stability of greater than 20 parts per million. The offset generator also provides a means to select one of the sixteen voltages based on a four (4) bit control word from the processor section. The voltage selected is subtracted from the data signal in the offset amplifier which is a unity gain differential amplifier. The output of the offset amplifier is connected to the input of the programmable gain amplifier. The programmable gain amplifier, which is formed by the gain amplifier and the feedback network amplifies or attenuates the output of the offset amplifier into a +/-2.5 volt signal required by the analog to digital converter. The gain of the amplifier is determined by the ratio of the input resistor and the feedback resistor. By selecting the correct feedback resistor from the bank of resistors available, it is possible to get the required gain to have various levels of input signals result in full-scale output codes. The operation of these circuits is best demonstrated by analyzing the signal flow of a typical signal through the circuit. If a signal with an anticipated range of zero to six volts is to be telemetered the processor would command an offset of three volts from the offset generator when that channels input gate was activated. This voltage would be subtracted from the input voltage resulting in a signal out of the offset amplifier of +/- three volts. The processor would also select an appropriate feedback resistor to provide an attenuation of .833 which would result in an output from the programmable gain amplifier of +/-2.5 volts which represents full scale to the analog to digital converter.

The binary codes to control the gains and offsets are generated by the central processor which consists of the instruction decoder, program counters and EEPROM. The EEPROM (Electrically Erasable Programmable Read Only Memory) is used to store all the information on channels to be sampled, gains, offsets, and instructions. The electrically erasable prom is essential in a High-G application as the requirement for rigid mounting of all the components precludes the use of a UV erasable type memory which must be mounted in a socket to allow it to be reprogrammed. The electrically erasable prom is erased and re-programed by the application of appropriate electrical signals which may by applied with the prom still connected to the logic circuits of the multiplexer. The electrical access is provided through a separate 25 pin connector on the multiplexer. The instruction decoder monitors the data from the EPROM and decodes the instruction which cause the processor to perform a special task such as output the frame synchronization word or alter the sequence of channels to be sampled by executed a jump to subframe program. The logic controls which location in memory is to be read and determines what action is to be taken by the PCM system if an instruction is inserted in the memory.

Upon initial application of power, the program counter is set to zero and causes the first word to be read from memory. The instruction decoder examines the first word to see if it is an instruction. If an instruction is not detected, the 16 bits of information that comprise the first word of memory are sent to the gates and to the programmable signal conditioning amplifier. The most significant 8 bits will activate one of the input gates, thus selecting which data input is to be sampled. The remaining 8 bits are used to select the correct offset from the offset selecter, and the correct gain for the data to be sampled. On the next cycle of the clock the program counter is incremented, and the process repeats itself.

When the memory contains an instruction, the instruction decoder determines if it is a program counter reset, a sub-frame instruction, or a sub-frame pointer reset. If the instruction is a sub-frame instruction, the logic executes a jump to the location specified by the sub-frame pointer and reads the data from that location. This data is used to fetch and process the next data sample. After the data is read, the sub-frame pointer is decremented from its starting value of 11111111_2 to prepare it for reading the next sub-frame word. The system control then reverts back to the program counter.

If the instruction is a main frame or sub-frame reset, the logic resets the appropriate counter to its initial value, and the sequence repeats itself. When the instruction decoder recognizes the sync instruction, a 24 bit barker code is inserted into the PCM bit stream.

SYSTEM DESIGN

To fully appreciate the advantages of the programmable multiplexer approach, it is necessary to first analyze the standard approach with separate signal conditioning and a standard fixed format PCM system. The following is a typical measurement list for a modern guided projectile.

AUTOPILOT SIGNALS

Measurement	Level	Sample Rate (SPS)
+15 Battery	15Vdc	20
+5 Battery	5VdC	20
X+Y Cannard Orders	1Vdc	2 x 20
X+Y Axis Accel.	35mV	2 x 20
A/P Cage Int. Out	5Vdc	400
Gyro Precession	1.5Vdc	800
Gyro Spin 1, 2	1Vdc	400
Gyro Coil 1, 2, 3, 4	2.5Vdc	100

Fuze Signals

Measurement	Level	Sample Rate (SPS)
Rotor 1 Unlock	5Vdc	5
Rotor 2 Unlock	5Vdc	5
S + A Arm	.5Vdc	5
Detonator Fire	5Vdc	40
Elect. Arm Sig.	60mV	5
Temp 1, 2, 3, 4	20mV	4 x 5

Seeker Signals

X Error Sig.	1Vdc	20
Y Error Sig	1Vdc	20
Demod X Pos	1Vdc	20
Demod Y Pos	1Vdc	20
X Pos Rate	2.5Vdc	40
Y Pos Rate	2.5Vdc	40
Cos 0 Rate	2.5Vdc	40
Sin 0 Rate	2.5Vdc	40
X Pres. Ord.	5Vdc	20
Y Pres. Ord.	5Vdc	20
Flight Status	10Vdc	20
Flight Ctrl	10Vdc	20

From the above list, the sampling rates may be summrized as follows.

1 Signal	@	800	SPS
3 Signals	@	400	SPS
5 Signals	@	40	SPS
17 Signals	@	20	SPS
13 Signals	@	5	SPS

In attempting to format the above data using a conventional multiplexer having only supercom or crosstrapping capability, the system designer is restricted in the available data rates by the requirements for even spacing dictated by sampling theory and by the restriction that supercom groups be separated by at least three words to allow the insertion of a standard three word Barker sync pattern. This results in a maximum of a group of 12 channels crosstrapped in a forty-eight (48) channel multiplexer therefore to accomodate the 800 SPS channel the basic frame rate must be 66.6 frames/sec. From the basic frame rate, the following format can be obtained.

1 x 12 Supercom		12 Channels
3 x 6 Supercom		18 Channels
35 Single		35 Channels
3 Sync.		5 Channels
	Total	70 Channels

Therefore, a seventy two (72) channel multiplexer is required with a sample rate of 72 x 66.6 or 4795.2k words/sec. If the same measurement list is formatted on the programmable multiplexer and its subframe capability is employed, the format can be optimized to match the data more closely. The initial steps are the same and the basic sample rate is the same but in this format the 5 sample per seconds data channels are placed in two nine channel subframes and the twenty (20) SPS channels are placed in six three channel subframes. When channels are placed in a subframe, the processor causes the multiplexer to sample a different data point on each cycle of the mainframe effectively time sharing one of the mainframe data channels among a group of low frequency data channels. The processor also inserts a subframe counter in the mainframe for subframe synchronization. The resulting format is:

1 x 12 Supercom		12 Channels
3 x 6 Supercom		18 Channels
3 Sync.		3 Channels
8 Subcom		8 Channels
1 Subframe Sync.		1 Channel
	Total	42 Channels

6 - 3 Channel Subframe providing 18 22.2 SPS Channels
2 - 9 Channel Subframes providing 17 7.4 SPS Channels

By utilizing the subcome feature, the frame size is reduced to 48 channels with a corresponding decrease in the sample rate to 48 x 66.6 or 3.196 ksps or a 33% saving in bandwidth. The programmable multiplexer was also able to eliminate 23 signal conditioning circuits including differential amplifiers and gain stages. This results in a two-fold savings since the amplifiers are eliminated and the supply current is also significantly reduced. The programmable multiplexer also has benefits after the system design is complete and the system is in use. Because of the uncertain nature of many of the parameters measured and the difficulty in precisely predicting the performance of the projectile during and after the launch environment it is necessary to allow for large variations in the measurements from anticipated nominal ranges. This extended range degrades the accuracy of the measurement if the parameter falls in the normal range since the accuracy of the measurement is a percentage of the full dynamic range. When this occurs, it is a simple matter to re-program the multiplexer to modify the gains and or offsets to match the data actually measured on the first shot to provide better accuracy on subsequent shots. The programmable multiplexer also serves as an excellent diagnostic tool in evaluating anomalous behavior in the projectile. When it is discovered or suspected that a section is malfunctioning the multiplexer may be reprogrammed to increase resolution or sampling rate on the suspected area. The supply voltage could also be monitored for possible fluctuations as either a cause or an effect of the malfunction.

CONSTRUCTION TECHNIQUE

From the above you can see that the progrannable multiplexer provides a powerful system but to be useful in a High-G environment, the device must be small, reliable and rugged. All of these requirements are satisfied by its thick film hybrid construction. The electronics of the multiplexer are fabricated on 18 1" x 1" ceramic substrates. In the first step of processing resistive and conductive patterns are printed on the substrates using inks which consist of microscopic particles of metal mixed with fine glass particles. The substrates are then placed in a high temperature (1700 F) furnace which fuzes the glass around the metal and creates highly stable resistors interconnected by conductive land areas. The resistors are then precisely trimmed to value by removing a small portion of the resistive material which cause an increase in resistance. The next step in the fabrication process involves the manufacture of the active devices which are to be installed on the substrate. The semiconductor chips are placed in a ceramic carrier called a “LID” or Leadless Inverted Device. The LID carrier is in the shape of a U with the interior surfaces gold plated. The active devices are eutectically bonded to the bottom surface and the I/O connections of the device are wire bonded to steps on the outer edge as shown in Figure 1. The interior of the U is then encapsulated with a glass filled epoxy to protect the chip and bond wires from the acceleration of the launch environment. The completed device is then tested and installed on the substrate by reflow soldering. In the reflow soldering process a paste solder is screen printed on the attach points between the LID device and the substrate. The devices are then placed on the solder. When all the devices are installed the entire substrate is heated above the melting point of the solder. As the solder melts capillary action aligns the bottom of the LID device with the conductor areas of the substrate and a joint is formed. The reflow process may also be used to replace defective devices. Figure 2 shows a completed substrate mounted in a module housing. The LID devices appear as rectangles with lot codes printed on the top surface. The thick film resistors can be seen as black squares on the bottom of the left substrate. This construction technique is used for all devices with the exception of the memory. The memory device is not available in chip form and must be purchased in a standard 24 pin ceramic dip package. Testing performed at the Army Armament Research and Development Command, Dover, N.J. (ARRADCOM) showed that the device as purchased would not withstand the shock, therefore it was necessary to harden the device. The approach which proved most effective involved removing the brazed on cover of the ceramic dip package and potting the internal cavity of the package with epoxy. The devices were then temperature cycled to prove thermal comparability between the epoxy and the device and then shocked in the air gun facility at ARRADOM to prove that they could withstand the shock. After successfully withstanding the shock test, the devices then have their leads removed and they are reflow soldered onto ceramic substrates. In the final assembly step the substrates are epoxied into modular aluminum housings. The complete unit unfolded for test purpose is shown in Figure 3. Figure 4 shows how the unit is folded into its final configuration. Each housing will hold two substrates and is designed with interlocking tongue and grove construction to increase the structural integrity of the completed assembly. This is extremely important as the substrates can withstand great forces but are extremely brittle which will result in fractures if torsional flexing is allowed to develop across the substrate. The final protection against the shock is foaming each module with an isocynate foam. The completed unit which measures 2" x 1.86" is shown in Figure 5.

QUALIFICATION TESTING

Prior to acceptance for actual use the design was verified by test firings in the rail gun at ARRADCM in Dover, NJ. The rail gun is a standard 155mm artillery piece with an arragement of steel rails around the exit end of the barrel designed to capture the exiting projectile and direct it into a water trough for a soft recovery. For the test firings the multiplexer was placed in a test projectile along with a transmitter which was previously qualified for gun launch use. The rail gun was equipped with the necessary receiving equipment for both inbore and free-flight reception. The unit was then fired with standard charges resulting in 15kG peak acceleration with the multiplexer mounted to receive the shock in each of the three perpendicular axis. In reviewing the data there was no degradation of data in any of the shots and the unit functioned successfully after being removed from the shell. After qualification, the system containing the multiplexer as successfully used for further evaluation and testing of the XM785 projectile both in the rail gun and on the actual firing range. The successful completion of this program proves that a properly designed programmable multiplexer will withstand the gun launch environment and provide accurate reliable data for test and evaluation of sophisticated munitions. It also gives the user complete freedom to modify his data requirements at any time in the evaluation program without costly design changes.

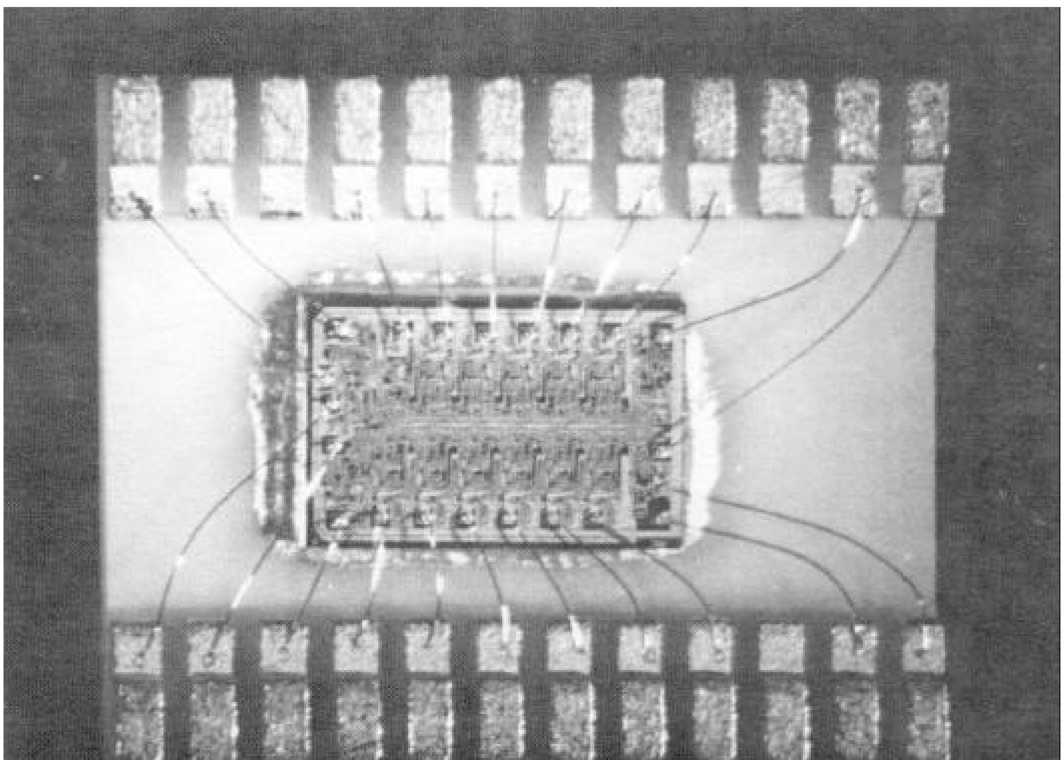

FIGURE 1

LID DEVICE BEFORE EPOXY COATING

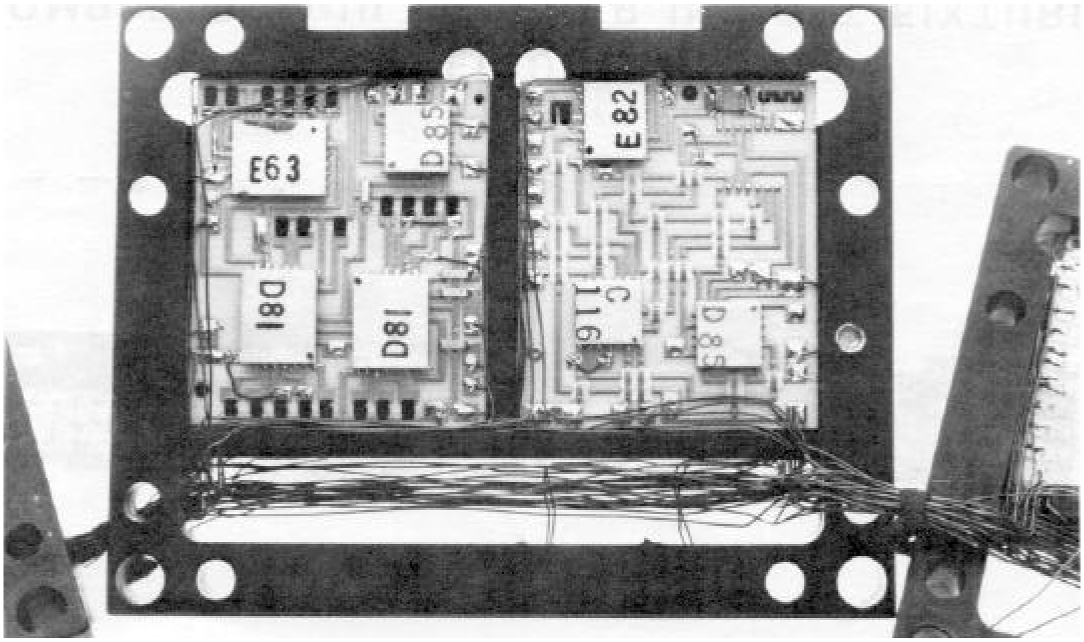

FIGURE 2
THICK FILM SUBSTRATE IN HOUSING

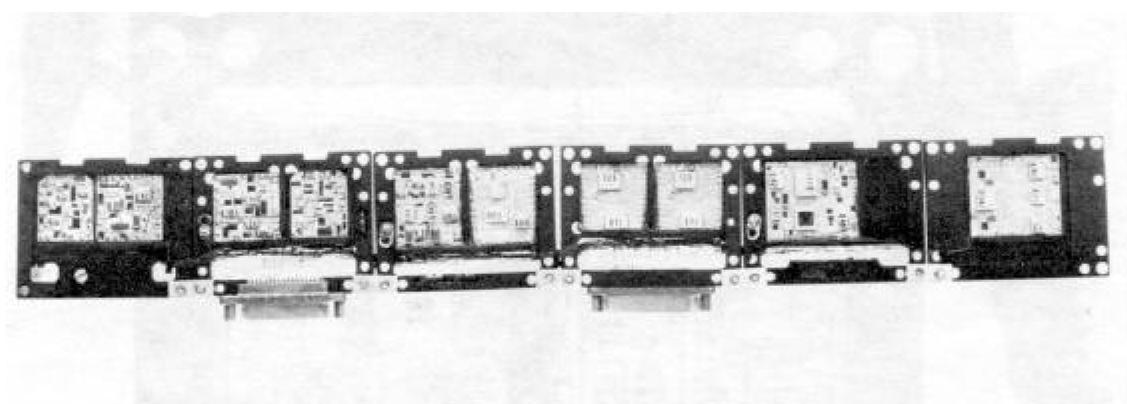

FIGURE 3
COMPLETED MULTIPLEXER IN TEST FIXTURE

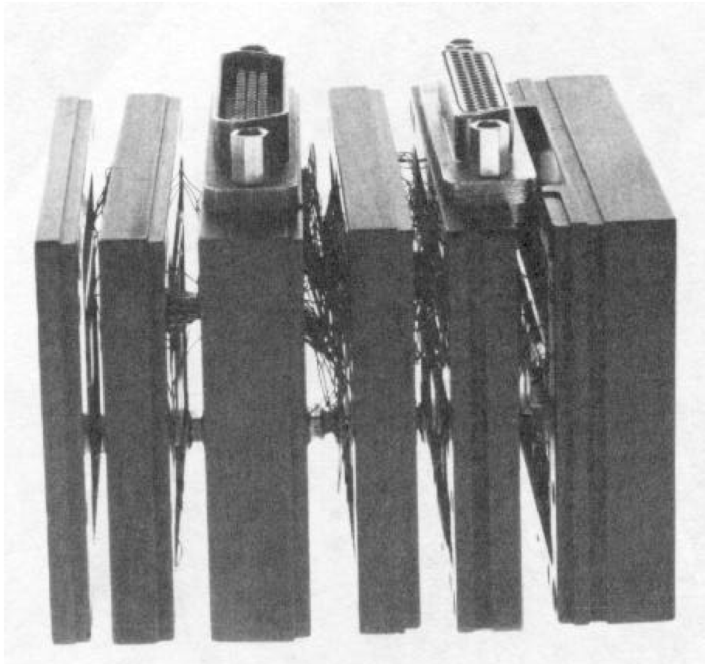

FIGURE 4
UNIT FOLDED INTO FINAL PACKAGE

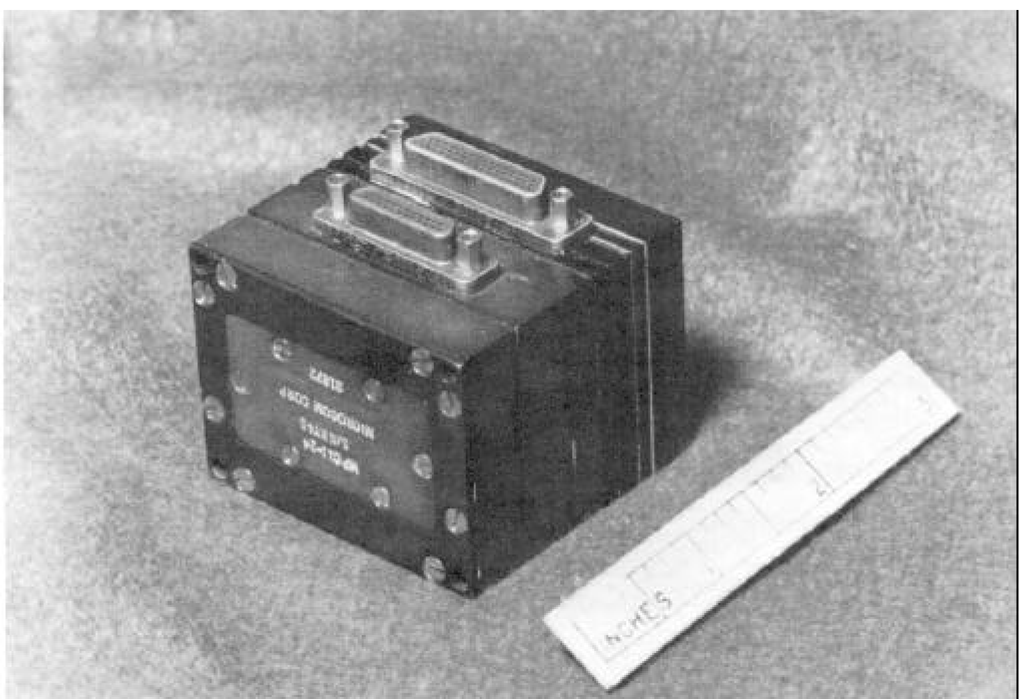

FIGURE 5
MULTIPLEXER MPC-11-24