AUTOMATIC GAIN RANGING AMPLIFIER

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ABSTRACT

The increasing complexity of Air Force aircraft and systems has created a demand for the collection of greater amounts of more accurate, higher dynamic range test data to solve dynamics related problems. The problems presented by higher volume can be resolved by making use of a time sharing Pulse Coded Modulation formatting technique. To meet demands for high dynamic range, the need is apparent for a device which "siphons" the wide dynamic range test data to a range which is compatible with the recording device. The Automatic Gain Ranging Amplifier performs this task and that of increasing the system's signal to noise ratio.

The AGRA has seven gain options from -12 dB to 60 dB (-12 dB is a one step 12 dB attenuation) in 12 dB steps. Gain is controlled by an internal peak detector or by an external (CMOS compatible) processor. Following the amplifier is a four rolloff frequency, six pole Butterworth low pass filter.

The AGRA senses the output measurement and automatically adjusts the gain to be within the required recording levels. In this manner, a large number of measurement devices (thermocouples, strain gauges, etc.) whose output swings vary over a large range can be made compatible with a single recording device.

INTRODUCTION

In the evaluation of new airborne systems, the AFWAL-FBIG attempts to collect and record as much data as possible for every hour of airborne testing so as to minimize the number of costly test flights. In doing so, a large quantity and variety of measurement devices must be used on each flight. It is desirable to reproduce the outputs of these transducers on a single recording channel. Since each type of sensor will have a unique output voltage range, the measurement system must have at least a 100 dB dynamic range. Because there is no recording equipment which can meet this requirement, the need for a

device which expands the dynamic range from the conventional 70 dB to 120 dB (as can be seen in Figure 1), becomes apparent.

This paper will describe the block diagram and the actual results measured on the AGRA prototype.

It is not our intent here to reveal design criteria of the detailed schematics of the AGRA.

1.0 BLOCK DIAGRAM

The AGRA block diagram appears in Figure 2.

1.1 Amplifier Section

As a single unit, the amplifier has a gain which can range from -12 dB to +60 dB in steps of 12 dB. These characteristics are described by two amplifying stages which are each comprised of wide-band instrumentation amplifiers, precision thin-film resistor networks, and a switching network. The first stage has a gain range of 1 to 200, while the second stage has a gain of 0.25 to 5.12. The aggregate gain range is 0.25 to 1024.

The amplifier's front end has differential inputs, high input impedance (10 Mohm in parallel with 60 pf) and DC/AC (2 Hz) coupling selections. In the AC mode, application of a negative DC feedback eliminates high output offset voltage.

1.2 Filter Section

The filter has four rolloff frequency options at 500 Hz, 2 kHz, 5 kHz and 20 kHz respectively. In-band frequency response is kept maximally flat with a six pole Butterworth configuration. The filter is realized as an active Voltage Controlled Voltage Source.

Selection among the four rolloff frequencies is accomplished by the application of two digital inputs. The filter output is buffered, with current limited at 25 mA, and it can drive an external current booster.

1.3 Peak Detector and Automatic Gain Ranging

The peak detector and auto gain ranging circuitry (as can be seen in Figure 3) controls the AGRA's gain so that output values fall within two preset thresholds. (This condition only holds true during internal auto gain ranging selection). The network can be operated in three different modes:

i) External - Gain is controlled by an external (CMOS Compatible) processor.
ii) Down Only - Gain can step down only, subject to input levels above the high threshold.
iii) Internal - Gain is controlled by the internal peak detector.

Rectification at the front end of the peak detector allows it to detect positive as well as negative peaks. The rectified signal is compared against two reference levels. A signal above the high threshold for a minimum period of time will cause the auto gain ranging circuitry to step down the amplifier's gain by changing the state of a binary counter. Similarly, gain step up is mandated when the rectified signal remains below the low threshold for the necessary time.

Following each gain change, the counter is disabled by logic circuitry for a short period. When the highest gain setting is reached, the count-up mechanism is disabled to prevent noise and cyclic counting. Count-down is disabled when the lowest gain is reached for the same reasons. Mode and gain control inputs/outputs are TRI-STATE CMOS compatible buffered.

2.0 REALIZATION

The AGRA is fabricated as a multi-layer, thick-film hybrid (package size 2.375 x 2.000, 46 pins). Thin film resistor networks and NPO capacitors are used in the amplifier and filter section to ensure gain and frequency response stability. To reduce power consumption, CMOS technology is used in the design of logic circuitry.

3.0 CONCLUSION

The Auto Gain Ranging Amplifier is a necessary device when one is confronted with the problem of collection and recording of data outputs from high dynamic range sensors. It is especially useful when data is to be collected from a complicated transducer array. Typical applications could include accurate temperature control, wide range vibration measurements, humidity, pressure and shocks.

AGRA SPECIFICATION

	DESCRIPTION OR TEST CONDITIONS	MIN.	TYPE	MAX.	UNIT
AMPLIFIER					
Gain Options	0.25, 1, 4, 16, 64 256, 1024.				
Accuracy	T = 25°C; 10 Vp-p ≤vout; f ≤20 kHz	-	-	0.5	%
Stability	-25°C < T < 85°C; G = 0.25 ÷ 64	-	-	1	%
	G = 256 ÷ 1024	-	-	1.5	%
Low Frequency Response	AC Mode	1.5	2	2.5	Hz
FILTER					
Type	6 Pole Butterworth low pass response				
Options	500 Hz, 2 kHz 5 kHz, 20 kHz				
Rolloff Accuracy	T = 25°C	-	1.5	-	%
In-Band Ripple	F ≤ 0.6 BW	-	-	0.2	dB
Phase Shift	@ Nominal BW	-	270 ±5	-	deg.
	@ f = 0.5 BW	-	115 ±2	-	deg.
Attenuation	@ f = 2 BW	33	36	-	dB
INPUT CHARACTERISTICS					
Input Impedance	Differential mode	-	10//40	-	Mohm//pF
	Common mode	-	2.5//160	-	Mohm//pF
Maximum voltage	-25°C < T < 85°C	-	-	100	Vp-p
OUTPUT CHARACTERISTICS					
Voltage Swing	R_L ≥2 kohm	20	24	-	dB
Capacitance Load		-	-	1500	Vp-p

	DESCRIPTION OR TEST CONDITIONS	MIN.	TYPE	MAX.	UNIT
Current Limit		-	25	-	mA
Overload Recovery Time	To ±1% of final value	-	-	100	uSec
Noise	DC mode BW = 20 kHz	-	50 +3G	-	uVrms
	BW = 500 Hz	-	25 +1.5G	-	uVrms
Offset	DC mode; T = 25°C	-	2 +0.01G	-	mVdc
Offset Drift		-	0.5G	-	uV/deg.C.
Distortion	f ≤ BW	-	-	0.5	%
CMRR	G = 1, f = 60 Hz	70	-	-	dB
	G = 16, f = 60 Hz	80	-	-	dB
	G = 64, f = 60 hz	90	-	-	dB
PSRR	G = 1, BW = 20 kHz, f = 60 Fhz	-	65	-	dB
	G = 64, BW = 20 kHz, f = 60 Hz	-	75	-	dB
PEAK DETECTOR					
Gain Change	Option 1; Step down	7.12	7.5	7.88	Vdc
	Step up	0.79	0.83	0.87	Vdc
	Option 2; Step down	1.20	1.25	1.30	Vdc
	Step up	0.133	0.14	0.147	Vdc
Step Down Time	Minimum time above threshold voltage for step down.				
	Option 1	-	650	-	uSec
	Option 2	-	170	-	uSec
	Option 3	-	70	-	uSec
	Option 4	-	20	-	uSec
Step Up Time	Minimum time below threshold voltage for step up.	80	100	125	mSec
Digital Input/ Output Logic Levels	CMOS Compatible	5	-	15	Vdc
Preset Pulse Width	5 -15V CMOS Compatible	3	-	-	uSec

	DESCRIPTION OR TEST CONDITIONS	MIN.	TYPE	MAX.	UNIT
Logic Blocking Time After Gain Change		10	12	15	mSec
POWER SUPPLY					
Supply Voltage		14	15	16	Vdc
Supply Current	@ Vs = ±15 Vdc,				
	Positive	-	35	45	mA
	Negative	-	18	22	mA
PACKAGE SIZE		-	2.375 x	-	inch.
		-	2 x .23		
Number of Pins		-	46	-	

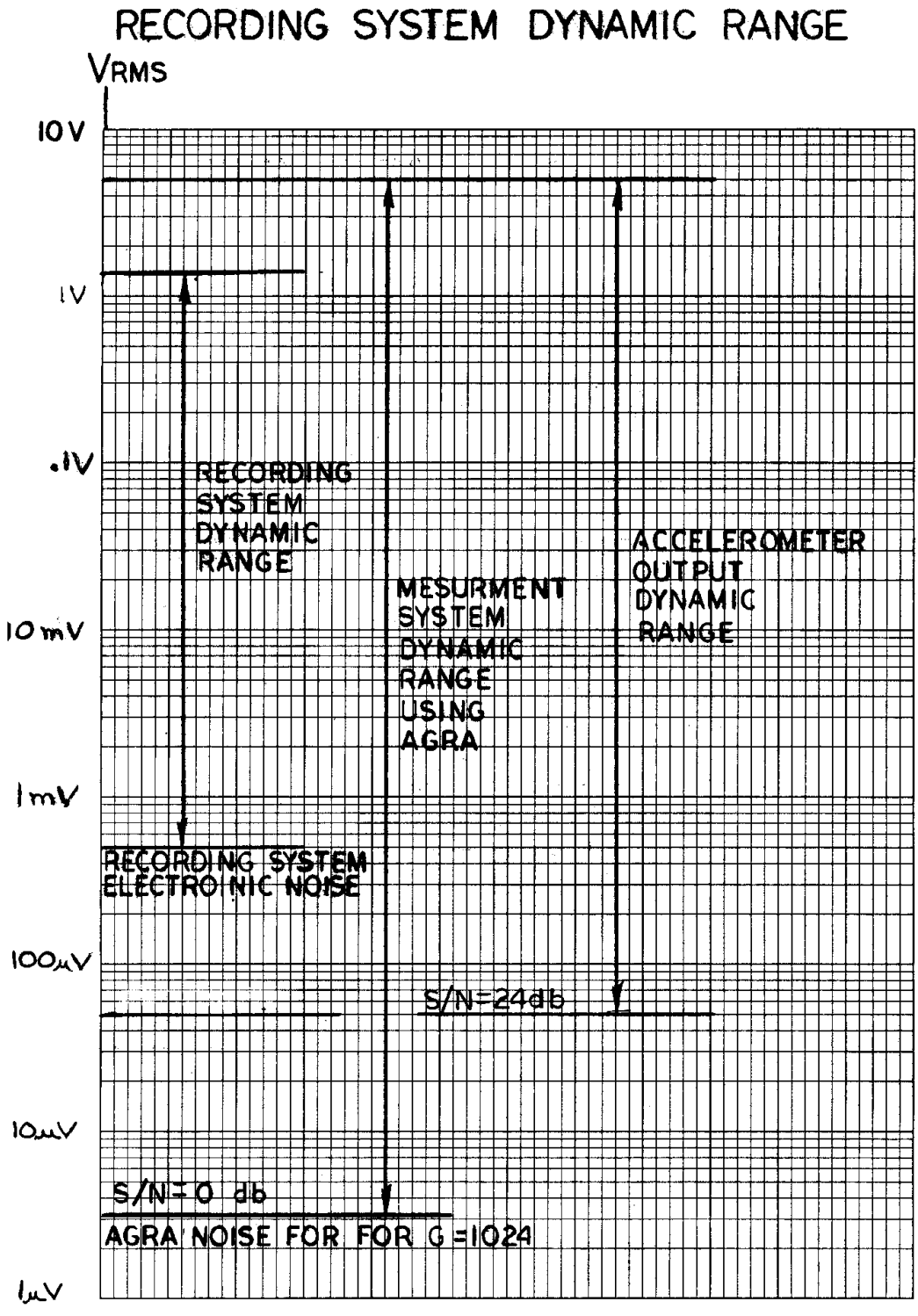

RECORDING SYSTEM DYNAMIC RANGE
VRMS
10V
1V
.1V
10mV
1mV
100μV
10μV
1μV
RECORDING SYSTEM DYNAMIC RANGE
MESURMENT SYSTEM DYNAMIC RANGE USING AGRA
ACCELEROMETER OUTPUT DYNAMIC RANGE
RECORDING SYSTEM ELECTRONIC NOISE
S/N=24db
S/N=0 db
AGRA NOISE FOR FOR G=1024

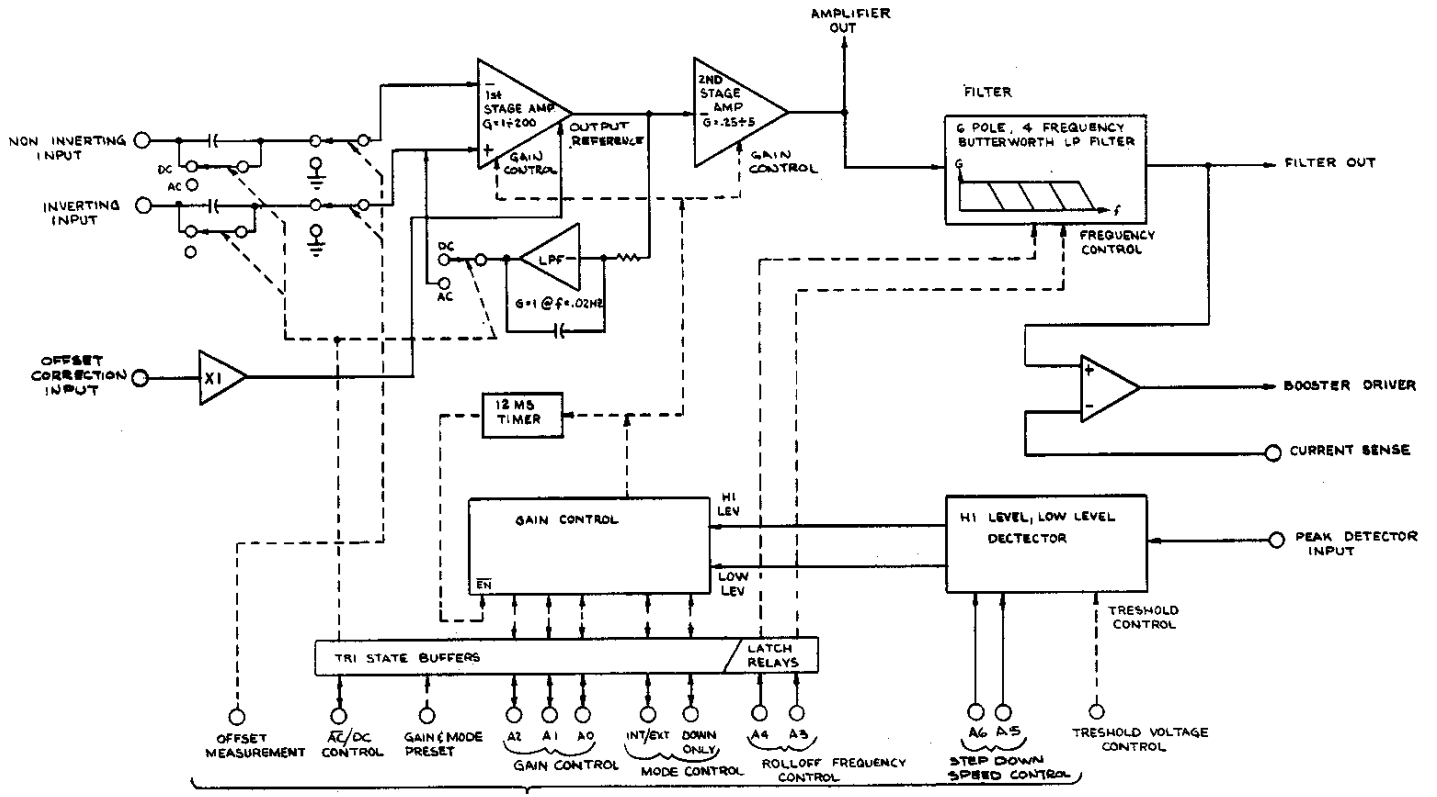
FIG. 1

FIG 2

AUTO GAIN RANGING AMPLIFIER

BLOCK DIAGRAM

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



OPERATION TRUTH TABLE

A4	A3	BW	A2	A1	A0	GAIN
0	0	500 HZ	0	0	X	.25
0	1	2KHZ	0	1	0	1
1	0	5KHZ	0	1	1	4
1	1	20KHZ	1	0	0	16
			1	0	1	64
			1	1	0	250
			1	1	1	1024

DASH NO.	NEXT ASSY	USED ON
	APPLICATION	

MATERIAL:

FINISH:

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
REMOVE ALL BURRS AND BREAK SHARP EDGES
SURFACE ROUGHNESS ✓
DIMENSIONS AND TOLERANCES APPLY AFTER FINISH TREATMENT.

CONTRACT NO. 8194
FIRST MADE FOR AGRA

APPROVAL		DATE
DRAWN	J.A Coleman	4/15/83
CHECKED		
MECH ENG		
ELECT ENG	Nagi	
QA-REL	Crowe	5/1/83
PROD ENG		
PROJ ENG		

AYDIN VECTOR DIVISION

BLOCK DIAGRAM
17

SIZE	CODE IDENT NO.	DRAWING NO.
C	13923	80003349

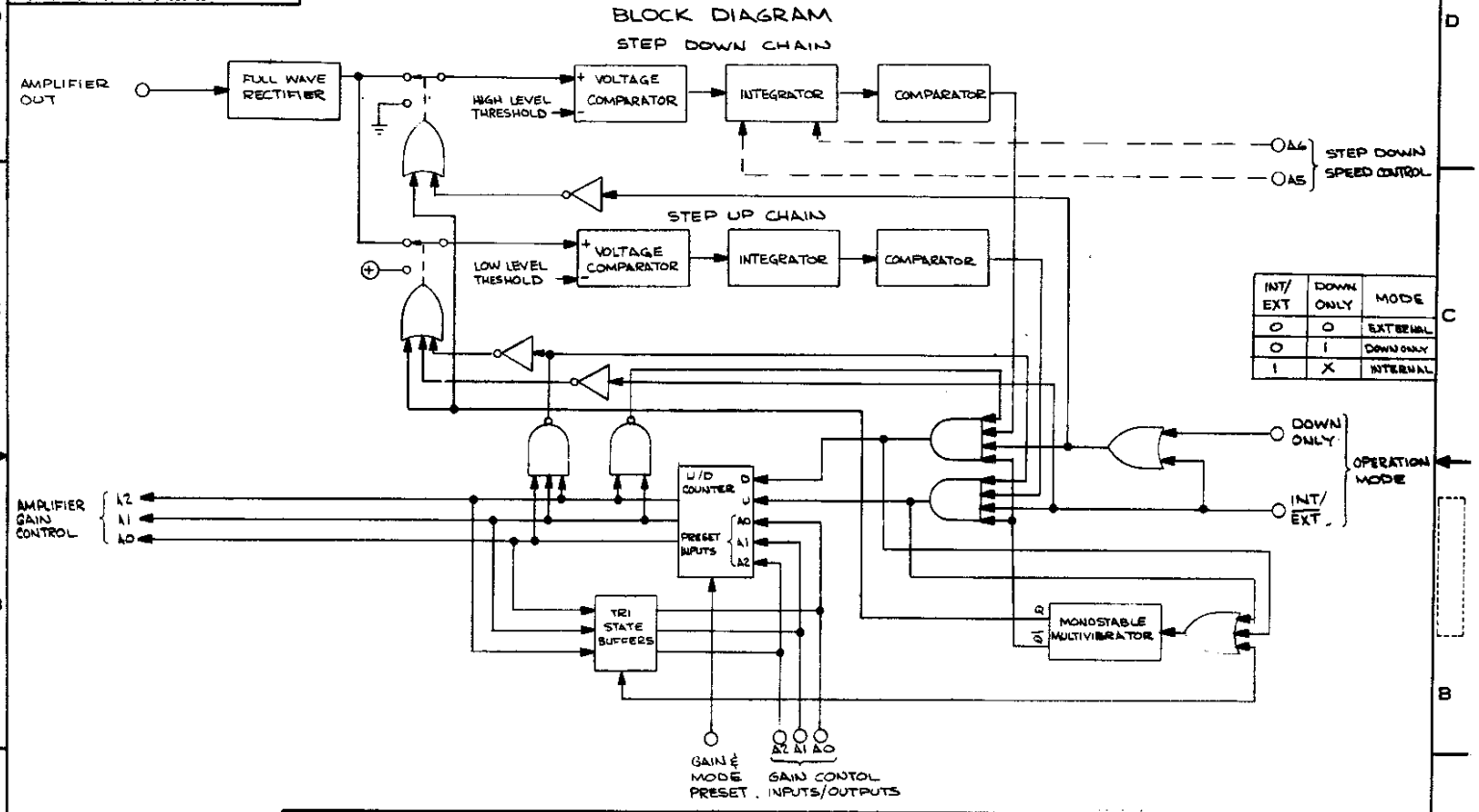
SCALE

SHEET 1 OF 1

FIG 3

AGRA PEAK DETECTOR & AUTO GAIN RANGING

BLOCK DIAGRAM



A6	A5	STEP DOWN RESPONSE TIME
0	0	680mS
0	1	170mS
1	0	70mS
1	1	20mS

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

MATERIAL:

FINISH:

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
REMOVE ALL BURRS AND BREAK SHARP EDGES
SURFACE ROUGHNESS ✓
DIMENSIONS AND TOLERANCES APPLY AFTER FINISH TREATMENT.

CONTRACT NO.
FIRST MADE FOR R.I.d.

APPROVAL		DATE
DRAWN	PB	7.7.83
CHECKED		
MECH ENG		
ELECT ENG		
QA-REL		
PROD ENG		
PROJ ENG		

DASH NO.	NEXT ASSY	USED ON
	APPLICATION	

AYDIN VECTOR DIVISION

PEAK DETECTOR & AUTO GAIN RANGING

SIZE	CODE IDENT NO.	DRAWING NO.
C	13923	

SCALE | SHEET