LINK PERFORMANCE ANALYSIS AND MONITORING: A UNIFIED APPROACH TO DIVERGENT REQUIREMENTS

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ABSTRACT

Link Performance Analysis and real-time monitoring are generally covered by a wide range of equipment. Bit Error Rate testers provide digital link performance measurements but are not useful during real-time data flows. Real-time performance monitors utilize the fixed overhead content but vary widely from format to format. Link quality information is also present from signal reconstruction equipment in the form of receiver AGC, bit synchronizer AGC, and bit synchronizer soft decision level outputs, but no general approach to utilizing this information exists. This paper presents an approach to link tests, real-time data quality monitoring, and results presentation that utilizes a set of general purpose modules in a flexible architectural environment. The system operates over a wide range of bit rates (up to 150 Mbs) and employs several measurement techniques, including P/N code errors or fixed PCM format errors, derived real-time BER from frame sync errors, and Data Quality Analysis derived by counting significant sync status changes. The architecture performs with a minimum of elements in place to permit a phased update of the user's unit in accordance with his needs.

INTRODUCTION

Telemetry is the process which allows the results of sensor measurements made at a given location to be transmitted to a remote location for analysis. The ability to accurately perceive the measurements as monitored at the remote location is directly dependent upon the reliability of the received data. In digital (PCM) systems, the perturbation of a single bit, resulting from a bit error induced in the transmission link, can have a very large effect on sensor data. Therefore, much care is taken to determine the characteristics of the transmission link and reduce error-causing conditions.

Many different types of equipment have been developed to satisfy the above mentioned requirements. Analog test sets are available which provide information about amplitude

and phase distortion, signal dropouts, attenuation, and noise pickup. Digital test sets may be used to provide bit error probability, block error rate, seconds error rate, and burst error rate measurements. Both analog and digital measurement techniques are required in order to properly characterize and optimize a digital telemetry communications link. Once the analog characteristics of the transmission link are determined, a digital system, which minimizes the effects of the analog perturbation, can be designed. This is accomplished by making proper use of digital codes, modulation, schemes, transmission rates, protocol restrictions, and so forth.

The generalized digital characteristics of a link can be determined prior to actual data transmission. For example, the digital link can be objectively compared to an ideal link which has zero errors. Digital error measurement methods and test sets require no subjective conclusion; either the indicated errors are there, or they are not. The difficulty in defining errors lies in the interpretation of the test measurements, which are taken at one time, and their relation to the data, which is taken from the link at a different time. Some link errors may be associated with specific times, data patterns, or other events; other errors may seem to be unpredictable.

During the preoperational period, it is certainly mandatory for every digital system designer to take link measurements during and after installation in order to determine link characteristics. The information gathered during this period is, of course, important and useful. However, in addition, an ideal system configuration would include some means of making link quality measurements while the signalling system is on-line.

THE UNIFIED APPROACH DEFINED

In order to accomplish significant transmission link testing, as outlined above, and assure an optimum digital telemetry communications link, a diverse array of equipment would be required. Clearly, a simplification of the processes and hardware requirements necessary for accurate link analysis would be a welcome development. The unified system approach presented here, as developed by AYDIN MONITOR SYSTEMS, fulfills the exacting requirements necessary for careful link quality measurements and does so with a modular approach. The easily configured, functional modules of this system are interactive, transportable, and interchangeable. The latter feature is most important in such a system, where changing test requirements would oridinarily necessitate significant system changes. The modular family of functional elements on which this system is based can be combined as required for a specific test type, or reconfigured for a new test. The elements are broken down into basic functions so that the same element can be used in various applications.

Each element is packaged on a standard size card (8 x 12") which has a common data bus interface called the High-Speed General Purpose Bus (HGBUS). In this application, the

HGBUS is primarily used for set up of the system modules, but can also be used for realtime data transfer in systems where recovered data is passed between modules. There is also a wire-wrap backplane for special module interconnection. These modules plug into a standard PC card enclosure with power supplies. All I/O is through the rear panel and the front panel hinges open for card access.

One module is common to all of the possible configurations, the I/O Controller. This module is an interface between the user and the functional elements in the system. It can provide user friendly control for local operation and can implement a number of interface protocols for remote control operation. The IEEE-488, RS-232, and other special interfaces are easily implemented. The I/O Controller receives the simple commands from the operator and converts them to the bit level setup commands for each element in the system. It also receives status from each element and formats it into meaningful reports.

The first function of a test device is to provide a stimulus. For digital link testing, the data can either be PN data or simulated frame data. In this system, a stored program simulator module is used to generate this data. The simulator actually outputs parallel data words along with length information and orientation information for input to a parallel-to-serial converter module. This design was implemented for two reasons. First, one of the simulator's data sources is an external parallel word input. By providing a parallel data output, two or more simulators may be cascaded to permit high-fidelity link data simulation, an important feature when format induced errors are present. Second, the design allows the same simulator module to be used for a wide variety of data rates, simply by changing the parallel-to-serial converter module. The parallel-to-serial converter module can have additional logic for specific applications. For instance, for low data rates to 20 Mbps (figure 2), the P-S module also contains a frequency synthesizer to generate an output clock and a code converter to provide bi-phase or other outputs. For higher data rates to 150 Mbps (figure 1), the frequency synthesizer is a separate module and the P-S module can contain a high-speed prescaler to be used for converting incoming data to a slower rate for a standard BERT module. Another P-S module operates with two simulators and outputs two data streams with a programmable bit skew between them (figure 3).

The link analysis function is performed by Bit Error Rate Testing (BERT). The simulator is programmed to output a pseudo-random noise (PN) sequence to the link under test. The other end of the link is connected to a BERT prescaler (figure 5) which compares the incoming data to an internally generated PN pattern. The errors are then reported to a bit error rate monitor which accumulates the errors over a preprogrammed interval to determine an error rate. The monitor can also report total errors, error free seconds, and so forth. The BERT monitor, like the simulator, can also be used with a dual-input prescaler

(figure 6) for simultaneous checkout of redundant links. The BERT can also function with short repeating patterns of 12 or 16 bits instead of a PN pattern.

A second link analysis method allows all data transferred over the link to be monitored, but it can only be accomplished with simulated data. This method compares the incoming data, bit for bit, with a delayed version of the output of the simulator. The delay allows for propagation through the link and through any equipment in the link. The delay can be determined either manually or automatically. The manual method (figure 10) requires the operator to determine the delay by analysis or by scoping the two incoming data streams. The automatic method (figure 11) requires frame synchronization on each input. The delay between the frame marker outputs is then counted. This count is then used as the delay to be inserted before the bit by bit comparison. These two methods are ideal for troubleshooting pattern sensitivity problems or when equipment in the link requires proper data patterns before it will pass it on. (ex. Packet Switching).

Real-time link quality monitoring can take two forms; both can use either real-time or simulated data. First, the real-time data format can be monitored. This is done by synchronizing to a framing pattern in the data using a frame synchronizer module (figures 8 and 9). This module searches for the framing pattern and determines if it is found without errors, at the proper time with respect to the previous pattern, and in the proper polarity. This information is monitored by a status counter module which accumulates expected frames, valid frames, frame dropouts, frames with sync pattern errors, inverted frames, and other data quality related parameters. If other synchronization information is available, a module can be added to detect it and report similar status. For example, the LANDSAT-D image data format has a preamble prior to each image scan; a presynchronizer module is used to synchronize to the preamble and report on preamble synchronization, dropouts, errors, and so forth. The method of link monitoring described thus far will only provide information on frame quality. A possible enhancement (figure 7) could use the frame sync error detecton card to pass frame sync error counts to a BERT monitor card, which could then accumulate the errors over a defined interval to determine a bit error rate. This could also be accomplished by using the presynchronizer to measure bit errors in the preamble. Both of these methods, however, only monitor a small fraction of the available data on the link.

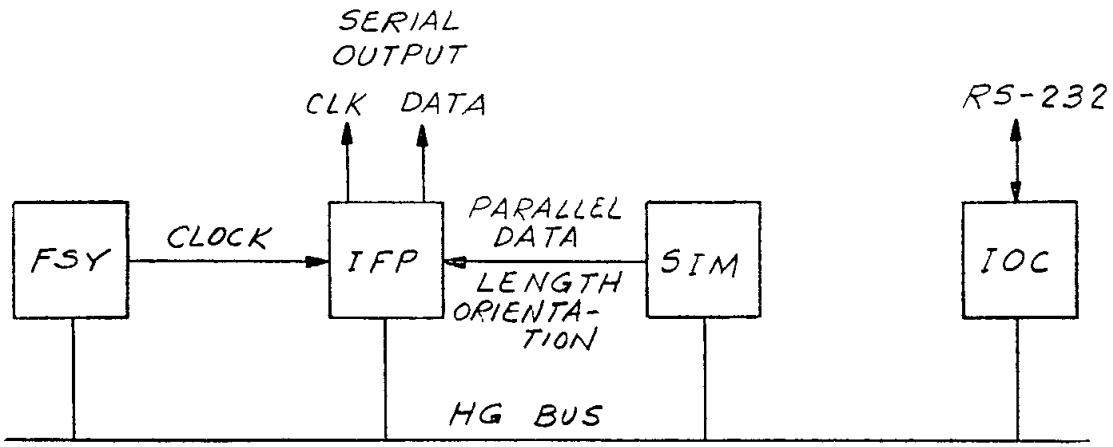
The second form is signal reconstruction equipment monitoring (figure 12). The receiver and bit sync AGC levels can be checked for signal strength and the bit sync soft decision levels can be checked for non-optimal decisions. All of these measurements provide an overall indication of link health, but not so much a quantitative measure of performance. However, they are useful for best stream selection when redundant input streams are available. Combining this method with some of the other real-time monitoring techniques can yield a very powerful best stream selection system.

Many other modules can be added to a system for special applications. For example, a PN generator module (figure 3) can replace the simulator and parallel-to-serial converter when only PN data is required. A perturbation generator module can be added to provide controlled distortion of the output data for margin testing.

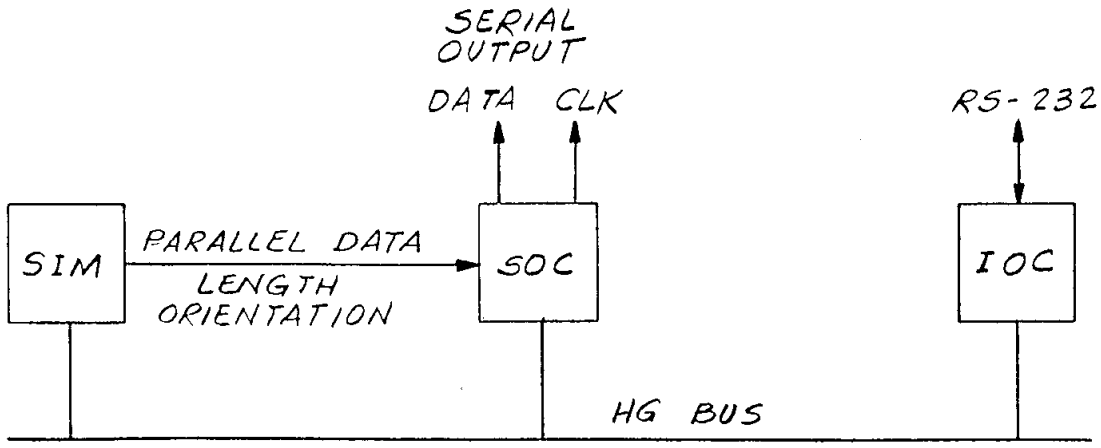
The link analysis and monitoring elements which have been described can be combined into systems with other data acquisition elements to provide a universal approach to communications and telemetry systems.

FIGURE ABBREVIATIONS

ADC - Analog-to-Digital Converter
BER - Bit Error Rate Monitor
BEF - Dual Channel BERT Interface
BSI - Bit Synchronizer Interface
DQM - Data Quality Monitors - Contains frame sync and status counters
DSC - Data Stream Comparitor - Detects errors between two data streams which may be arriving at different times
FSB - Frame Sync Bit Error Correlator - Correlates frame sync errors to position in frame and synchronization strategy
FSC - Frame Sync Error Correlator
FSE - Frame Sync Error Detector
FSY - Frequency Synthesizer - Generates clock for simulated data
IFP - Interface and Prescaler - Contains parallel-to-serial convertion for simulator and error detector for BER
IOC - Input/Output Controller
MTP - LANDSAT MSS and TM Presynchronizer
PNG - PN Generator
SCI - Status Counter Interface
SIF - Dual Channel Simulator Interface
Sim - Simulator
SOC - Simulator and Output Code Converter

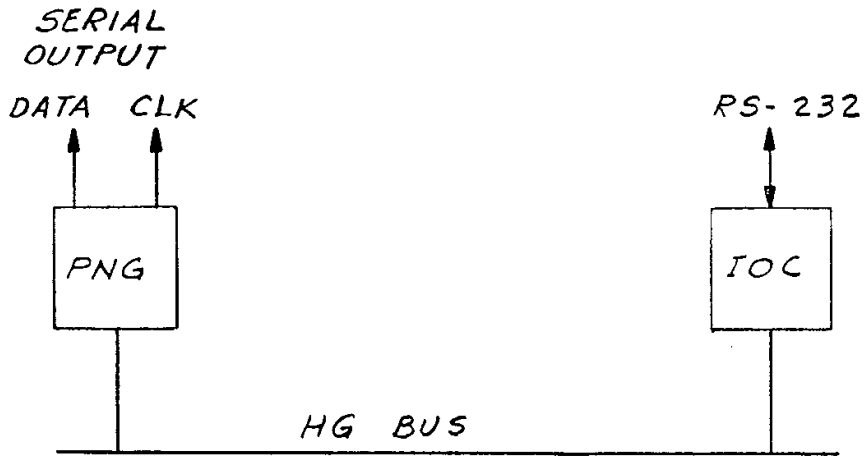


150 MBPS SIMULATOR
FIGURE 1

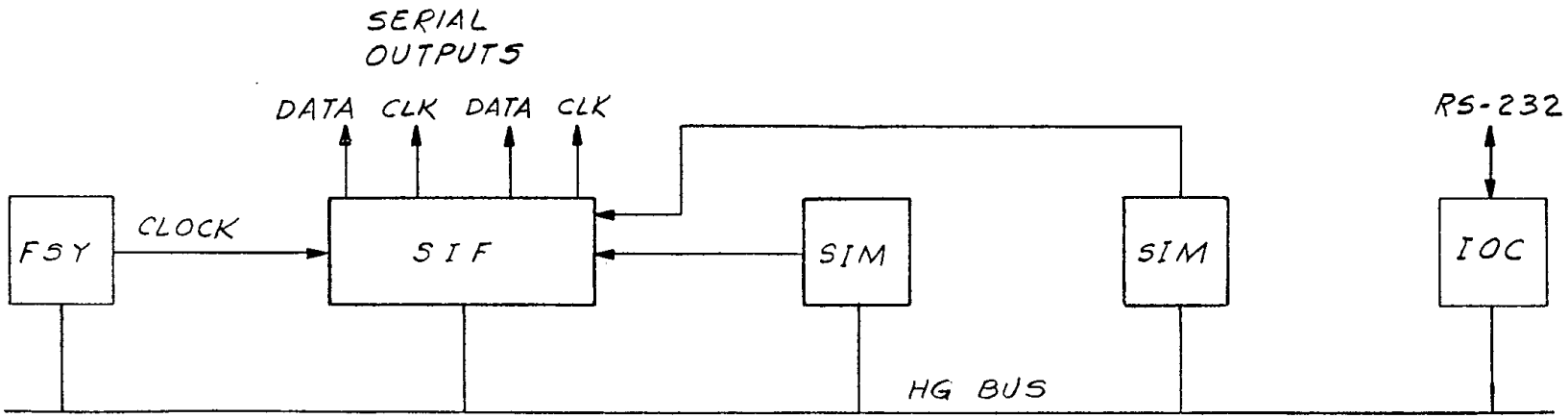


20 MBPS SIMULATOR
FIGURE 2

B) 01-3333-1

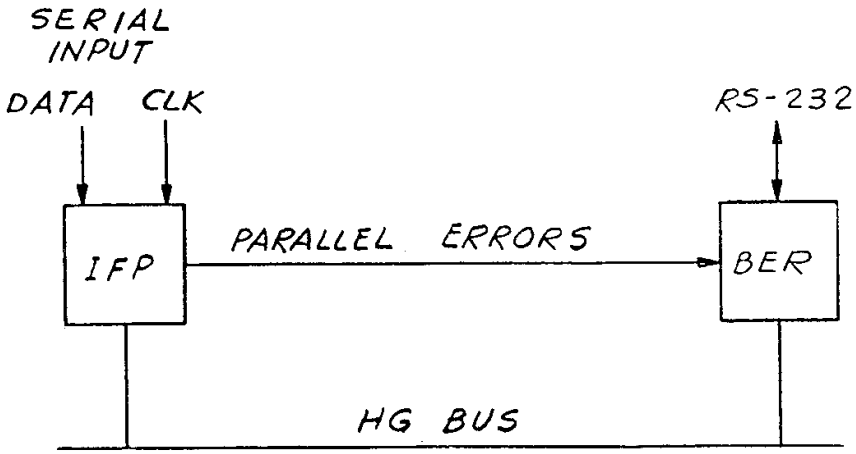


20 MBPS PN PATTERN GENERATOR
FIGURE 3

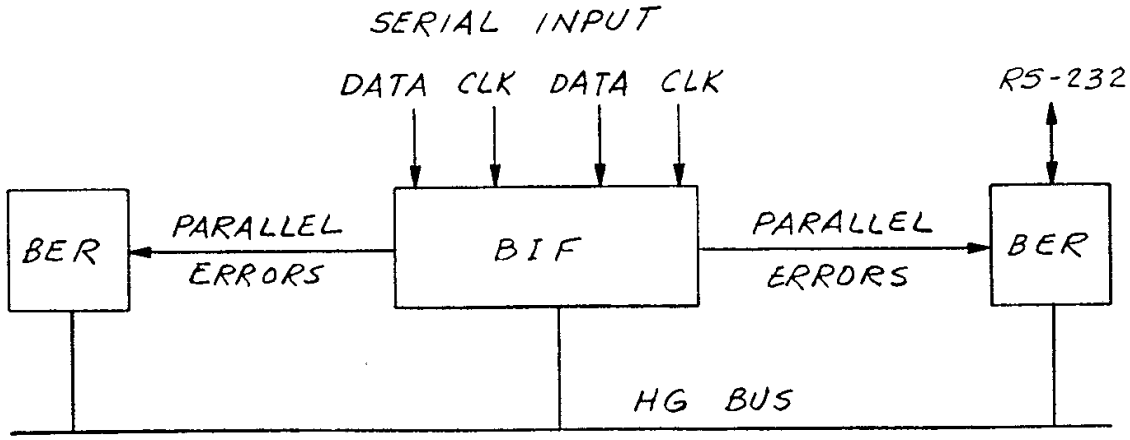


DUAL STREAM SIMULATOR
150 MBPS FIGURE 4

B)01-3333-2

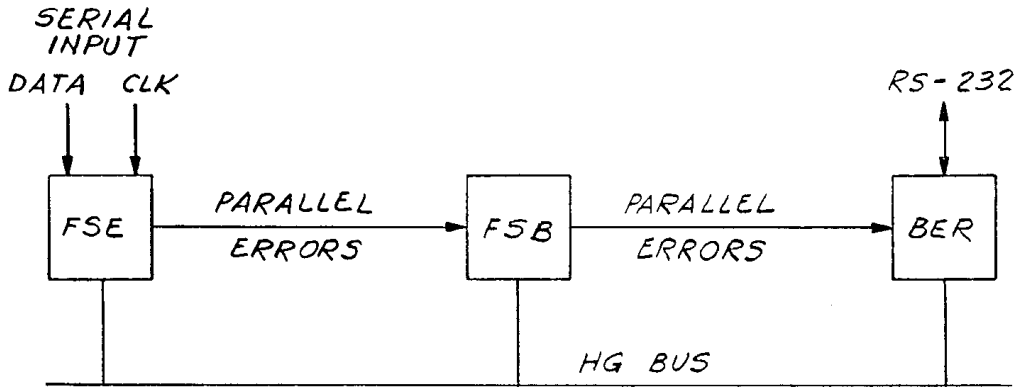


150 MBPS BERT
FIGURE 5

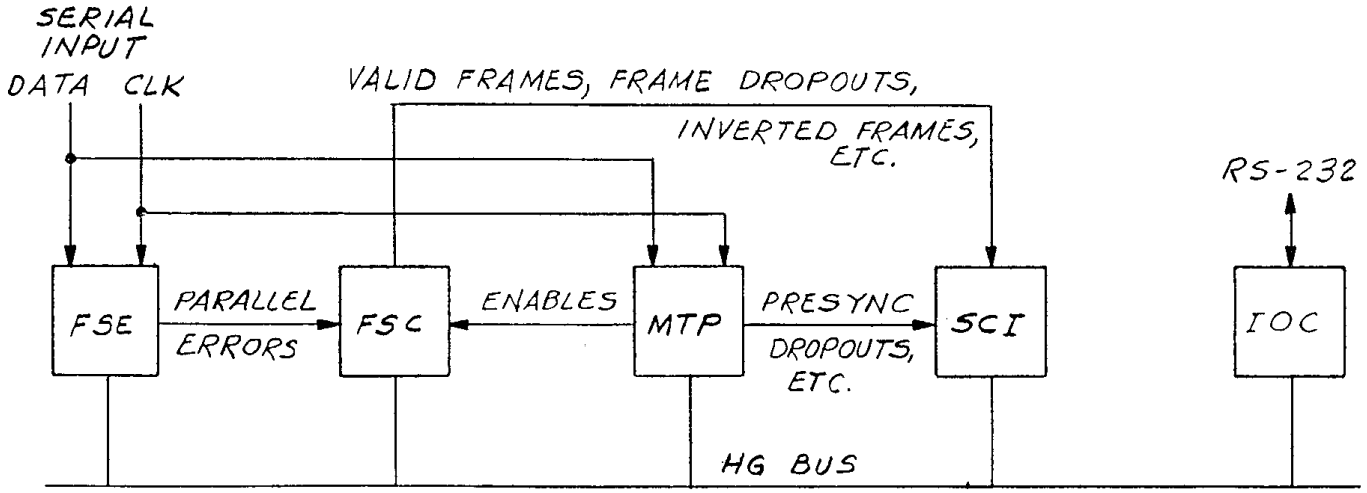


DUAL STREAM BERT
150 MBPS FIGURE 6

B)01-3333-3

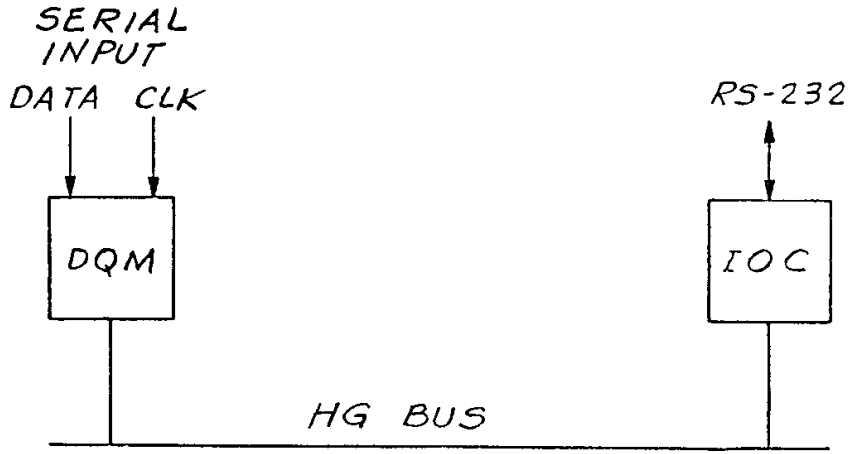


FRAME SYNC PATTERN ERROR RATE TESTER
150 MBPS
FIGURE 7

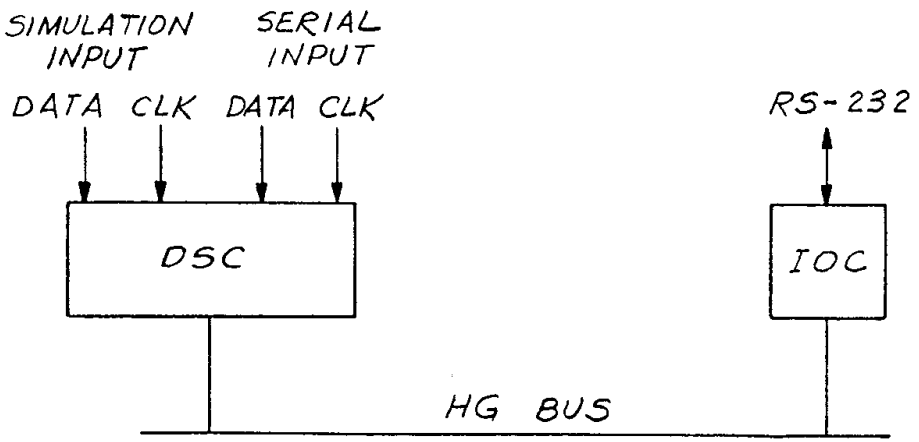


150 MBPS DATA QUALITY MONITOR
WITH PRESYNCHRONIZER
FIGURE 8

B)01-3333-4

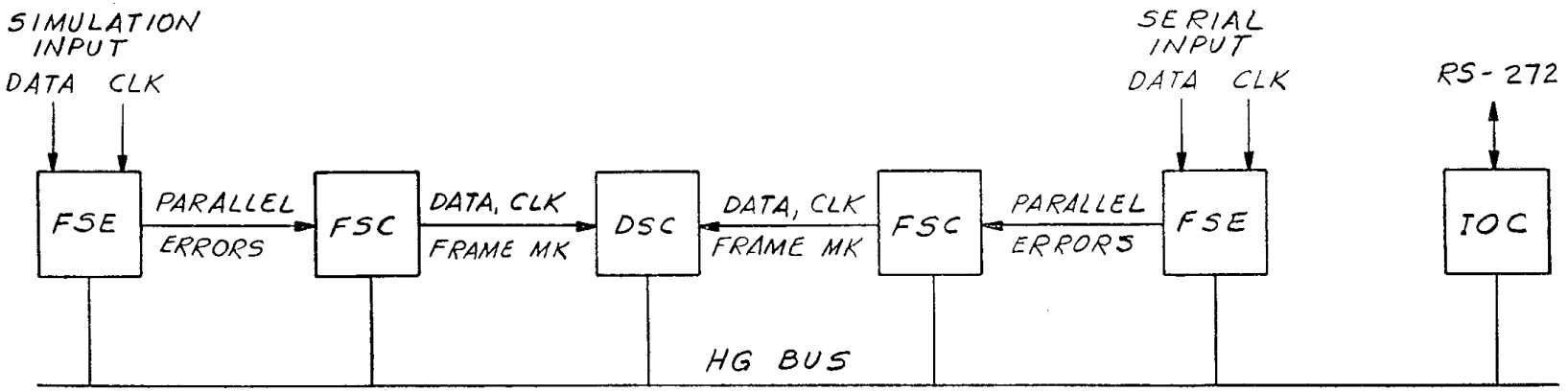


20 MBPS DATA QUALITY MONITOR
FIGURE 9

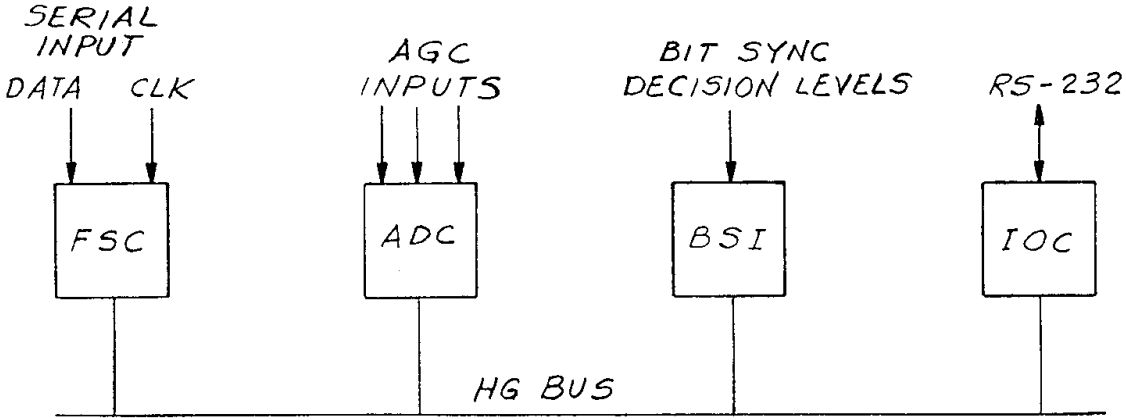


150 MBPS DATA STREAM COMPARITOR
(MANUAL DELAY SELECT)
FIGURE 10

B)01-3333-5



150 MBPS DATA STREAM COMPARITOR
(AUTOMATIC DELAY SELECTION)
FIGURE 11



20 MBPS DATA LINK HEALTH MONITOR
FIGURE 12

B)01-3333-6