An Effective Simple Error Correction Scheme

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ABSTRACT

A simple yet effective error correction scheme for high bit rate digital recording (HBR) using an IRIG tape format is presented. The system is independent of input data rate and requires no analog dropout detection. Typically, 3 orders of magnitude of correction are achieved. The error correction system requires no adjustments. Theoretical results are presented along with emperical data.

1. Introduction

The primary limitation of high bit rate recording today is the error rate achievable with the presently available media. The media performance for analog systems has improved substantially as new and more demanding applications have required, however the demands of HBR systems are significantly different from analog requirements and most HBR systems are presently limited by the media performance, specifically in terms of dropouts. There have been significant improvements in signal processing methods in order to cope with this limitation. The past few years have seen the introduction of Error Correction methods as an attempt to overcome this limitation. The limitation of Error Correction is, of course, the fact that it requires additional data (overhead) to be recorded which reduces the effective storage capability available to the user. The system designer is then faced with implementing an effective ECC scheme which uses the minimum amount of overhead.

2. Analog vs Digital System Parameters

The performance of analog systems is measured primarily in terms of amplitude and phase response versus frequency and dynamic range (ie. SNR). While these are meaningful and necessary to the analog and digital system they are generally measured with instruments which, by virtue of their RMS or average nature, ignore the effects of short term dropouts which are very detrimental to digital signals. The structure of the

digital signal also has different equalization requirements than analog systems. The amplitude response is less critical than the phase response of the system, and the effect on the phase of the signal before, during, and after a dropout is less understood than the effect on the amplitude.

2.1. Dropouts

The effects of dropouts on HBR systems are presently the limiting factor in system performance. Many investigations have been done on dropouts, by both the tape manufacturers and users, in an attempt to characterize the source and effects. This has been done not just for the instrumentation HBR systems but for the digital audio and video systems as well. The generally accepted conclusion is that dropouts are not going to go away, although they can be minimized by careful manufacturing and handling of the media.

Even in applications where dropouts are measured there are a plethora of definitions of how much signal loss for how long constitutes a dropout and how many of these are allowed. For instance. A 1 microsecond loss of signal in an analog system would probably not be noticed, but that same dropout in a 5 Mbit/sec digital system becomes a loss of 5 bits plus any recovery time required by the Bit Synchronizer. Bit Synchronizer design has become an art in itself in order to minimize the additional errors created. Even "partial" dropouts cause a momentary drop in signal to noise ratio which may cause the Bit Synchronizer to improperly decode the data and the phase shift which occurs during the dropout may cause errors which remain undetected until the Bit Synchronizer finds a pattern to resynchronize itself.

3. Error Correction

The system described in this paper was implemented after a number of years of investigation and testing of various schemes to detect dropouts and various methods of Error Correction. Dropout detection methods of various types were tried, with the general result that with every method implemented media was easily found that defied detection. Both Batelle-Hahn and Reed-Solomon Error Correction methods were implemented and although the testing showed encouraging results, the penalties in terms of system architecture and overhead were not encouraging. The system described here is not the only one being used at AMPEX. We have discovered (painfully at times), as most users have, that there is no all purpose ECC system. Each has its advantages and disadvantages and the system selected must be carefully chosen to achieve the desired results within the framework of the system being designed. The system we have chosen for longitudinal HBR yields an error correction ability more than sufficient for the uses we project this system will encounter, it is straightforward in design and implementation, requires little

operator interface (no adjustments) and is comparable with existing AMPEX HBR systems.

The system chosen is a rectangular scheme which is generally familiar to anyone who works with computer systems. It uses a longitudinal Cyclical Redundancy Check on each track to detect blocks of data which contain one or more errors, and an across the tape parity check to correct the errors. After evaluation of the various ECC systems available and the expected error distribution this was determined to be the most effective system with the least overhead for an IRIG tape format system. With this method, the additional overhead is 1 track (the parity track) per 12 data tracks or 8.4%. There is also a version (with less correction ability) with 1 parity track for 24 data tracks which is only 4.2% overhead. With 2 orders of magnitude improvement (typically 3 orders are achieved) in error rate for the system this is a 100 times better performance with only a small overhead penalty.

4. System Description

The ECC system is integrated into the standard AMPEX HBR format, therefore a brief review of that format is included.

4.1. HBR System-Fig 1,2

The parallel inputs (either directly or from serial to parallel conversion) are directed to Sync Insertion circuits where 32 out of each 512 bits of data are moved to a Master channel and a sync word is inserted in their place. The 32 bit block removed from each channel is staggered from channel to channel such that the data in the Master channel becomes a series of 32 bit blocks removed from each of the data channels. Using the 512 bit repeat allows for up to 15 data channels per master channel (the master channel has a sync word also). Thus an IRIG format 14 track recorder can have up to 13 data channels. Figure 2 shows a 12 channel format with one Aux channel where channel 13 has been replaced with the Aux track. In addition channels 12, 11, and 10 can be used as Aux channels by system programming. A 28 track system operates as though it is two 14 track systems with one Master channel slaved to the other.

The purpose of the sync word is for deskew and time base correction in the reproduce system. The sync word is symmetrical about the center so that data can be read in forward or reverse. At the output of the Sync Inserter there is an additional channel (the Master channel), which is the system overhead, but we have not changed the original data rate and no rate dependent circuitry is necessary, thus no adjustments are required in the digital electronics.

The data is then Encoded and sent to Head Driver circuitry and on to the tape. The parallel clock is also divided down to a reference for the transport servo. This causes the transport to run at a speed which is related to the data rate, producing a constant density recording.

The reproduce circuitry consists of the usual Reproduce Amplifier and Bit Synchronizer at the output of which we have data and clock from each channel with the added time base error, static and dynamic skew from the transport. Each data channel is sent to a Deskew circuit which consists of an elastic FIFO which writes data in using the reproduce clock and reads data out using clock and control signals from the Master channel. In this manner skew is removed and, by controlling the Master channel from the customers clock, time base error is also removed. The Master Deskew also redistributes the 32 bit data blocks to the respective channels and the data is sent to the output or to Parallel to Serial conversion as appropriate.

4.2. ECC System- Fig 2.3

The addition of ECC to this system is fairly straightforward. The Sync Inserter is changed to create a parity channel generated from the input data. The channels to be corrected are selected by means of switches on the Sync Inserter. Any combination of channels can be selected for correction, channel 12 will normally be replaced by the Parity channel and channel 13 will be the Aux channel. In configurations with 12 corrected data channels the Parity is automatically moved to channel 13. The programmability allows the user to error correct only those channels which have the most significance, and the fewer channels included in ECC the better the level of correction. Any channels not selected for correction or as Aux channels can be used as normal uncorrected data channels at the parallel clock rate of the corrected channels.

The Sync word is changed from the 32 bit word in the older system to a 16 bit sync word in order to leave room for the Check word in each channel. The Sync word is changed to be symmetrical so that data can be reproduced in forward and reverse as was the case in the original system. In addition the pattern chosen is comparable with the older systems in the forward direction, so older tapes are interchangeable and ECC tapes can be played on the older systems.

A CRC generator is added after the Sync Inserter. It generates a 16 bit word, called a Check Word, which is a result of multiplying the 480 bits of previous data by a binary formula. At the end of each 480 bit period the Check Word is inserted into the first 16 bits of the 32 bit sync period. At the end of the Sync Word (the beginning of the next 480 data bits) the CRC Generator is preset to begin a new calculation. Thus each data block in each

channel will have an independent Check Word. The Master channel and Parity channel are treated the same as data channels so that errors in them can also be detected.

The reproduce electronics have two added functions, Error Detection and Error Correction. Since it is necessary to keep the Master channel intact until after error correction the data redistribution function is disabled in the Deskew electronics.

The Error Detector checks the recorded data and CRC word in each block to determine if an error exists and generates a flag if an error is detected. The flag will be one block minus the sync and CRC space (ie. 480 bits) long regardless of the length of the error. The sync and CRC are not included in the flag since there is no reason to correct them. Because an error cannot be detected until the complete data block has been read, it is necessary to delay the data by the block length of 512 bits. Thus at the output of this circuitry the data and flag are coincident as shown in figure 4. The error flags are also available at a connector on the rear panel for monitoring purposes.

The Error Corrector checks the Parity to see which bit(s) are in error and, by knowing which channel had an error flag, corrects the bits in that channel. This system will correct a channel which has a 100% dropout. The Error Corrector also determines if more than one flag is present and correction is disabled during the time more than one flag is present. The multiple channel flag (called FLAG-2) is sent to the system control panel (Mode Select Panel) to illuminate an LED. Both of the flag signals and the parity result are available at the monitor connector. Because of the staggered sync format, the occurrence of a FLAG-2 does not mean an uncorrected error occurred. It is possible, and in fact this has been seen a number of times, for the error in each channel to be outside the bounds of the FLAG-2 and therefore the errors are corrected, as shown in fig. 4.

After the errors are corrected the Master channel data is redistributed as in the non-ECC system. For customer confidence the parity is checked again after correction and the result is available at the monitor connector.

5. RESULTS

Before this system was designed there were a number of tests and calculations performed to determine if the design was feasible. Principally these involved determinating if simultaneous errors could be expected on more than one channel of typical tape samples. Using some special equipment we tested various samples of tape both very good and very bad for simultaneous errors. The testing also provided data on the expected length of the errors. It was estimated that if we tested 1000 rolls of tape there would be stastically significant evidence to prove or disprove the idea. Needless to say, enough tape was tested to conclude that in the IRIG format simultaneous errors were not likely. In fact all the

simultaneous errors that were found were tracable to manufacturing defects (non-oxide matter coated on the tape) or poor tape handling (scratches or fingerprints on the oxide in the middle of a roll).

An exhaustive probability calculation was also undertaken. By calculating the probability of overlapping flags with various error lengths versus raw error rates it was possible to see what the correction ability of this system should be even without the tape testing program. the results, shown by the solid lines in figure 5, lead into the design of a prototype system. With the encouragement of the results from the tape testing, the final design was completed.

After the first system was complete, another testing program was initiated to attempt to validate the calculations. As can be seen by the data points on figure 5 the calculations have been shown to be fairly accurate. From a more detailed analysis of the data it is also possible to construct a probability estimate of the effective length of a dropout. The typical length of a dropout turns out to be approximately 15 bits or 450 microinches at 33 Kbpi. One of the difficulties of testing a system with error correction is the storage capacity of the tape. A 28 track system stores 1×10^{11} bits (100 gigabits) of data on a 9200 ft. roll of tape and an error rate of 1×10^{-10} allows only 10 errors on an entire roll of tape. Thus at these error rates 90 errors in an entire roll of tape is an order of magnitude difference.

6. Additional Features

During the system design it was determined that we could reduce the setup requirements for the user, provide a low rate data space for such things as time code or other logging information without wasting an entire tape track, and provide a monitor system which can be used to make decisions about the quality of the data actually being reproduced. These features are called Auto Channel Select, M48, and the Flag Monitor.

6.1. Auto Channel Select

The requirement of selecting the channels included in ECC in the reproduce electronics places an additional burden on the operator to know the recorded format. To eliminate this need the system records information about the format and this information is used to program the error corrector electronics.

As can be seen in the sync format (figure 2) there are two unused 32 bit blocks in the Master channel, data block positions for channels 14 and 15. These 64 bits are partioned into a 16 bit block for internal use, and a 48 bit block for customer use. The Sync Inserter inserts a data pattern into the first 4 bits of the 16 bit block which represents the channels selected for error correction. These are read in reproduce to automatically program the

channels to be corrected. The only operator selection is whether it is a one or two Parity channel format.

6.2. M48

The remaining 48 of the 64 bits are available for customer use. A connector on the rear panel has clock and gate outputs and a data input for the record side with clock, gate and data outputs on the reproduce side. With the 48 bit data block occuring once every 512 bits, this gives another data channel at 9.4% of the parallel data rate. This data space can be used to record time code, tape identification information, decoding instructions for a data processor or any other information which can be blocked into the 48 bits. Since a variety of input possibilities exist the remaining interface is left to the customer. The basic interface can be in the form of a parallel to serial converter controlled by the gate and clock from the HBR.

6.3. Flag Monitor

The error flags from each channel are brought out to a connector at the rear of the system. This connector also has the Flag 1 (indicating one or more channels in error), the Flag 2 (indicating 2 or more channels in error and that errors during this time are not corrected), the parity result, the retested parity result, gate and clock signals. The parity error output can be used to determine the raw error rate quite accurately, and along with the channel flags the error rate per channel prior to correction can be determined on the actual data as it is reproduced. The FLAG-2 signal can be used to mark portions of the data which may have errors for further evaluation. These signals are available during playback of actual data.

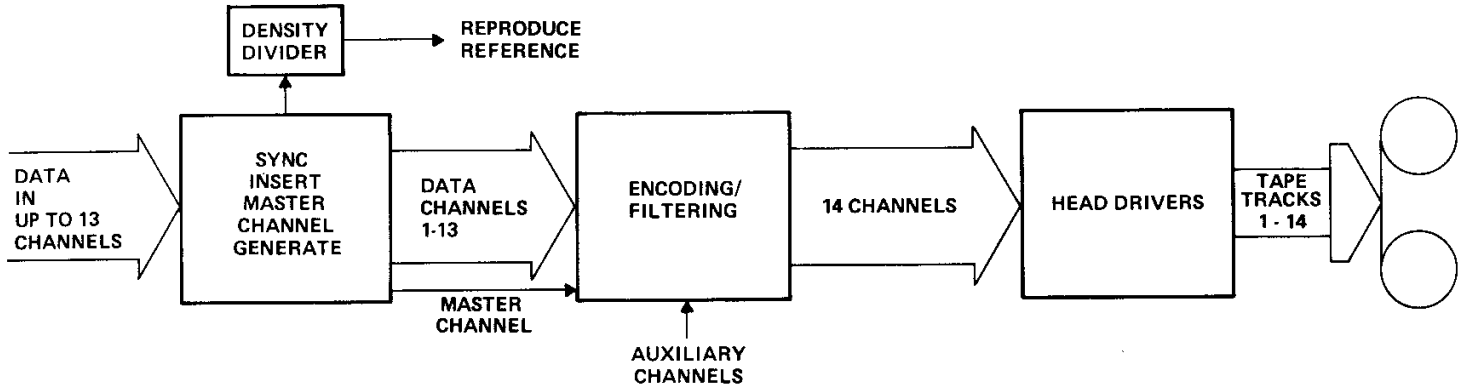


Figure 1A
RECORD SYSTEM

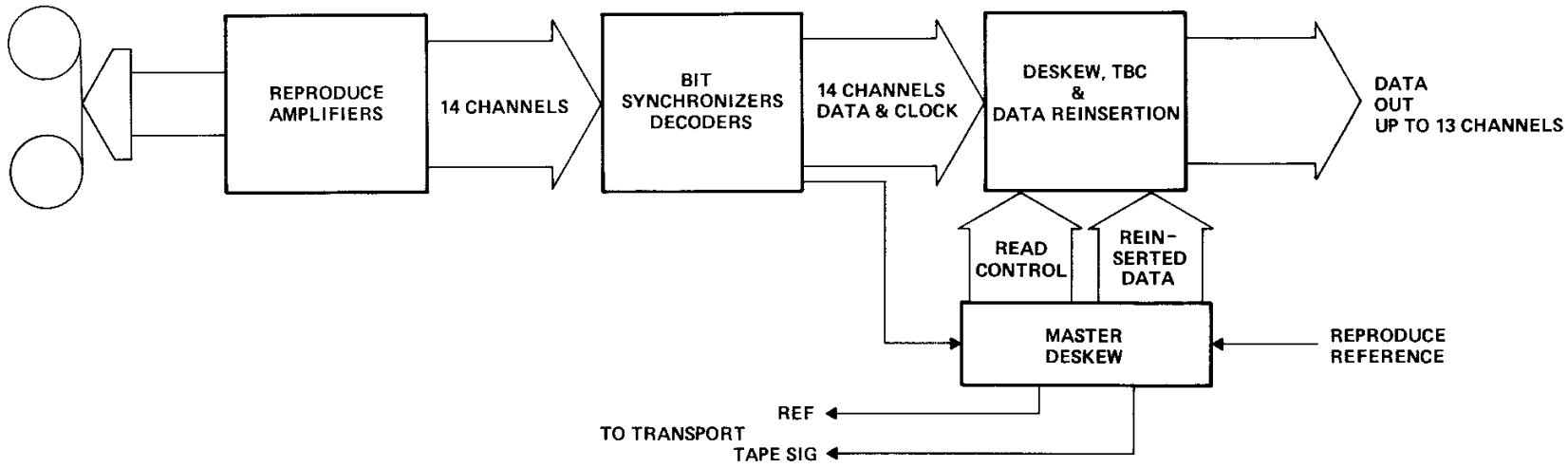


Figure 1B
REPRODUCE SYSTEM

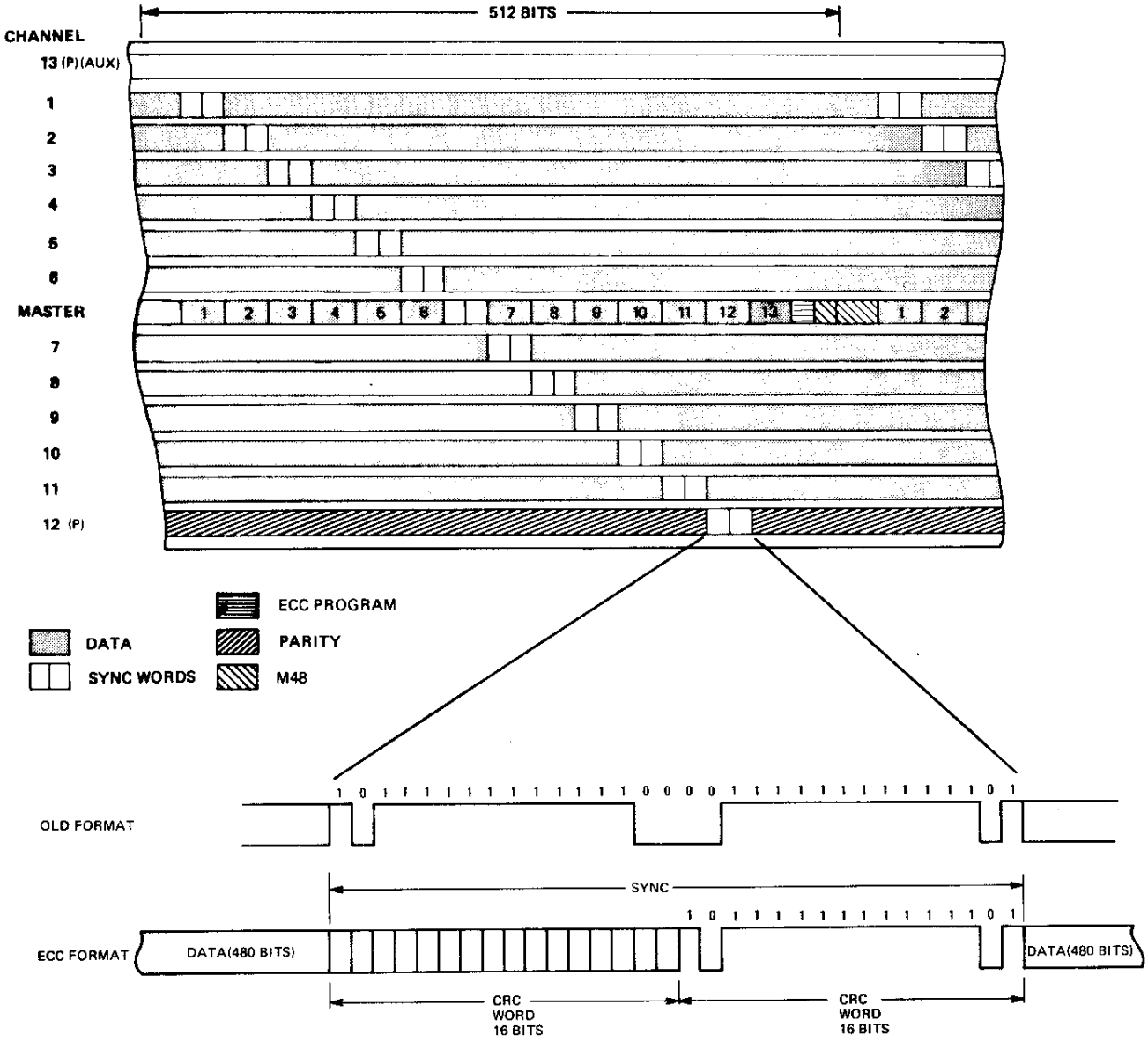


Figure 2 HBR SYNC INSERTION FORMAT

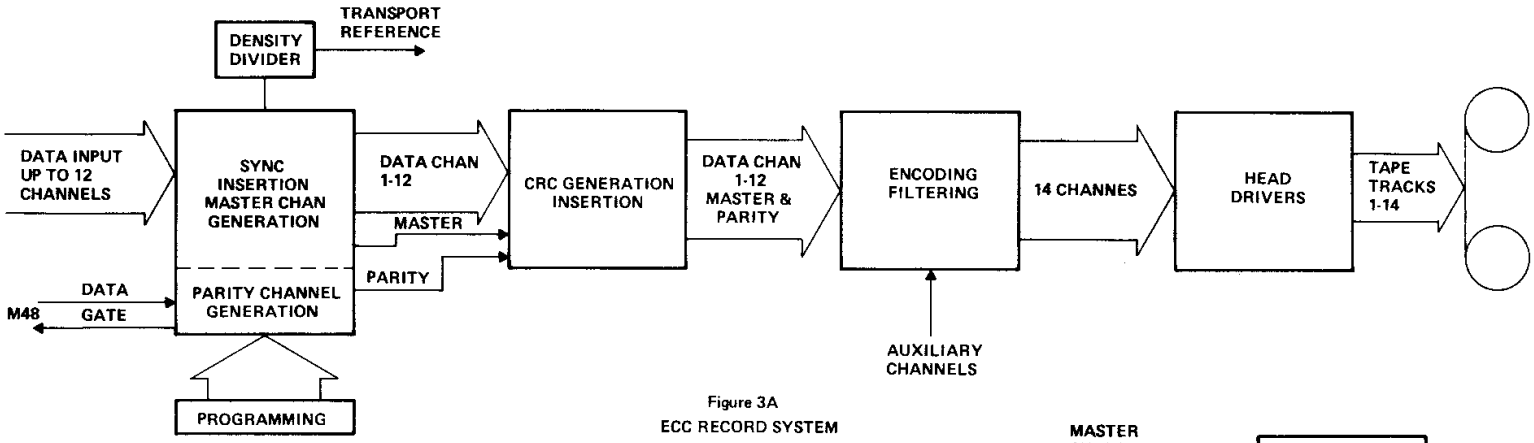


Figure 3A
ECC RECORD SYSTEM

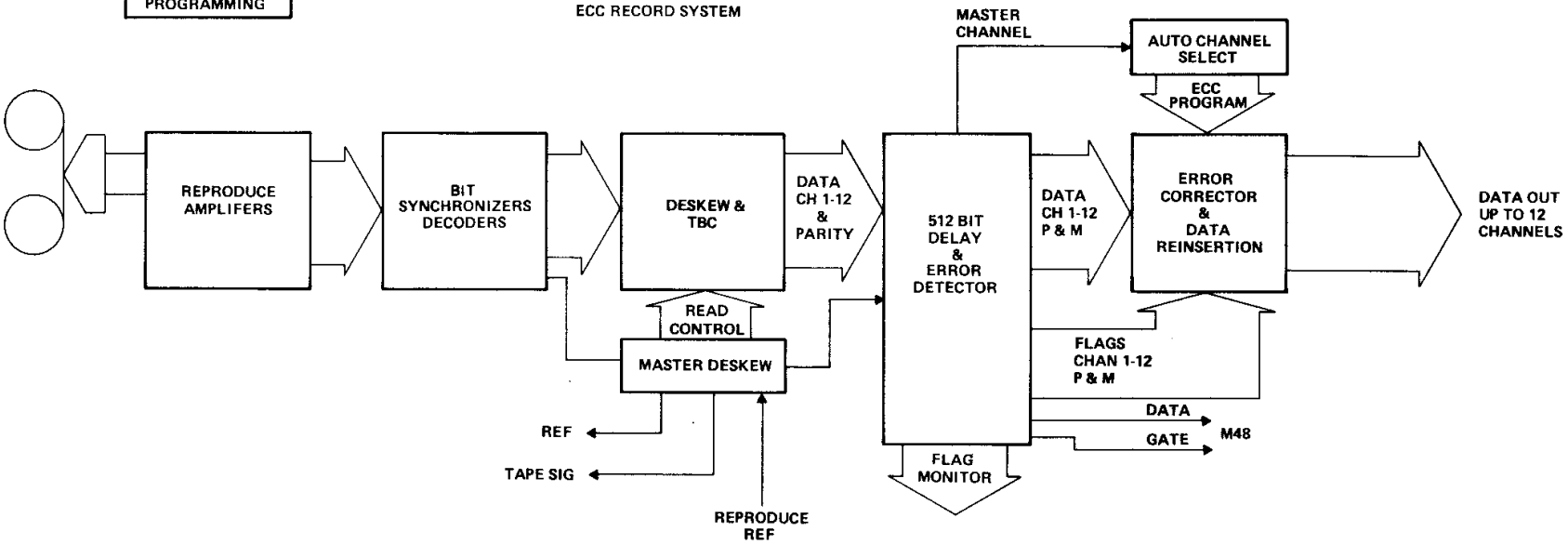
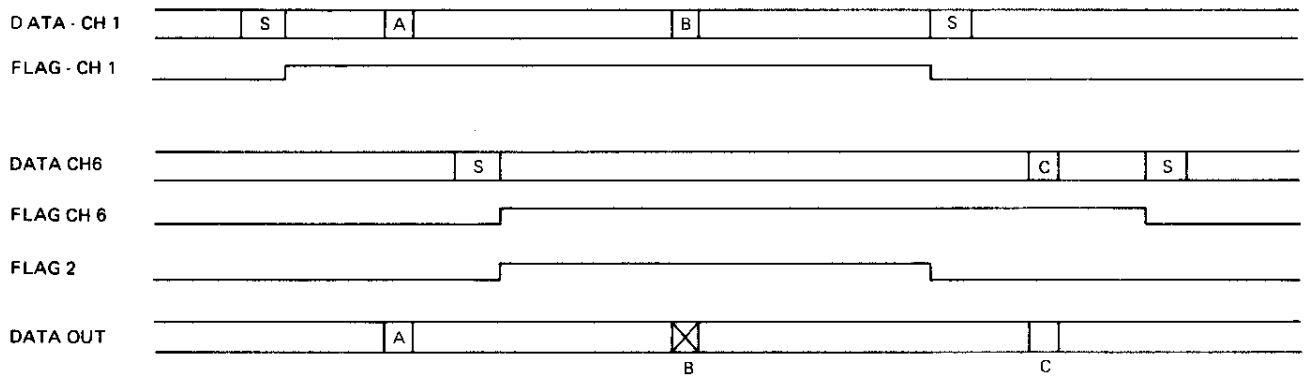


Figure 3B
ECC REPRODUCE SYSTEM



ERRORS A & C ARE CORRECTED
ERROR B REMAINS

OVERLAPPING FLAGS

Figure 4

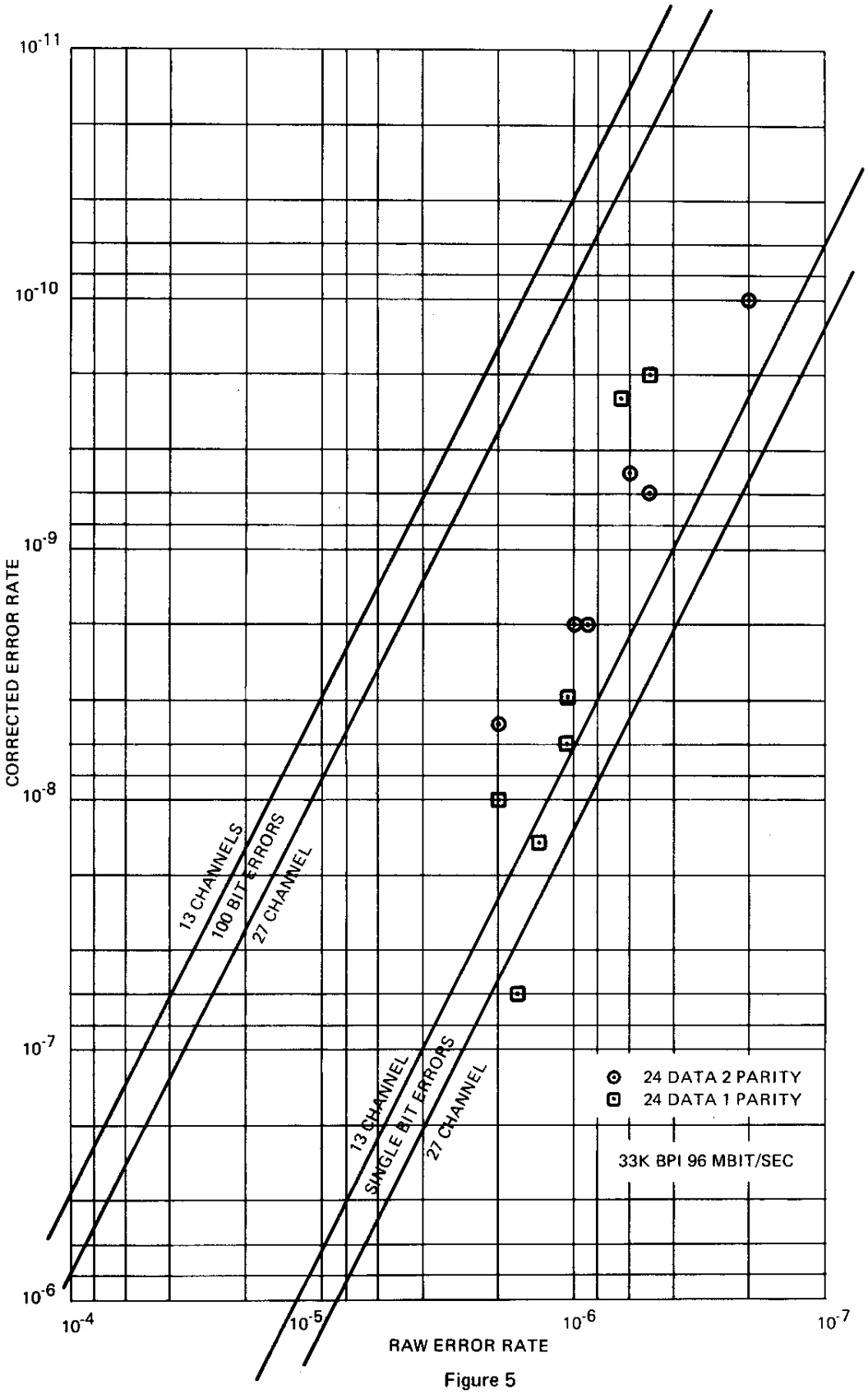

10^{-11}
10^{-10}
10^{-9}
10^{-8}
10^{-7}
10^{-6}
CORRECTED ERROR RATE
10^{-4}
10^{-5}
10^{-6}
10^{-7}
RAW ERROR RATE
13 CHANNELS
100 BIT ERRORS
27 CHANNEL
13 CHANNEL
SINGLE BIT ERRORS
27 CHANNEL
24 DATA 2 PARITY
24 DATA 1 PARITY
33K BPI 96 MBIT/SEC

Figure 5