REALIZING HIGH-RATE SYSTEMS: 
A TECHNOLOGY STUDY REDUCED TO PRACTICE 
for LANDSAT-D

David Grebe 
Engineering Manager 
AYDIN MONITOR Systems 
502 Office Center Drive 
Fort Washington, PA. 19034

ABSTRACT

Generalized use of ECL in telemetry systems requires the reduction of transmission line theory, power distribution, topology considerations, and device characteristics to an implementation that is reproducible, permits rapid changes, and is cost effective. Bringing high data rates (up to 150 Mb/s) to everyday status was one goal in the development of a LANDSAT-D format synchronizer. The unit had to perform preamble and minor frame synchronization followed by decoding, decommutation, and formatting at the Thermatic Mapper real-time rate of 85 Mb/s. To additionally handle MSS and standard telemetry, as well as stream simulation and bit error rate measurements, a generalized solution was required. This is in opposition to a specially designed unit to fulfill only LANDSAT mission requirements. To produce the unit best suited to telemetry disciplines where formats change rapidly, the unit was implemented using wire wrapped modules with the stated goals realized.

INTRODUCTION

This paper deals with the broad aspects of high-rate equipment design. To achieve general purpose, reconfigurable equipment requires much more than careful attention to propagation delays and transmission line theory. The work described herein was accomplished during the design of the 150Mb/sHigh-Rate Frame Analyzer (HRFAS) and LANDSAT-D Format Synchronizer units, both developed under an AYDIN MONITOR Systems contract with NASA, GSFC. Although this paper is centered around these equipments, the reasoning behind the approaches developed has been explained to permit application to the general case.

The development of a family of high-rate equipment (up to 150 Mb/s) began with the adoption of a modular, well-defined electrical and mechanical environment. Other options
were reviewed and dismissed. For example, while mission-specific unit design would represent the smallest total chip count (important to these rates), it would also reduce flexibility and incur zero-based nonrecurring engineering costs. Another approach is to upgrade existing designs by using faster logic families. This would involve too many ICs to be practical in terms of repeatability, reliability, and recurring manufacturing costs.

The modular approach permits a cascading of capabilities since the modules developed for one unit may be applicable to another, reducing unit development costs. Simple interfaces between modules are adopted to permit flexibility and promote high-rate operation by reducing the amount of high-rate interboard connections. After a study of chips-per-function was made in existing designs, a board size was chosen, approximately 180 TTL or 95 ECL. A bus for setup and status collection was developed, to which every module must interface. These two factors alone, board outline and control bus, establish the electrical and mechanical environment. All functional modules developed are, therefore, transportable between units, allowing unique combinations of cards and the addition of specials to address mission specific requirements.

At the module level, each function was reviewed with respect to its performance specification and possible alternate design approach. From the start, it was obvious that the amount of logic actually operating at bit rate had to be minimized. An example of the results this approach yields is the bit error rate tester. It incorporates only 28 ECL ICs. Their operation is supported by approximately 70 TTL chips operating at a parallel word rate of 7.5 Mw/s. Obviously, it is easier to attain 150 Mb/s with 28 ECL and 7.5 MW/s with 70 TTL chips than to take the brute force approach and use 50 plus ECL chips operating at bit rate.

**REVIEW OF ECL CONCERNS**

**Bit Rate**

The design of circuits to be employed directly in the data path began only after certain design guidelines were established. These guidelines were derived from the interactive process of correlating the operating bit rate to the logic families available, to the functionally desired, and finally to the power/size/cost restrictions imposed by the real world. Bit rate has implications for the system beyond limiting the propagation delays acceptable between elements in a synchronous system. At speeds of the TM link, 85 Mb/s, wiring propagation delay becomes a significant factor, as does the apparent delaying of clock lines due to edge distortions. Thus, the selection of design techniques must incorporate clear topological considerations. For example, placing two elements an entire board’s width apart may add as much as 2 ns to the net and prevent operation at the
desired data rate. Although this extreme example is obvious, it illustrates the general principle which must be considered at every step of the design.

Another bit rate derived requirement is the adoption of a completely synchronous clocking technique. In a system where IC complexity is likely to approach 100 ICs per function, the recurring test aspects of the system do not advocate the use of ripple counters or matched combinational network delays. These are accompanied by the requirement for variable or select by test delays for alignment of subfunction signals. Despite its advantages, synchronous clocking is difficult to achieve, since the response time of the ECL families requires the clock skew throughout the system to be well controlled.

**Logic Families**

There are primarily two ECL logic families, 10k and 100k. The 100k family uses a 24-pin DIP package and contains more functions-per-package than the 10k family. It also includes temperature compensation superior to 10k. Thus, signals which span a length of board with an appreciable temperature delta do not suffer loss of noise margin due to temperature shifted VBBs. The 10k logic also offers a significant improvement in speed. This consideration is important not only for the frame sync board common to the 150 Mb/s HRFAS unit, but to the 85 Mb/s LANDSAT presync card. Faster devices mean more gate levels between reclocking which reduces chip count and, therefore, the potential for high rate problems. The 10k devices have the advantage of a similar package size to TTL which may be needed for space considerations on mixed board layouts. The 10k family also offers more device types, presenting greater design flexibility.

**Construction Techniques**

There are basically three wiring techniques available to the logic designers: wirewrap, Multiwire, and multilayer. The choice of technique to be used to achieve a generalized application of high-speed logic involves quite a few parameters. The minimum recurring baseboard cost (multilayer) does not represent the best impedance environment when trying to place a large number of ICs in a given area. The best impedance environment technique (Multiwire) does not present the best total project cost (measured including development time and money), a keen concern of the user. The best total project cost approach (wirewrap, below 100 Mb/s) requires the best designers to juggle multiple, often conflicting, design techniques and rules.

Table 1 highlights the factors involved in the choice of wiring techniques. The importance of each factor was determined to be:
1. Density of ICs

Given that all methods may be used with an appropriate set of design guidelines, the highest density of ICs represents the lowest risk for the following reasons:

   a. Close spacing of elements lessens the importance of transmission line effects. Less propagation time permits ringing to settle quicker before the data is clocked into a register. Less propagation delay also makes more time to settle available between clocks.

   b. More subfunctions may be placed on a board. With fewer boards, fewer high-speed backplane problems are encountered in the system.

   c. Shorter clock runs facilitates low skew, faster clock operation speeds.

2. Ability to make changes

This concern appears in all aspects of a module’s life. During development, the ability to implement a change rapidly represents cost savings. Likewise, the ability to manufacture a board ‘JUST LIKE’ an XYZ-type ‘BUT’ with a few changes here and there requires the ability to make changes to an existing board to keep development costs down.

The density concern rules out the use of a multilayer technique, since it does not represent the highest available density. The ability to make changes does not at first seem to rule out the Multiwire technique. However, changes are made by baseboard cuts and wire additions, a practice viewed with concern by Quality Assurance functions of most users. To eliminate the added wires, subsequent iterations of wire list updates, prototype checks, and final production quantity releases all combine to add substantial delivery delays to what are always demanding schedules. Thus, the wirewrap technique, where changes are made in exactly the same manner as the original wiring was performed, represents the best choice to a practical utilization of high-speed logic in the telemetry field.

3. IC Thermal Consideration

In a high density system, where boards are placed very close together, the ability to provide adequate cooling of the chips is also a high priority. Using wirewrap simplifies the cooling by essentially placing a heat sink on each IC lead (the wiring pin). Large amounts of air are then passed over the boards, top and bottom, to provide the cooling required, especially in the area of the socket pins. No exotic board-based cooling techniques need therefore be employed.
Table 1
Consideration Factors of Wiring Techniques

<table>
<thead>
<tr>
<th>SUITABILITY TO HIGH-RATE OPERATION</th>
<th>SUITABILITY TO THE PRODUCTION EFFORT</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Propagation per unit length</td>
<td>- Absence of wiring errors</td>
</tr>
<tr>
<td>- Controlled impedance</td>
<td>- Material costs</td>
</tr>
<tr>
<td>- Low impedance power planes</td>
<td>- Manufacturing costs, less boards</td>
</tr>
<tr>
<td>- IC thermal dissipation</td>
<td>- Correction of wired board errors</td>
</tr>
<tr>
<td>- Density of ICs</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SUITABILITY TO DEVELOPMENT EFFORT</th>
<th>SUITABILITY TO TYPICAL USER LIFE CYCLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Ability to make changes</td>
<td>- New board cost (development costs)</td>
</tr>
<tr>
<td>- Ability to make high-speed scope observations</td>
<td>- New board design to delivery schedule</td>
</tr>
<tr>
<td>- Changes should match production performance</td>
<td>- Ease of modifications</td>
</tr>
</tbody>
</table>

OTHER HIGH-RATE CONCERNS

Consideration must also be given to the baseboard on which the logic is to be placed. Power distribution must account for the higher currents associated with ECL logic, especially the termination voltage. All power runs must provide a low impedance path to the power source and be well bypassed using capacitors with lead lengths approaching zero. At the edge speeds involved, the leads of the capacitor represent series inductors with the capacitor, which undermines the usefulness of the capacitor.

The ground plane should be on the wiring side of the board in order to serve a second purpose beyond power return. It also provides the wiring transmission line reference. As such, it is important that the ground etch include the area between the IC leads over which wires will be placed.

REVIEW OF UNIT REQUIREMENTS

A brief review of the LANDSAT-D data formats at this point will aid understanding of the design development.

One or both data types (TM or MSS) may be downlinked to ground stations using an X-band link. Thermatic Mapper (TM) data is output at 84.903 Mb/s and Multispectral Scanner (MSS) data is output at 15.0626 Mb/s. Both use formats composed of.

Preamble - a predictable string of data used to achieve synchronization with the start of each minor scan.
Start of scan code - one unique data word which identifies the start of video data minor frames.
Minor frame data - the video data with sync patterns. TM frames are encoded by a PN sequence.

Postamble - data output at the end of the minor scan. This may include calibration data.

The format synchronizer must therefore contain three elements: 1) a preamble/start of scan detector function to synchronize the startup of the minor frame, 2) a minor frame sync to establish video frame data synchronization, and 3) a decommutator to reconstruct the parallel sensor data for input to the computer.

For TM, the preamble consists of an 816-bit PN code sequence. The presync must detect this and lock an internal generator to it. The PN sequence terminates on the all ones code (10 sequential 1s) to indicate scan start. By using a local generator, the start of scan time is located, even though a noise burst might obscure the 1s sequence on the link itself, causing the entire mirror scan to be lost. MSS preamble consists of a repeating 6-bit word followed by its complement to define the scan start. By combining the 6-bit start code with the first 6-bit minor frame sync pattern, a 12-bit start code can be detected. Only the presync’s ability to detect these bits corrupted with errors prevents the loss of an MSS line.

TM minor frame data utilizes a 32-bit sync code. A conventional approach to a frame sync, but at higher, rates is adequate for this data. Therefore, the HRFAS frame synchronizer board set was used. The frame sync function was too large to fit on one board, so it had been divided at a point to minimize the board interconnects. One board compares the incoming data bit-by-bit to the sync pattern and outputs the resulting number of errors in binary. The second board correlates the errors to the expected frame rate, polarity, and applies a programmable sync strategy to achieve minor frame synchronization:

The MSS data uses a 6-bit code augmented by a 6-bit complement code located at midframe. Rather than add a special synchronizer to handle this format, the system
architecture was developed to permit the already special preamble board to aid in minor frame synchronization. By adding a second binary input port to the FSC module, the presync could input the number of errors detected on the 12-bit MSS code generated by the sync and its 1/2 frame delayed complement. This significantly reduces the probability of falsely locking on a 6-bit data word which resembles the sync pattern and permits a straightforward approach to MSS synchronization. The alternative was to establish variable width windows in which to search for the sync pattern, requiring more logic to implement.

The decommutator packs the data into multiple byte words 32 bits wide (4 each, 8-bit words) in order to handle the real-time rate for TM. This could be input to the processing computer (array processor or 32-bit computer) for storage at an acceptable rate (85/8/4 = 2.5 Mwd/s). The TM data also required synchronizing to the PN sequence for decoding the data. This was also considered a special function and placed on the ‘LANDSAT’ decom card.

With the above system capabilities at a ground station, the unit would therefore be capable of handling MSS data at four times the input rate (60+ Mb/s) via tape playback. This is an important consideration for picture production processing.

The unit also provides a rapid indication of the data quality without requiring the operator to examine the video data as it is received and recorded. This is accomplished using the known format characteristics:

* count the number of expected frames of data
* count the number of frames transferred to the CPU
* count the number of minor frame dropouts
* count the number of presync dropouts
* count the number of flywheel minor frames

From these numbers, data quality can be deduced and monitored in real time.

The system also provides built-in tests for itself and other equipment using simulated data. The simulator needed to have the capability to simulate the link formats as an aid to the back-end processing equipment checkout. This dictated the development of a high-rate stored program simulator. The unit also supports tape recorder checkout using bit error rate measurements. This is accomplished using the simulator for data generation and a high bit error rate receiver.

Local control of these functions is required for maintenance operations and stand-alone operation. Remote control is provided for automated picture production facilities.
SYSTEM APPROACH TO THE PROBLEM

The adoption of a standard size module for all functions and the use of a standard bus for setup and control data distribution facilitates future expansion and system reconfiguration as requirements change. But it also imposes a trade-off by restricting the amount of logic available per function. Some functions must be divided into two modules, such as the minor frame sync. It has been found that such divisions often become an advantage, as was the case in AYDIN’s LANDSAT unit when the need for a second error detector input (for MSS) was discovered to be the best approach to synchronization of a less than optimal sync pattern.

It is by repetitively reviewing the partitioning of functions, their interfaces, and architectures, that a synergism of modules can be accomplished. The holistic system approach may even be more important in the realization of high-rate systems than at the lower rates. The setup function is an example. The standard bus for control eliminates banks of switches and indicators from being wired directly to the front panel. Instead, a microprocessor is now between all operator inputs (local or remote) and the boards via the bus. Local control now utilizes a formatted, menu-driven CRT terminal. Adding or subtracting modules requires only the addition or deletion of PROM data on the processor board rather than new front panel metalwork and wiring. The same is true for RS232 control interfaces which required only the interface driver software to be replaced for operation with different host computers.

ECL TECHNIQUES DEVELOPED

Nothing encountered or developed during the high-rate projects was new. All the problems found could eventually be traced to some fundamental precaution or design guideline found in device manufacturers’ literature. It is the relative importance, or misdiagnosis of a problem where large amounts of time can be spent if the design did not take into account ALL of the rules.

Because everything is clocked and reclocked after every few gate levels, the clock is heavily fanned out. To keep clock skew to a minimum, not only must the chip topology be considered, but all the subtle effects on an ECL signal must be accounted for or the clock will be distorted. Distorted edges will have the same effect on operation as skewing or incorrect propagation delays. For example, the power ground leads of an IC cannot handle large, high-speed current changes, as happen when all 8 outputs of a 100112 clock driver become a logic 1 state simultaneously. The result is a knee in the rising edge, almost appearing on an oscilloscope as underterminated net operation. The solution: keep constant current on the power ground pins by terminating all unused complementary outputs corresponding to a used output.
Another substantial problem when using DIP packages is the difference in $C_{\text{out}}$ on the pins at the end of the package. These pins have as much as 7 pF each, compared to 3 pF on the center pins. When used to input to the end pins of other chips, total net capacitance of 20-40 pF is possible. This distorts edges and can produce output signals that appear stretched relative to the input. The rule of thumb was adopted to never use the complementary output to clock drivers, since they are located at the ends of the DIP package.

Another source of edge distortion is poor parallel terminator bypassing. All the LANDSAT modules used SIP terminator packages which have $V_{tt}$ input on one end of the network and no bypass capacitor built in on the other. This leads to noise on the far end pins generated by other pins’ operation, causing crosstalk noise on critical edges.

One reason edge distortion is so critical is the relatively low (3-5 X) gain of ECL devices. Signals that undergo simple edge rounding must be passed through several gates before the normal, controlled rise and fall times are restored. In the case of edge distortion, where one edge (rising or falling) is affected differently than the other, the signal will not be squared-up to the original shape. Apparent clock skewing can be caused by the changing of the duty cycle due to this effect.

**RESULTING SYSTEM**

Figure 1 shows the resulting AYDIN Model 443 LANDSAT-D Format Synchronizer. In one 14"H x 19"W x 20"D chassis it contains:

- Removable Power Supply Drawer (+12, +5, -2, -5 volts)

- 90 Mb/s General Purpose Frame Synchronizer
  32-65K bits/frame 0-15 error tolerance
  AFS, CFS, APC operation 2-32 bit sync pattern with mask
  0-15 check patterns ±1,2,3 bit window
  0-15 flywheel lock patterns

- 90 Mb/s General Purpose, Stored Program Simulator
  5 instructions 5 data sources for output
  2 ID counters 2-32 bits/word, each output uniquely programmable
  indexed data addressing 2048 by 32 data memory
  1024 instruction memory

- 1 B/s to 90 Mb/s Frequency Synthesizer
determines simulator output rate
  5-digit plus exponent resolution
- 90 Mb/s Bit Error Rate Tester
  advanced 3 level, 2 register sync approach
  maintains sync up to .40 BER environment
  achieves resyn to true loss of sync within 148 bit times for BER better than .05
  3 PN codes, 2 pattern lengths
  10E3 - 10E10 measurement base

- Status and Counter Module
  six 32-bit dual ranked counters provide data quality monitoring

- LANDSAT-D TM (85 Mb/s) and MSS (4X, 61 Mb/s) presynchronizer
  12-bit sync pattern for MSS

- LANDSAT-D Decommutator
  PN decode for TM
  byte stacking
  1024 word by 32 bit FIFO
  end of scan shutdown
  computer data interface
  frame flywheeling

- Microprocessor Based Operator Interface
  dual RS232 interface for local and remote control
  floppy disk interface for local storage of setup and simulation data

Figure 2 presents the block diagram of the unit. Note that the number of high-speed lines has been kept to a minimum and in no case is there high-speed, critical feedback from one card to another. Because three of the cards must support higher rate operations in the HRFAS unit for TDRSS, the interface and frame sync cards (EFP001, FSE001, FSC002) were designed using 100k logic. To perform the large number of functions described on one presynchronizer board, the LANDSAT MTP001 card also uses 100k logic. This permits more gate levels between reclocking and therefore lessens the register overhead. The mission-specific card, the decommutator, also contains the TTL-based computer input interface. 10k ECL was chosen to perform the bit-rate functions, such as serial-to-parallel conversion and PN decoding, while the byte stacking, FIFO, and setup interface use TTL.

Also note that the BER and SIM functions are performed using parallel, TTL processors supported by ECL prescalers on the IFP001 module. These prescalers perform the parallel-to-serial conversion function (22 ICs) and BER local PN sequence generation, error detection, and error sampling (28 ICs). Error rate accumulation and PN sync/resync strategy is done by the TTL BER002 card.
CONCLUSION

The goal of developing a standard solution to a non-standard problem generated a high-rate technology base which can be expanded or reconfigured as simply as a 1 Mb/s TTL modular system.

For example, the same functions can be made available (that is, data acquisition, simulation, bit error rate tests, data quality monitoring, and local CRT control) for the French SPOT satellite by replacing the LANDSAT-specific modules with a set tailored to SPOT. In this instance, the MTP presync, the FSE and FSC minor frame sync set, and the DCM decom module are deleted. Their functions are replaced with two new modules. One is a frame sync module capable of 25 Mb/s operation with the long SPOT data frame (64-bit sync pattern on a 74000+ bit frame). The second module is a SPOT-specific decommutator which performs serial-to-parallel conversion and data sample reconstruction from the differentially encoded PCM data (DPCM).

Another variation is to delete the same modules as mentioned above and add a conventional, low-rate TTL frame synchronizer and decommutator to permit the acquisition of the LANDSAT-D Engineering Telemetry, or the Mission Format Telemetry.

Both these examples illustrate that the basic building blocks are configurable to permit their use in widely diverse data acquisition functions without requiring extensive redesign. That this technology base supports formats as commonplace as 8 Kb/s LANDSAT telemetry, as complex as 85 Mb/s LANDSAT imaging streams, or as high rate as 150 Mb/s TDRSS downlink data illustrates that high-rate technology need no longer be synonymous with highly specialized, dedicated systems. Technology is available to support widespread, generalized use of 100 Mb/s telemetry.

References


Multiwire is a registered trademark of the Kollmorgen Corporation
Figure 2. Model 443 Landsat Format Synchronizer Block Diagram