THE GRUMMAN ADVANCED TELEMETRY PREPROCESSOR

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ABSTRACT

The Grumman Automated Telemetry System (ATS) was one of the first computer based real-time flight test systems. It delivered real-time answers enabling Grumman to cost effectively meet its aircraft test objectives since 1970.

Since then, aircraft systems have become more sophisticated with higher data rate requirements and with more on-board processing. Analysts have become more involved with defining man/machine interfaces and more sophisticated in their demand for real-time test data processing system.

This paper provides an insight into the analyses and design trade-offs made when the first major section (The Preprocessor Subsystem) of the ATS was to be replaced. It proceeds from the requirements definition, through acceptance test results of the Advanced Telemetry Preprocessor (ATP).

Emphasis is placed on the ATP hardware configuration, the subsystem software and the design/build cycle. System test results and a look into the future regarding planned applications and possible performance upgrades are summarized. The ATP is the first step in a series of planned upgrades of the ATS which will enable it to meet the flight test user's demand for increased volume, sophistication and user-friendly interaction.

INTRODUCTION

The Grumman Automated Telemetry System was designed in the late 60's and supported the first F-14 flight on 12/21/70. Since then it has supported approximately 3,700 flights of F-14, EA6B, EF-111, A-6A, E2C, Gulfstream and other aircraft as well as several helicopter programs, and numerous ground test activities.

During ATS procurement a team of Grumman engineers generated the specification, Control Data Corporation (CDC) was the prime contractor and Astrodata was the major subcontractor. Since then changes in business directions of both CDC and Astrodata has left the ATS custom subsystems essentially unsupported.

Figure 1 shows an overview of the ATS. Telemetered PCM data and converted analog data are conditioned in the pre-processor section for entry into the central computer. This data is further processed and sent on to the display section for output to the user. The ATS concept, from the initial design, has been to provide “answer” type information to flight engineers in real-time. An example of this is shown in Figure 2 where control stick force is plotted versus aircraft load factor. This one cross plot graphically presents the aircraft pitch transfer function to the engineer. A requisite to this type of plot is that the data points be time aligned.

Another advance afforded by ATS was real-time flutter analysis. Central computer processing involved a time domain least-squares parameter identification technique based on a system difference equation model to determine the resonant frequencies and damping coefficients of aircraft flutter modes. For this processing, it is important that sample time variations, even between data parameters sampled at different rates, be kept to a minimum. It was through techniques like this that the ATS allowed Grumman to cut the F-14 development test program to one-half of its originally planned duration.

THE PROBLEM

The problem was time correlation. In order to achieve real-time answers to the accuracy required, the data parameters must be closely time aligned.

To keep time correlation between data samples, a rate group buffer scheme was implemented to transfer data between the pre-processor section and the central computer. In this process, up to 10 separate buffers are established (corresponding to up to 10 data sample rates) with the length of each buffer chosen so that all buffers fill in 0.1 seconds and transfer at the same time. Central processor software was designed around the rate group technique so it has been necessary to continue with this scheme in the design of the ATP.

Because of the rate group buffer requirements to fill each buffer as expected, data compression was not utilized. Limit checking is done in the pre-processor with any Out-of-Limits (O-O-L) data identifications sent to an O-O-L buffer, which is sent independently to the central processor.

The pre-processor (Figure #3) was built by a CDC special systems division at La Jolla which has since been disbanded. Custom hardware and software was designed and produced for the CDC 1700 based pre-processor including a 1700/pre-processor operating system. The hardware was composed of CDC “cord wood” circuits, a technology branch that didn’t develop so replacements haven’t been available for years.

PCM data at rates up to 50,000 wds/sec were sent through a bit synchronizer and then to the Telemetry Data Formatter (TDF) which was actually a software decommutator. Analog data was sampled by an Analog-to-Digital Converter (ADC) that was completely controlled by the Analog Data Formatter (ADF). Sample taking was commanded by the ADF to accomplish requested sample rates to be merged with PCM data samples.

The Programmed Input/Output Channel (PIOC) accepted PCM data from the TDF, analog data from the ADF and did Engineering Unit conversion as well as limit checking. Time code words were input through another interface and were appended to each data buffer. The External Storage Module (ESM) stored coefficient values for engineering unit conversion and limits information. Digital parameters were sent to Digital-to-Analog converters (DAC) for output to chart recorders.

The CDC 1700 computer communicated with the central processor, loaded the special boxes, controlled the special boxes, monitored status and generated digital tape.

To derive the design for the ATP each function of the existing equipment was reviewed regarding which to maintain and which to eliminate. For instance, PCM data would be accepted at the bit synch outputs, analog data would need a complete new path. DAC data and time both depended on obsolete equipment and would require complete new systems. The central computer interface would have to be functionally identical to avoid software changes.

REQUIREMENTS SUMMARY

Provide a throughput of at least 50,000 wds/sec for 512 parameters.
Accept PCM bit synchronizer outputs.
Engineering Units Conversion.
Out-Of-Limits checking and buffering.
Do rate group buffering.
No data compression.
Merge PCM and analog data.
Time tag data buffers.
Store EU coefficients.
Store limits information.

Provide DAC outputs.
Generate digital tape.
Run diagnostics on all elements.

REPLACEMENT CONSIDERATIONS

Replacement criteria for the preprocessor function included a baseline of the capabilities of the current system and expansion capacity to meet future requirements based upon predicted aircraft testing and instrumentation systems. Among the future requirements were increased processing speed (from 50,000 to 100,000 samples/second), capability for the preprocessor to be a standalone system, having both calculation and display abilities. A critical goal for the ATP is the ability to handle formats from systems flight test aircraft which in the future are seen to be the bulk of the test work at Grumman. The ATP must be able to handle word lengths from 1 bit to 64 bits, intermixed word lengths within a format and programmability of EU conversion algorithms. A further set of goals was added by the design team over and above the required objectives of the Advanced Telemetry Preprocessor (ATP). The most important of these were:

1. Provide as much excess machine power as possible (the design goal was 50%).
2. Strive for modularity in hardware and software for product growth purposes.
3. Develop the nucleus of a design which could be used to satisfy other needs.

With this background, a preliminary design was conceived including tradeoff analysis between telemetry equipment and computer hardware and software. In a market search it became apparent that there was no product on the market at that time which fully satisfied Grumman's needs. It was decided that for PCM inputs a unique ID rather than frame and subframe addresses would facilitate a table lookup scheme for data elements. Thus an Aydin - Monitor 1126B decommutator was chosen since it offered the ID tagging capability in a single piece of equipment as well as the other necessary format handling abilities.

The ability to process up to 50,000 5th order polynomials per second "on-the-fly" pointed to a choice between streaming data through an array processor, building some special purpose dedicated hardware or utilizing multiple mini-computers. Since it had been decided to build hardware where it was felt to be necessary to meet the overall design criteria rather than possibly sacrifice speed or cost to make use of off-the-shelf equipment, that decision coupled with the functional requirements of the preprocessor pointed to a blend of off-the-shelf and special purpose hardware to satisfy the architectural requirements as well as the goals set by the design team.

HARDWARE OVERVIEW

A block diagram of the ATP is presented in Figure 4. To provide simultaneous testing of two programs, there are two identical ATP's which share common peripherals not utilized in support of real-time tests. Only one complete ATP is depicted in the diagram with the other understood to be an exact duplicate. Data flows in from the left and has already been conditioned by an IRIG compatible front end which includes telemetry reception and demodulation equipment, wideband tape recorders/reproducers, bit synchronizers, analog discriminators, cross-connection facilities and various calibrators, simulators and monitoring equipment for setup and checkout. The PCM and Analog 2 stage processors differ in the first stage but have identical second stages. Stage I of the PCM receives data/ID pairs from the decommutator which is programmed to pass only the data of interest. Under software control as the ID is used as a vector into a list which points to the addresses of previously linked lists of algorithms to be used for each measurement. Data can then be converted to engineering units (up to a 5th degree polynomial), or passed raw, then DAC'd out before passing to Stage II. The second stage performs limit checking and stuffs various buffers (real-time, mag tape, out-of-limits, critical) using an external write mechanism available with SEL's HSD interface. Time is also tagged to each full buffer through a special interface developed to a time generator/translator.

Analog data is treated much the same way with a 96 channel 12 bit MUX/ADC in place of the decommutator interface card. Analog Stage I controls the sampling and first degree polynomial conversion using a variation of decommutator programming rather than the typical scan list. Data is passed to the second stage in an identical manner to the PCM processor and the second stage data handling is identical.

The SEL 32/77 mini-computer receives interrupts from the Plessey microcomputers when the various buffers are filled and after interrogating status words to determine which buffers are ready, chains them together, performs format conversion and packing as necessary, and writes data to the Network Systems Corporation HYPERchannel™ data link in real-time mode or to the attached tape decks if in standalone mode. Buffers are delivered to the central computer in the same format from the ATP as from the replaced 1700 system. This was accomplished by reformatting the data in the SEL computer before transmission to minimize software changes in the central computer system.

The heart of the ATP is the Plessey microcomputers which make up the PCM and Analog processors. The devices are general purpose 16 bit microcomputers chosen for their speed, peripheral card capabilities and separate program/data memory architecture. The common bus structure made an excellent vehicle for physically locating and developing the various special interfaces built by Grumman. Executing all but two of its native instructions in 250 nanoseconds, including a 16 x 16 bit multiply using a hardware multiplier card, the Plessey

has the speed to support Grumman's "processing on - the - fly" preprocessing concept while allowing full programmability. Figures 5 and 6 present the PCM and Analog Processor sections respectively. Each consists of two Plessey microcomputers in a pipeline arrangement which effectively doubles the available processing bandwidth. A common multidrop 16 bit parallel path connects to all PCM and Analog stages using a Grumman developed Down Line Loader (DLL) card as well as to the Aydin Monitor 1126B decommutator. The DLL has the capability of servicing up to 16 devices and provides a two-way path for both loading and readback of status or data. Each DLL is capable of both DMA and cycle stealing operation in both read and write modes providing both fast loading (DMA) and the ability to change coefficients, DAC assignments and other variables while the processor is running (cycle steal). All DLL's are identical, requiring only the setting of address switches to uniquely identify themselves to the multi-drop bus.

Replaceable PROM's driving a microprogrammable engine on the DLL permit easy modification of the DLL's internal instruction set should the need arise. Full programmability of both program and data memory allows easy changes to be made both betwen and during flight tests. This allows for completely different algorithms to be used at various times in a test.

Stage I of the PCM Processor contains processing lists of linked algorithms and corresponding constants and coefficients for each measurement of interest. A decommutator interface card receives both data and corresponding ID in a parallel format and buffers it through a FIFO to smooth burst data rates. Using the ID to vector to the first address of the processing list, an instruction word is sent to the decom interface which provides code conversion, parity strip and up to 15 bit shifting in the next 250 nanosecond machine cycle. Control is then returned to the next entry in the processing list which may typically include up to a 5th order polynomial conversion, a raw data pass and/or output to either a 12 bit DAC (EU or raw) or to a parallel register for event data. Other existing algorithms support handling of multi-syllable data (for which the ID is imbedded in the data word) and some data compression. Because of its programmability (supported by a cross-assembler on the SEL computer) almost any conceivable algorithm could be implemented. The input FIFO assures that long algorithms can be accommodated by providing smoothing of the burst input data.

Eight channel Digital-to-Analog Convertor cards, also built by Grumman, provide a variety of code conversions and voltage output ranges depending upon strapping options. Requiring only one card slot per 8 DACs there are presently 48 DACs in the first PCM stage.

Analog Stage I has a 96 channel multiplexer with 64 single ended and 32 differential channels controlled by the Plessey microcomputer. A Grumman-built programmable

frequency divider card provides interrupts which start the microcomputer through pre-programmed channel sequences downloaded to data memory. Overlapping between the MUX/ADC and hardware multiplier card allow rates as high as 110 K samples per second to be achieved, including linear conversion. PCM and Analog Stage I's differ only in the program and data downloaded to them.

A dual parallel interstage interface allows passing of both data and its corresponding ID to the second stage with an interlock to the input FIFO to prevent more data from entering Stage I until the outgoing data has been accepted by Stage II. The interstage interface also allows bidirectional passing of data and status between stages, if desired. The second stages of both the PCM and Analog Processors are identical, each having a DLL interface, an interstage interface to communicate with Stage I and a Plessey/SEL Interface (PSI) to send data to and from the SEL computer. Stage II builds series of double buffered rate groups depending on sample rates and output locations. The buffers are built directly in SEL memory through use of the external mode capability of the SEL High Speed Data (HSD) interface. This device allows external, scattered, write and read capability from an external device directly into the SEL's memory. Once placed in external mode at the initialization of a test (it also supports DMA mode) the HSD operates with no overhead of the SEL's CPU. The PSI and Plessey program keep track of all buffer locations and are limited in address capability to safeguard the SEL's operating software. Upon filling a buffer, the Plessey/PSI immediately begins writing the corresponding half of the double buffer, reads time from the time code device down to 100 microseconds and then posts the status of the buffer and time when filled to the SEL. The PSI contains an output FIFO to account for possible contention on the SEL's internal bus, called the SEL bus, when writing to or reading from memory. Utilizing a microprogrammed sequence directed by a PROM the PSI is capable of reading data back from the SEL, modifying it within the Plessey as desired. The unique capability allowing machines to be added to the SEL minicomputer with no bandwidth loss of the SEL CPU has not as yet been fully exploited, but surely will be in the future.

The SEL 32/77 minicomputer is a 32 bit 800 K instruction/sec. machine. It is especially suited to high I/O rates with microcomputer based smart interface cards (such as the HSD and the 26.67 M Byte SEL bus connecting them. This machine was chosen for its I/O bandwidth and purposely under-exploited in the initial implementation of the ATP to have as much excess power as possible for future growth. In the real-time mode, the SEL acts as the traffic cop controlling all loads, transfers and processes all requests. All ATP software resides on its disk which is then downline loaded to the Plesseys and decom and upline loads to the central computer, via the HYPERchannel link. HYPERchannel mode consists of two parts, a general network interface common to all modes, and a specific machine interface to attach to the particular type machine at a mode. All network protocol and transfers are handled in a common fashion while specific machine code is necessary to

fill the HYPERchannel's internal buffers in the prescribed formats. Due to the intelligence of the mode a low overhead is used in the host computer.

SOFTWARE OVERVIEW

An overview of the ATP software is presented in Figure 7. The software set is basically divided into four areas:

1. Plessey programs.
2. Real-time Operating System supervisor in the SEL.
3. Modifications made to the existing Telescope™ 340 Software running on the central computer.
4. DETAIL telemetry compiler/utilities.

All software with the exception of the modifications made to Telescope™ 340 was built to run and be supported on the SEL computer to facilitate the standalone capacity of the preprocessor and the move toward a new distributed architecture at the ATS.

Descriptive Telemetry Acquisition and Input Language (DETAIL) is a compiler which interfaces to the system user in terms familiar to flight analysts and telemetry users. It produces a set-up file which consists of groups of object codes to load each of the boxes and computers with the format information, parameter lists, algorithms, coefficients and data descriptors required for specific aircraft tests. Written in FORTRAN 77+ the compiler accepts format descriptions and lists of active measurements from an Instrumentation file as well as lists of desired outputs (real-time, mag tape, DAC, etc.). Using keyword directed, free-format style, input is syntax checked and divided into intermediate tables. Patching lists, decommutator programs, MUX/ADC sampling programs, measurement algorithm processing lists, DAC assignments and data descriptions are all produced automatically by DETAIL. Included is the capability to support concurrent analog and digital processing, multi-syllable words, multiple asynchronous subcoms, super-commutation, in support of most IRIG compatible data formats.

Several utilities are also included such as a translator which converts source statements used for the old 1700 TELIN language to DETAIL source statements. The translator permits all old flight tapes described via TELIN to be played through the ATP using only those resources of DETAIL and the ATP which are pertinent.

The Real-time Operating System (RTOS) is an executive program which resides beneath the SEL's normal MPX Operating System RTOS and which directs the operation of the preprocessor in the real time mode where directives are received from and data transferred to the central computer. In standalone mode the same software is used except that

directives are input directly to the SEL and data is output to local computer compatible tapes. Upon request, RTOS supervises peripheral connection, downloads the decom and Plesseys with the specified Setup Files, and in real-time mode uploads the central computer with descriptions of all parameters which are to be transferred. The present command set allows such operations as loading boxes, dumping boxes, turning data on and off, turning computer tapes on and off and changing the assignment of DAC's and coefficient values while data is being transferred.

Programming in the Plesseys is supported by a cross-assembler written for the SEL. All supervisory programming, drivers and algorithms were developed by Grumman to specifically support the ATP. The overriding consideration was speed of execution, thus programming at the assembly level was indicated. Programs and algorithms are modularized permitting changes and additions with very little trouble.

Modifications to the Telescope™ 340 (TS340) Operating System on the central computer were necessary mainly to accommodate the HYPERchannel interface which was not used on the 1700 system. Since the same buffering strategy was used as in the older system, the changes required were at the I/O driver level and did not propogate very far upwards in the system. Several other areas were also changed in the initialization of the system but these were not time critical. Because of a difference in philosophy of the system where the CYBER now requests loading from the ATP rather than downloading to the preprocessor, changes were necessary in the commands given and ability to receive data descriptors from another machine.

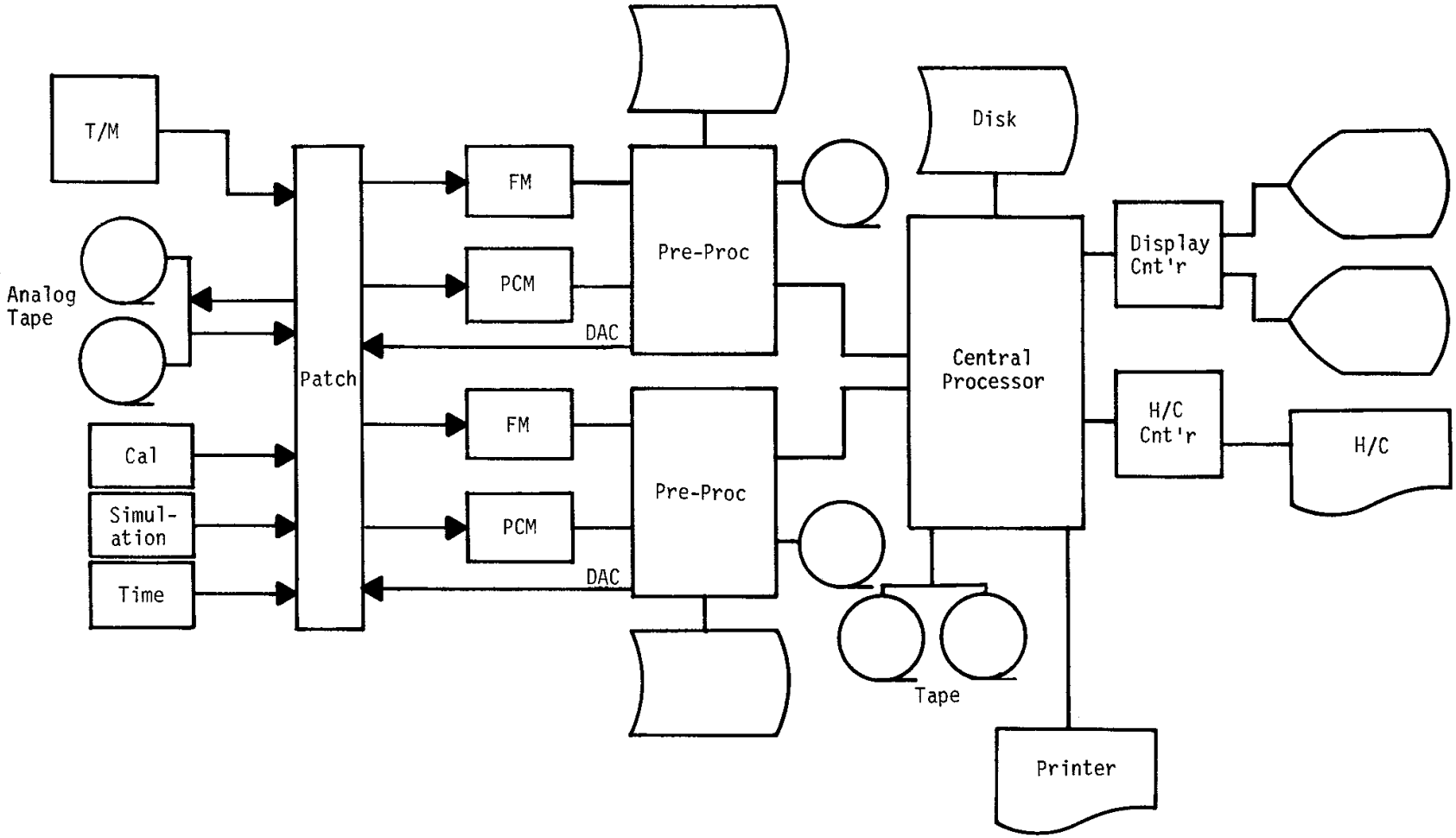
With the philosophical change of removing the central computer from the role of master in its relationship with the ATP a further step was taken away from 1700 emulation. Although the ATP still puts out data in formats compatible to the TS 340 system, the command processor, file system and compiler were all moved to the preprocessor machine.

ATP PERFORMANCE REPORT

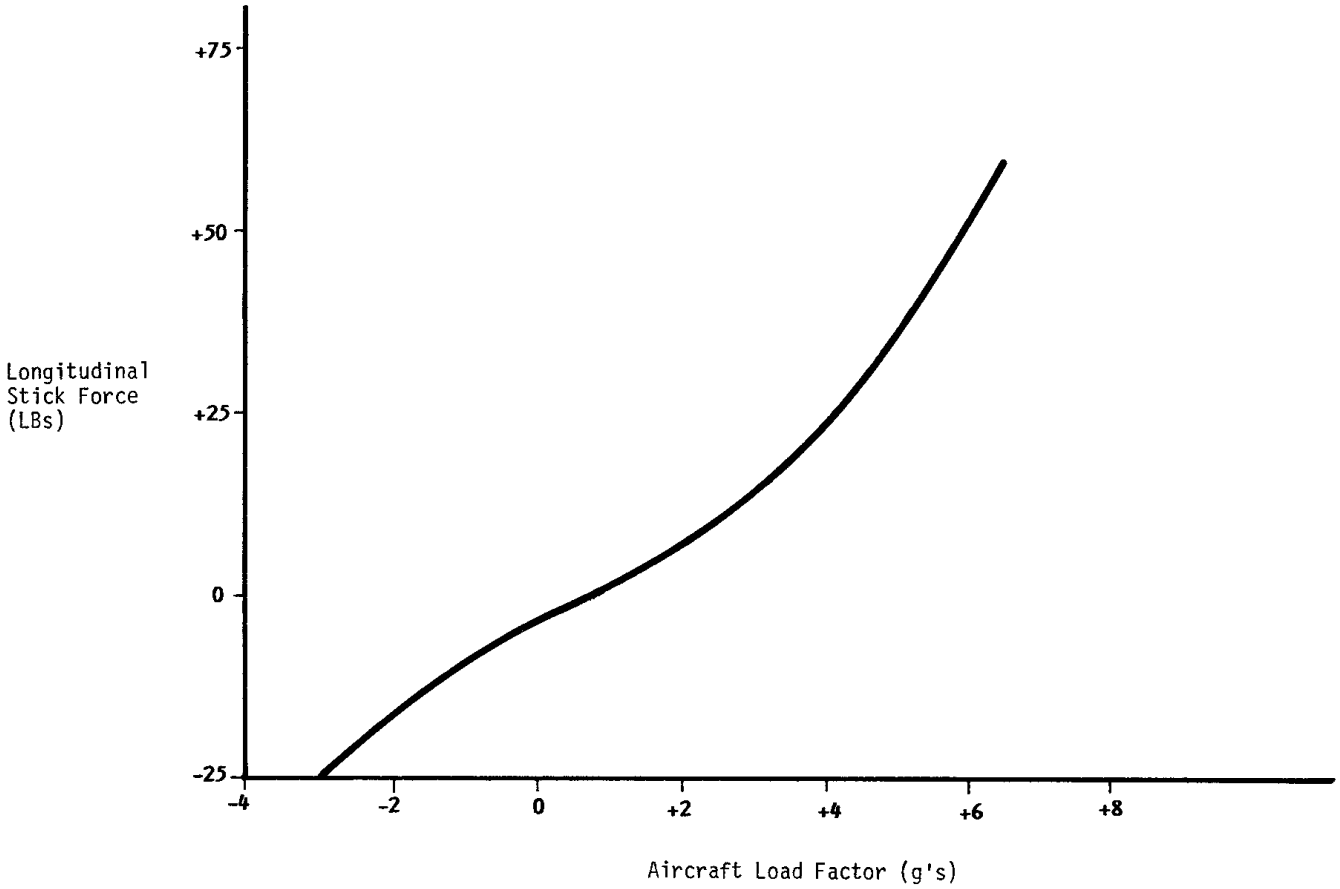
Acceptance testing prior to full integrtion into ATS included rigorous testing at design goal rates both on-line and standalone. The ATP achieved all performance goals and appears to have a healthy margin for future growth. The ATP project spanned 2½ years, was accepted into production status at the ATS in July, 1982 and has been successfully supporting all flight tests since that date. As had been directed and planned, the switchover from the 1700's to the ATP's was physically accomplished over a weekend with software compilation previously having been completed. The 1700's were left in place for 3 months until confidence in the ATP's permitted their removal.

The growth, expendability and modularity of the ATP design has already been proven with the addition of an aircraft fixed base flight simulator to the preprocessor. This project, begun even as the ATP was undergoing acceptance, utilizes the I/O capabilities of the Plesseys to accept analog data from cockpit controls and return analog data via DAC's and event registers. The simulator's all digital aircraft dynamic model is implemented on the SEL host computer.

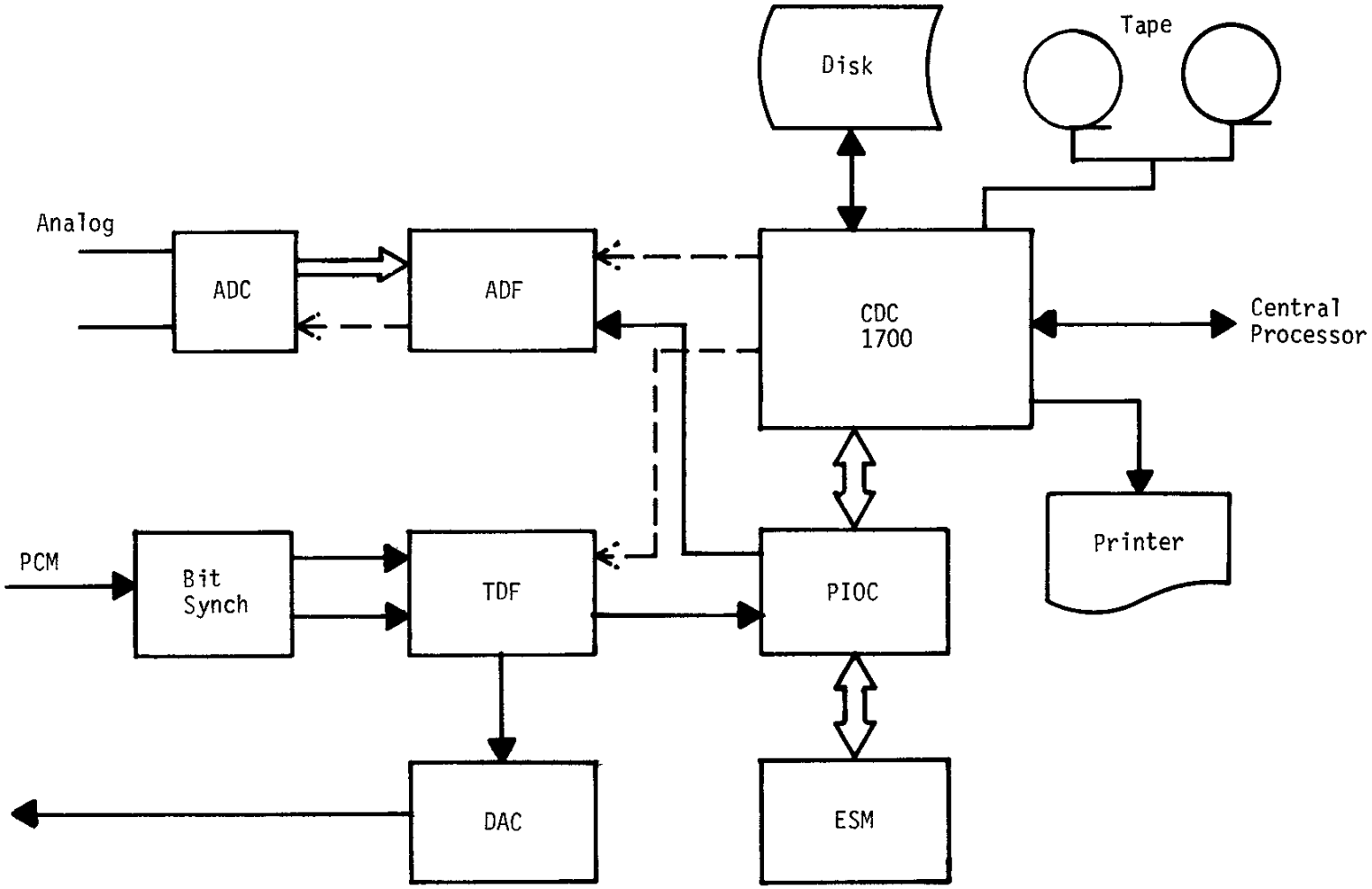
Because of the ATP flexibility it has been possible to design, implement and test a Fixed Base Simulator in 14 months. The system now is serving the Flight Test Community as well as Engineering at Grumman and is available to be changed from either a preprocessor to a simulator or vice versa simply by changing one patchpanel and several type-ins which change the software loads.



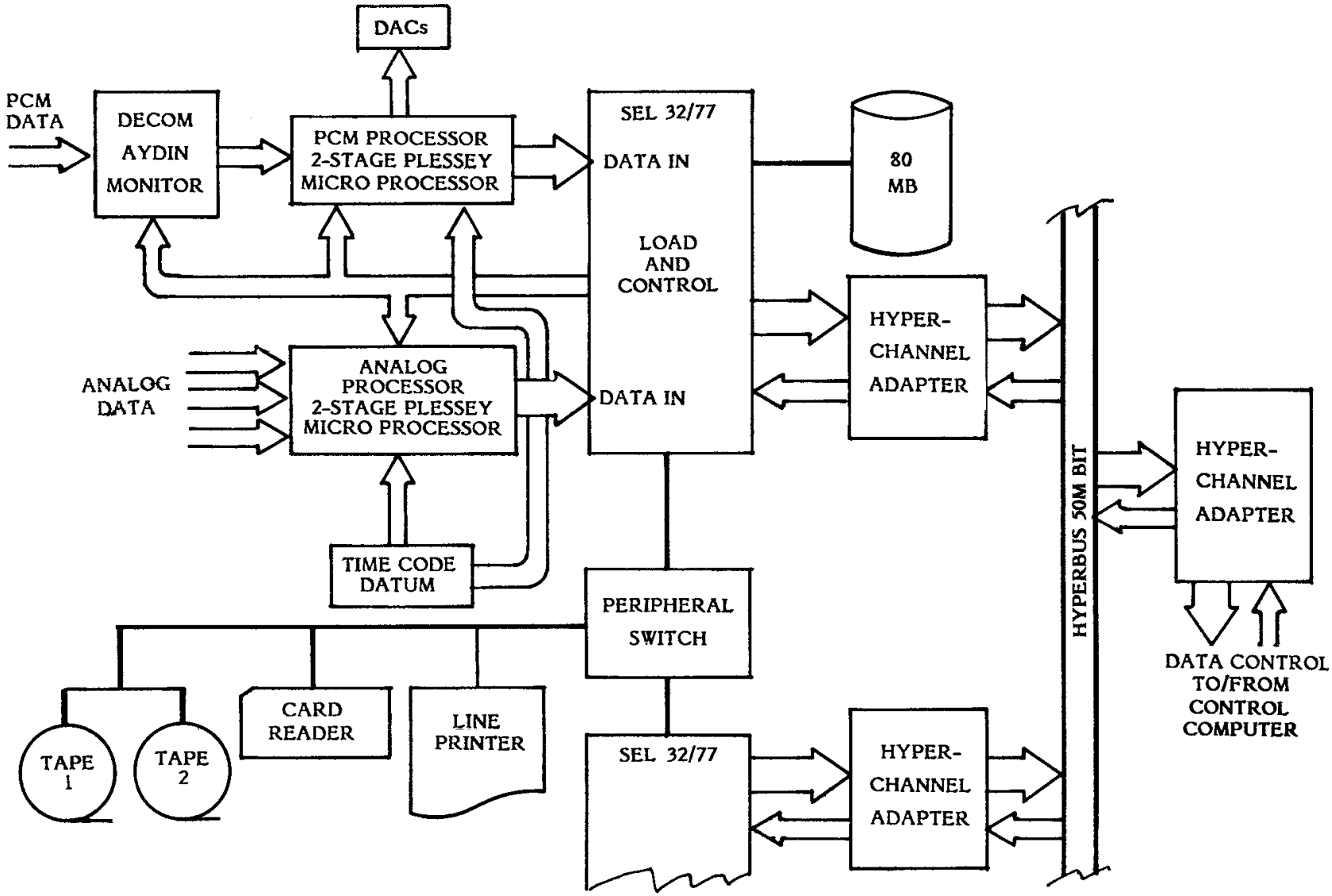
ATS OVERVIEW
FIGURE 1



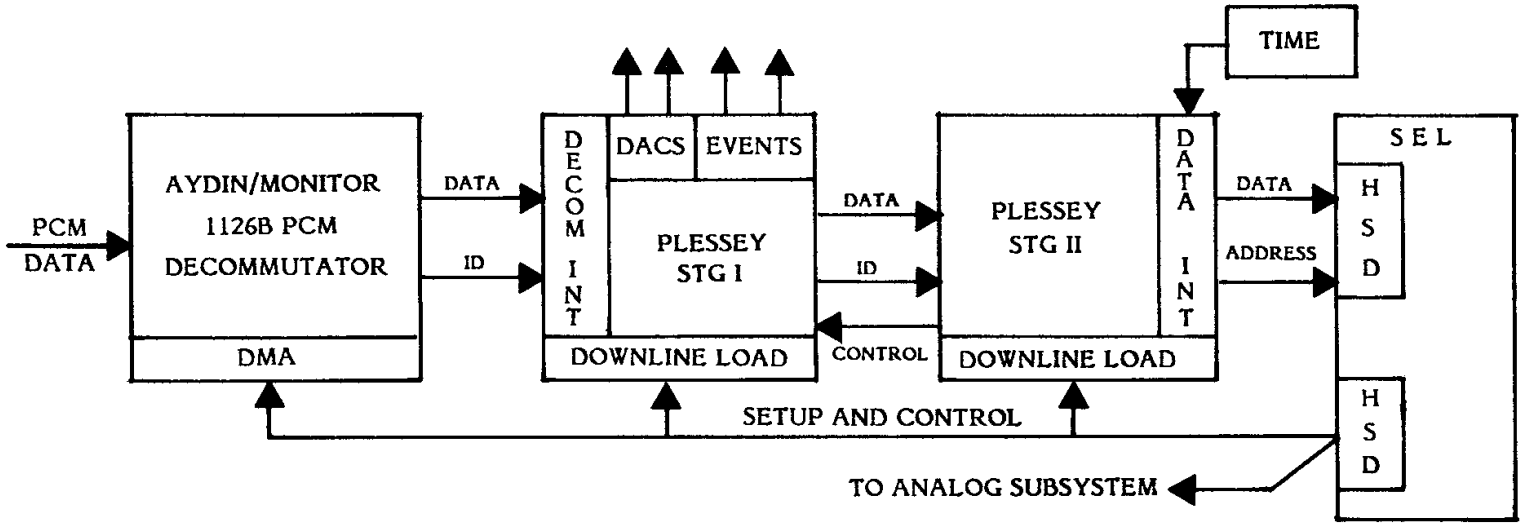
TYPICAL CROSS PLOT
FIGURE 2



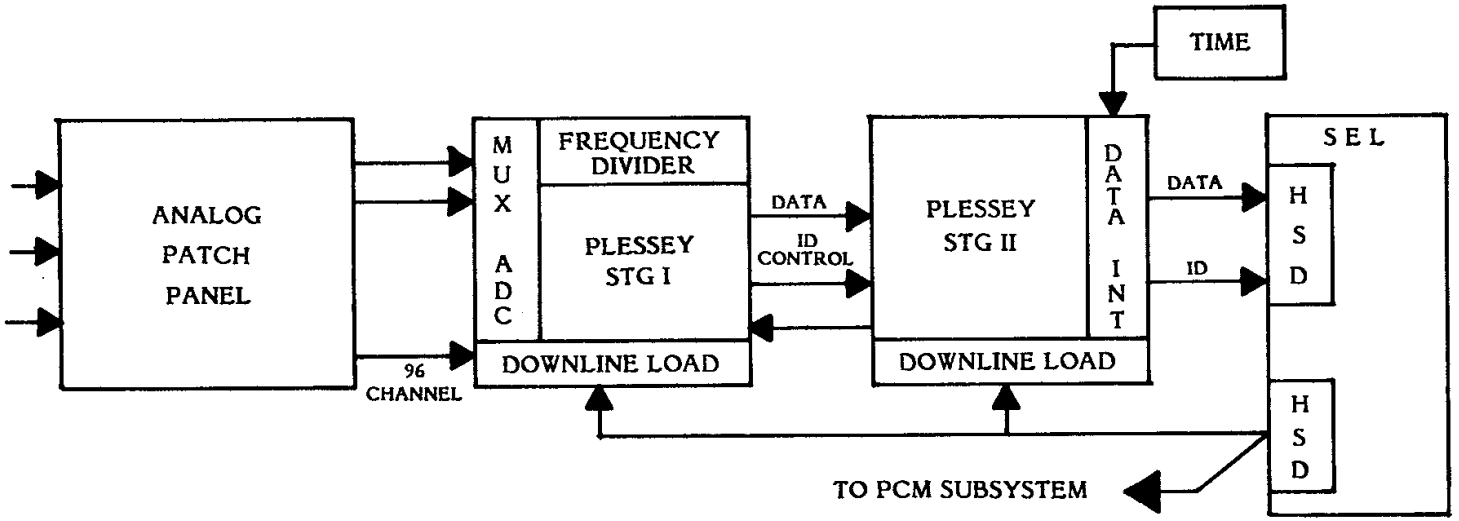
PRE-PROCESSOR
FIGURE 3



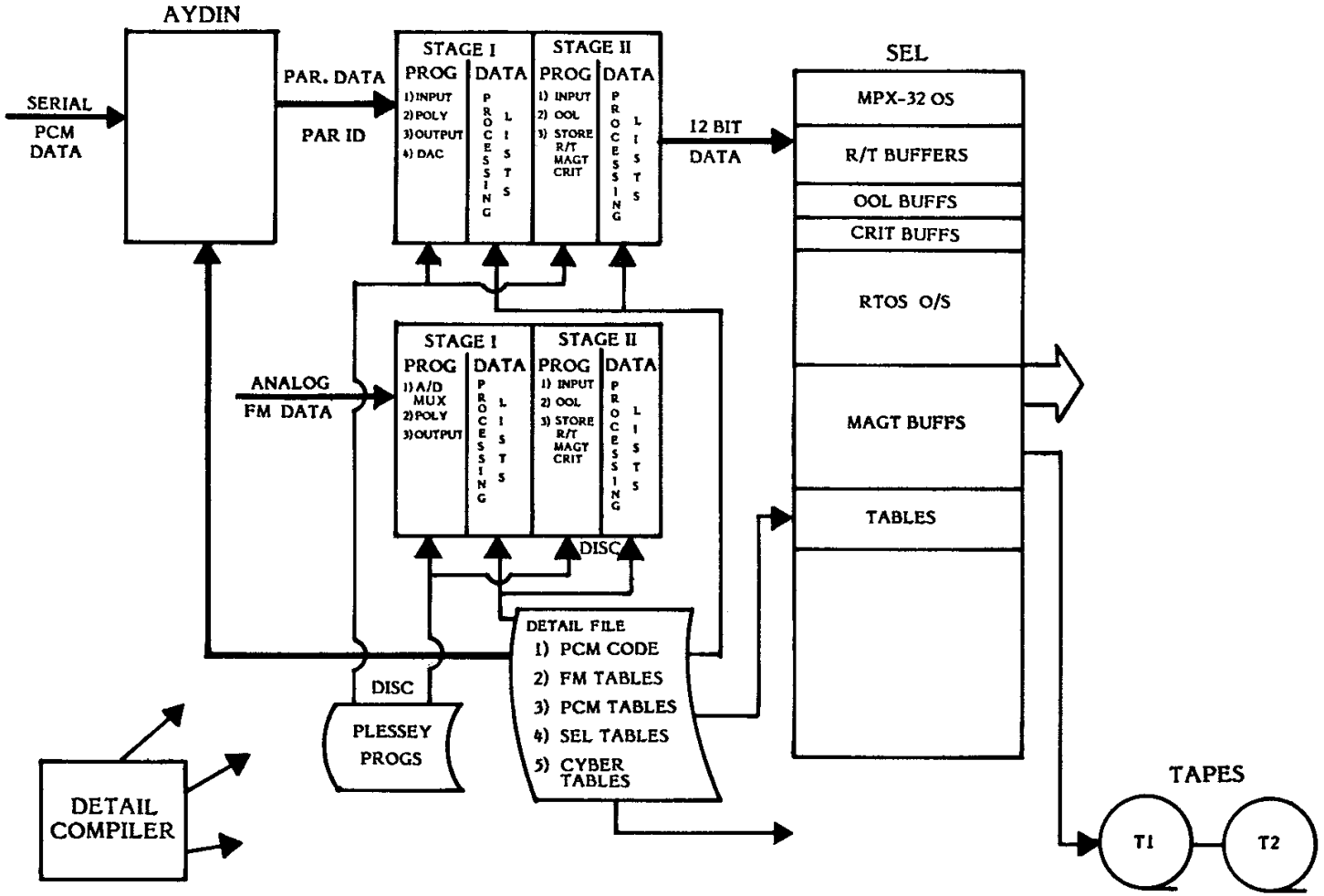
ATP BLOCK DIAGRAM
FIGURE 4



PCM SUBSYSTEM
FIGURE 5



ANALOG SUBSYSTEM
FIGURE 6



SOFTWARE SUBSYSTEM
FIGURE 7