# GREATER THAN 3 MHZ MULTICHANNEL A/D CONVERSION ON A SINGLE VME BOARD

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## ABSTRACT

A VME computer can be used to provide the basis for a telemetry data processing station. Using "off-the-shelf cards" the designer is able to build up a front end that meet several of the data processing requirements. The ease in interfacing to the VME bus also provides a convenient platform for the development of highly specialized interfaces requiring programmable control. The results are a low-cost high-performance system that is easily expandable as needs and/or technology grow.

Based on this strategy, the Physical Science Laboratory (PSL) at New Mexico State University developed a multichannel high-speed analog-to-digital converter (ADC) assembly on a single VME board.

The design approach used at PSL to develop the VME-based ADC is discussed in an effort to describe both developments in analog-to-digital conversion integrated circuits and the use of a VME CPU to control them for data processing purposes.

## INTRODUCTION

PSL developed and installed the Telemetry Processing System (TPS) at Holloman Air Force Base (HAFB), NM for processing data acquired from the Holloman High Speed Test Track. One of the requirements for the TPS was to provide a high-speed analog-to-digital conversion subassembly (ADS).

The ADS had to be capable of accepting up to ten simultaneous channels of analog data carrying frequencies of up to 64 kHz each with a channel sample rate of five samples per cycle, maximum 320 Ksamples per second per channel, for a total aggregate throughput of 3.2 Msamples per second. If only one channel of the ADS is utilized, a frequency response of 640 kHz or 3.2 Msamples per for a single channel

had to be possible. If any number of channels up to the ten channels of the ADS was utilized, the per channel frequency response and sample rate had to be programmable by the operator for sample rates less than 3.2 Msamples per second. Data also had to be available for real-time display at an aggregate rate of 100 Ksamples per second.

Recognizing the need for programmability and given the desire of the customer to have expansion capabilities over the long period of the system's life, the decision was made to develop a VME-based system that would meet the requirements.

## THEORY OF OPERATION

The ADS (see Figure 1) was developed to meet the requirements of the Analog-to-Digital section of the TPS. The ten analog data inputs come from the TPS patch panel into the ADS subassembly and enter the buffer boards. The buffer boards route the analog data to the two A/D boards. At user-selected rates (see Table 1), each channel of analog data is then converted to a 12-bit digital word. The output data from the discriminators, along with the appended 4-bit channel number, are then routed to the ACROAMATICS telemetry processing front end for storage or real-time display.

System operation commands are sent to the ADS from the DEC system computer. Data are packaged in frames that are 256 words wide. Frame synch is provided by having the frame synch bit in the first word of the frame set low. Additional header bits such as time tag are appended inside the ACROAMATICS front end. The user has the ability to select data rates (see Table 1) that are eight base two divisions of the maximum or aggregate data rate for the processing being used. The storage and real-time rates are mutually exclusive.

The DEC-based system software creates a frame map which ensures that all the samples occur at the right time. The algorithm is implemented as follows:

a) The operator, through the user interface, selects the rates from Table 1 at which each of the desired channels should be sampled.

b) The ADS program sorts the sample rates in order of magnitude.

c) The channels are then loaded into the map, starting with loading the channel requiring the highest sampling rate into the first word.

d) The channel with the next highest, or equally high, sample rate is started at the next available slot

e) The channels are loaded into slots repeatedly at the desired frequency (as an example, 800 Msamples would be every fourth word) until the frame boundary of 256 words is reached

f) This process is repeated until all of the channels have been loaded.

g) The DEC computer downloads 256 16-bit words to the VME CPU to later go to the A/D board. The word command contains the required bits to perform the conversion on the A/D board.

An example of how a frame map would look is presented here. Consider the following entries by the operator:

| CHANNEL NUMBER | SAMPLING RATE (Ksamples/sec) |
|---|---|
| 1 | 100 |
| 2 | 400 |
| 3 | 800 |
| 4 | 25 |
| 5 | 200 |
| 6 | 400 |
| 7 | 200 |
| 8 | 50 |
| 9 | 200 |
| 10 | 200 |

The resulting first 256 words (the second 256 words are identical) of the frame map can be seen in Table 2. Blank spaces indicate word blocks where a conversion is not required. Null data is not sent to the ACROAMATICS front end, but rather a conversion is skipped.

## SYSTEM DESCRIPTION

The high-speed A/D subassembly is based on a standard VME chassis which includes

a) a VME CPU board
b) a standard VME J1/P1 bus, with terminators
c) P2 connector plugs
d) two A/D boards
e) two buffer/interface boards
f) a linear +5 volt and a linear ±12 volt power supply

The CPU board ROM contains all the code necessary to allow it to act as a conduit for the system is DEC computer to operate the A/D boards. The commands to the CPU board are transmitted via an RS232 port on the front of the CPU board. The DEC system computer downloads to the CPU board the bit patterns required to set up the A/D boards. During the data conversion processing time, the CPU board is in an idle mode waiting for a stop command.

A standard VME J1/P1 backplane is used to interface the CPU to the two A/D PCBs and two buffer PCBs. Power to all of the boards in the chassis is supplied through the P1 backplane. P2 connector plugs are provided to interface the output of the A/D cards to a 37-pin sub-miniature D connector mounted on the rear of the VME chassis. From there, the parallel digital data go to the ACROAMATICS telemetry processing hardware. The A/D boards pass data by handshaking directly with the ACROAMATICS front end FIFOs.

The A/D boards consist of both an analog and a digital front end. The analog inputs are scaled, multiplexed, and then converted. The digital front end interfaces to the standard VME bus to receive setup commands from the CPU board. Upon CPU command, at the board frequency, the A/D board digitizes the user-selected analog inputs with 12-bit accuracy, appends the 4-bit channel number, and strobes the resulting 16-bit data into the ACROAMATICS front end FIFOs.

## DETAILED DESCRIPTION OF THE A/D BOARDS

For this paper, detailed description is limited to the A/D boards.

## VME BUS INTERFACE

The following VME bus signals on P1 are used to operate the A/D boards:

a) A01-A23 - Decoded to indicate that the CPU is talking to that board and also to provide addressing for the control RAM.

b) D00-Dl5 - Used to pass the control bits to the A/D board RAM.

c) DTACK, AS, DS0, DS1, WRITE, AM0-AM5 - These signals are used for VME bus for address and data validation.

## DIGITAL CONTROL CIRCUITRY

This section describes the digital control portion of the A/D board. Figure 2 is a block diagram of the A/D board digital section.

The digitization process on the board is controlled by a pattern of bits stored in the onboard RAM. With the rising edge of the board TTL clock (either 3.2 MHZ or 100 kHz), a new A/D cycle begins. On that rising edge the RAM outputs a new control bit pattern. The following circuitry makes up the digital circuits used to control the board command and timing operations. The purpose of this section of the board is to receive the logic patterns from the main computer, load them into onboard RAM and clock them to devices under RAM control upon receipt of the start command from the main computer. The bit pattern will then control the process of digitizing the analog data and appending the channel number for transfer to the ACROAMATICS front end for real-time display and/or storage. This circuit also has the capability to stop digitization operation on main computer command.

a) Control Bit Pattern - Each bit has a distinct control or data function on the board. D00 through D02 control the two 8:1 analog multiplexers. D03 controls the 2:1 analog multiplexer. D04 is low when a conversion is to be done on that clock cycle. D08 through D11 provide the channel number to be appended to the data. D12, when low, indicates the beginning of the frame.

b) Data Transfer Operation Control - Data is written from the CPU board to the onboard RAM by word transfer. The addresses going to the RAM are routed through two multiplexers. During data transfer operations, the flow line out of the DECODE PAL is set high so that the address multiplexers will feed the addresses from the VME bus to the RAM.

c) A/D Conversion Operation Control - All A/D conversion operations are controlled by the bit patterns from the RAM. During A/D conversion operations, the flow control line out of the DECODE PAL is set low so that the address multiplexers will feed the addresses from the 8-bit-wide counters bank to the RAM. These counters are clocked by the A/D timer clock, which runs at 3.2 MHZ for the storage HSAD board and 100 kHz for the real-time ADS board. When the conversion process is started, a START command is issued by the CPU board.

The RAM is loaded with 256 command words, with each of these 256 words corresponding to one word of a minor frame of ADS data. The A/D conversion circuitry continuously sequences through these 256 words.

## TIMING CONTROL

The two A/D boards are identical except in the area of timing. The storage data digitizer board uses a 3.2 MHZ TTL crystal oscillator. The real-time data digitizer board uses a 100 kHz TTL crystal oscillator. The combination of the oscillator output, some additional timing logic, and the D04 line out of the RAM being low (indicating a conversion is to take place on that clock cycle) cause the required convert signal to go to the A/D converter.

## ANALOG CIRCUITRY

The analog circuitry for the A/D board consists of gain adjustable buffer inputs, two 8:1 multiplexers, one 2:1 multiplexer, and an A/D converter.

a) Gain Adjust Resistors and Buffer Amplifiers - Each of the ten inputs from the buffer boards is first passed through a voltage divider network. Since most flash converters are only capable of digitizing inputs of around ±1.25 volts the typical input ranges of ±10 volts must be attenuated.

b) 8:1 Multiplexers - The first stage of multiplexing is done using high-speed 8:1 multiplexers. This is one of the key stages to the circuit. Multiplexers that can settle to less than 1% in under 300 nanoseconds have become available only recently. Only the first five channels of each multiplexer are used with the other inputs grounded in the HAFB/TPS application. This is due to the requirement for only ten channels. Expansion to allowing the board to take the inputs of sixteen channels is trivial. As detailed in the section on digital control circuitry, the RAM outputs a new decode pattern (D00-D02) to the multiplexers at the start of every clock cycle. Both multiplexers will have inputs selected even though ultimately only one will be digitized by the A/D.

c) 2:1 Multiplexer - The next stage of multiplexing is done using a wideband switched-input op amp. Each of the outputs of the 8:1 multiplexers is fed into the op amp with the feed from channels 1 through 5 going into the A input and the feed from channels 6 through 10 going into the B input. As detailed in the section on digital control circuitry, the RAM outputs a bit (D03) to the op amp at the start of every clock cycle. This enables either the A or B channel to go to the output and on to the A/D converter.

d) A 10 MHZ 12-bit A/D converter (a hybrid that contains all required sample and hold circuitry, etc.) - This is used to digitize the analog output of the 2:1 multiplexer. When a rising TTL edge is applied to the convert control input of

the A/D, a conversion process begins. After approximately 100 nanoseconds, the conversion is completed, and the 12-bits of data are latched into output buffers by the converter's data valid pulse. It is important to understand any pipeline delay within the converter to ensure that the data is tagged with the correct channel number. During board manufacturing any gain or offset pots associated with the converter should be set and locked. End-to-end signal offset and gain adjusts must be done on a per-channel basis. In the HAFB/TPS system the offset is done on the buffer and the gain adjust is done at the gain adjust resistors.

## DESIGN DISCUSSION

The most difficult part of this design is to ensure that the analog front end circuitry is settled to within the resolution range of the A/D. For a 12-bit converter, meaning 4096 counts, the input should ideally be settled to ±0.025%. For a 12-bit converter with a full scale of ± 1.25 volts, the bit weight is 610 microvolts per bit. The front end devices must be selected to meet the setting percent requirement. As previously stated, the storage board is designed to do a conversion at 3.2 MHZ, which is a sample every 312.5 nanoseconds. When the 6 nanosecond setup time of the A/D (time that the signal must be present and stable at the input to the A/D) is considered, this means that the front end analog hardware must be able to switch and settle in just over 300 nanoseconds. The speed of the front end parts used on the HAFB/TPS design based on data sheets specifications is as follows:

a) Input buffers - The input buffers are selected for their speed. The buffers used in the HAFB/TPS design are specified to settle a 1 volt step in about 20 nanoseconds.

b) Digital control circuitry - The relevant digital control circuitry is guaranteed in 31 nanoseconds.

c) 8:1 Multiplexers - The 8:1 multiplexers used were found to consistently settle to the required 0.025% in less than 150 nanoseconds.

d) 2:1 Multiplexer - The delay due to the settling to within 0.01% is 25 nanoseconds.

The resulting delay due to the analog front end becomes

| | |
|---|---|
| delay due to the input op amps | 20 ns |
| delay due to the 8:1 mux | 150 ns |
| delay due to the digital set up | 31 ns |

| | |
|---|---|
| delay due to the 2:1 mux | 25 ns |
| total propagation and settling | 226 ns |

This indicates that the analog front end should be able to switch in the channel desired and have it settled to the required 0.025% before the 300 nanoseconds has elapsed.

The HAFB ADS board design was under the constraint of allowing the user to select any channel to operate at any frequency, only limited by the bandwidth. This meant that adjoining channels of the same multiplexer could be selected for sequential output. Better performance from the additional settling time for the multiplexers could have been obtained by having the operator interface tell the operator where to plug the analog inputs into the patch panel. This would have ensured that the n + 1 channel selected would come from the other 8:1 multiplexer, resulting in more settling time. This would require the multiplexers to be addressed separately, but the, gain in performance would have been significant.

## CONCLUSION

Given today's high-speed analog integrated circuitry and the ease of interfacing to the VME bus, multichannel high-speed analog-to-digital conversion is obtainable on a single VME printed wiring assembly. Resolution specifications are not given here because of the difficulty in accurately measuring them; however, the system was easily demonstrated to provide resolution better than 1% even before the assistance of software calibration. In addition, the board could have operated at a higher data rate than that specified by the HAFB/TPS requirements.

## ACKNOWLEDGMENTS

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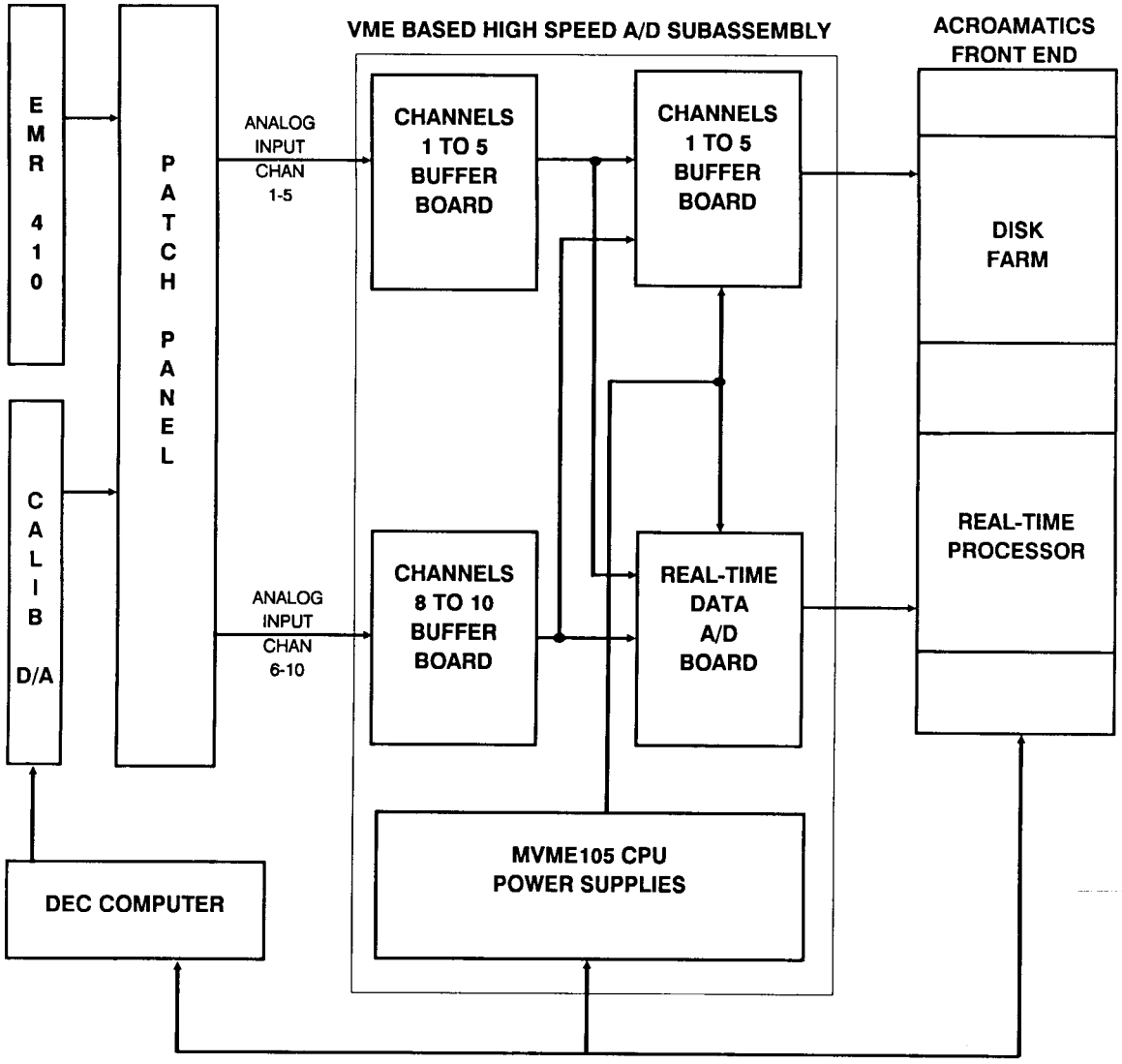
TABLE 1
SAMPLING RATE SELECTIONS

| STORAGE A/D BOARD (samples/sec) | REAL-TIME A/D BOARD (samples/sec) |
|---|---|
| 3,200,000 | 100,000 |
| 1,600,000 | 50,000 |
| 800,000 | 25,000 |
| 400,000 | 12,500 |
| 200,000 | 6,250 |
| 100,000 | 3,125 |
| 50,000 | 1562.5 |
| 25,000 | 781.25 |

TABLE 2
SAMPLE OF THE 256 WORDS OF AN ADS FRAME

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | 8 | 4 |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | 8 | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | 8 | 4 |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | 8 | |

| TABLE 2<br>SAMPLE OF THE 256 WORDS OF AN ADS FRAME | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | 1 | | |
| 3 | 2 | 6 | 10 | 3 | 5 | 7 | 9 | 3 | 2 | 6 | 10 | 3 | | | |




ADS SYSTEM BLOCK DIAGRAM
FIGURE 1

A/D BOARD DIGITAL BLOCK DIAGRAM

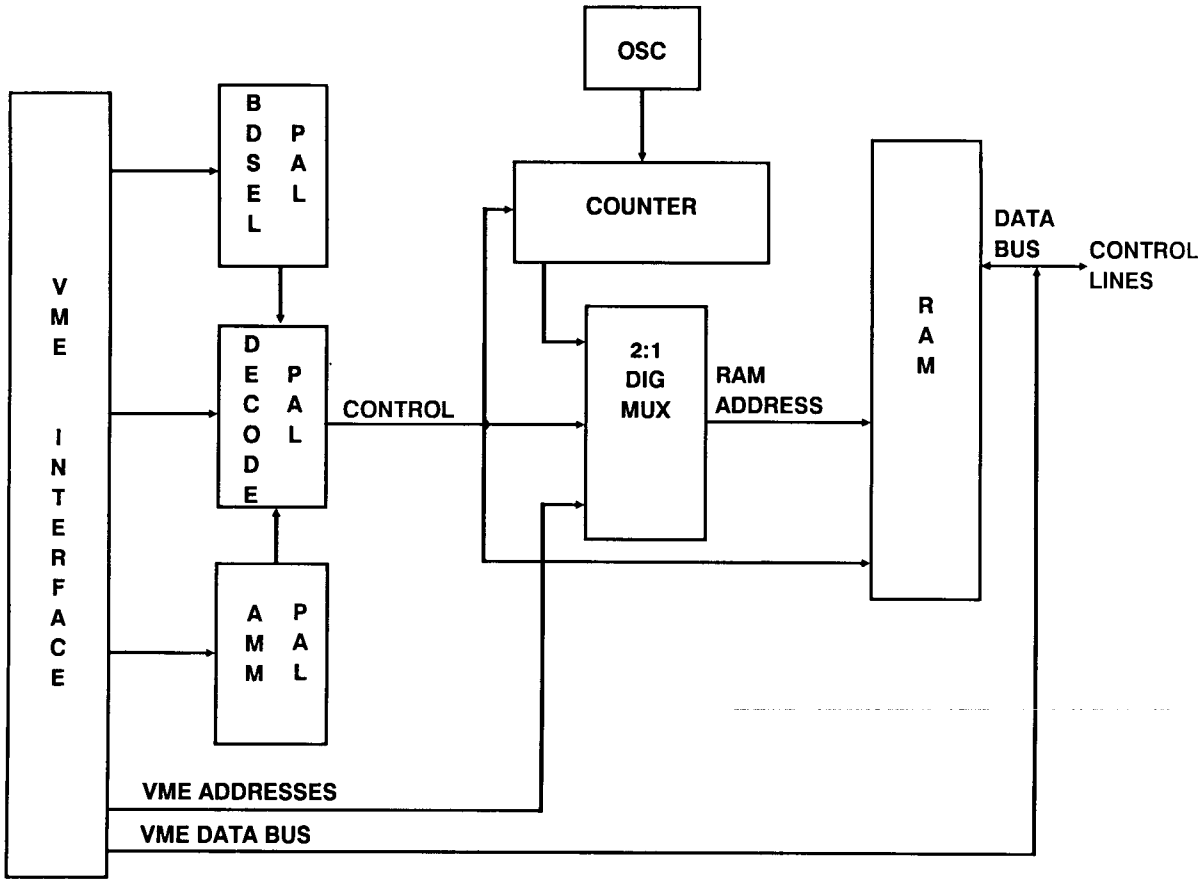
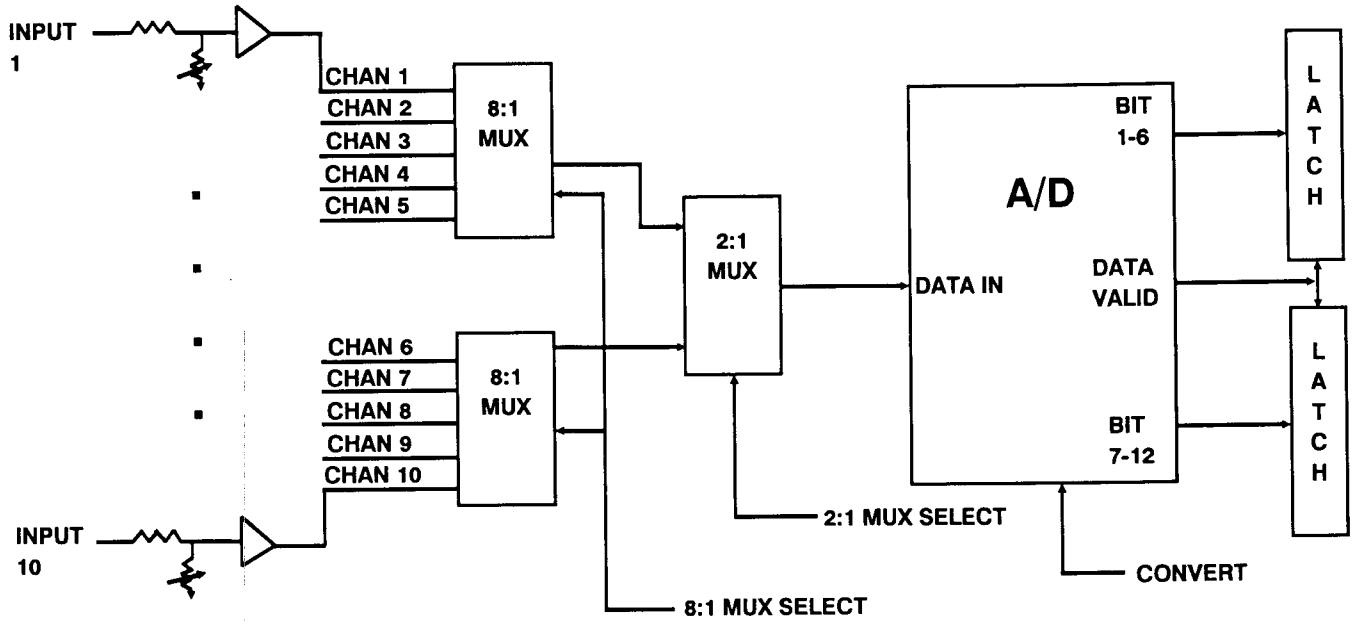



FIGURE 2




**A/D BOARD ANALOG BLOCK DIAGRAM**
**FIGURE 3**