THE REAL/STAR 2000: A HIGH PERFORMANCE MULTIPROCESSOR COMPUTER FOR TELEMETRY APPLICATIONS

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ABSTRACT

In this paper we describe the design of the REAL/STAR 2000 system, a high-performance real-time computer for telemetry applications. The REAL/STAR 2000 is a symmetric, tightly-coupled multiprocessor, optimized for real-time processing. The system provides a high level of scalability and flexibility by supporting three configurations: single, dual, and quad processor configurations, based on Motorola 88100 RISC processors. The system runs the multiprocessor REAL/IX operating system, a real-time implementation of the AT&T UNIX System V. It compiles with BCS and OCS standards, meets the POSIX 1003.1 standard, and has the current functionality of the emerging POSIX 1003.4 real-time standard. The REAL/STAR 2000 promotes an open system approach to real-time computing by supporting major industry standards. Benchmark results are also presented in the paper.

Key words: Real-time architecture, Tightly-coupled multiprocessor, RISC-based architecture, Multiprocessor real-time UNIX operating system.

INTRODUCTION

The heart of a modern ground-based telemetry system is a high-performance real-time data processing, data management, data analysis, and engineering interfaces computer system. One of the characteristics of these systems is an increased demand for computer processing power, which can be achieved by the introduction of multiprocessor architectures [1, 2, 3].

Multiprocessor architectures can improve the speed of computation; however, they may or may not be optimized for real-time processing. In real-time, in order to meet time-critical requirements, a system must be based on an architecture that:

- allows tasks to be scheduled on a fixed-priority basis,
- provides mechanisms for intertask communication and synchronization,
- provides high reliability,
- provides predictable execution time, low interrupt latency, and
- supplies high-computational performance.

The REAL/STAR 2000 is a symmetrical, tightly-coupled multiprocessor, which meets these requirements, and is optimized for real-time computing. It includes RISC CPU technology, open system architecture, high-speed memory, real-time system software, and a high-speed process I/O subsystem. The REAL/STAR 2000 system is based on the open system philosophy by supporting industry standards, such as the REAL/IX operating system, a real-time implementation of the UNIX System V Operating system, and standard buses and interfaces, such as VMEbus, SCSI, Ethernet, and others. By incorporating industry standards, the system enables users to take advantage of the latest technological developments while maintaining compatibility among diverse systems.

Besides high computational performance, the REAL/STAR 2000 system also provides deterministic and fast response time, fast task switching, low interrupt latency, and high real-time I/O throughput.

The REAL/STAR 2000 system meets the requirements of time-critical applications in real-time data acquisition and control, government, aerospace, communications, process control, and factory automation markets.

SYSTEM ARCHITECTURE

The REAL/STAR 2000 system is a tightly-coupled, symmetric multiprocessor using Motorola's 88100 RISC technology. The system supports three configurations: single, dual, and quad processor configurations. The quad processor system architecture is shown in Figure 1.

The base system consists of three standard VME modules: main logic board, memory board, and system controller board, interconnected through a high-speed local bus. The main logic board consists of one, two, or four 25 MHZ 88100 RISC processors and eight MC88200 Cache/Memory Management Units (CMMU), integrated into a HYPER-module, and the control logic required for the system bus. The 88100 processors also integrate integer and floating-point operations. The CMMU chips support tightly-coupled multiprocessing functions by providing a cache coherence protocol. In this way, all eight caches (each of 16 KB size) contain a coherent image of their shared data on the system bus. For the fastest operation, the system supports

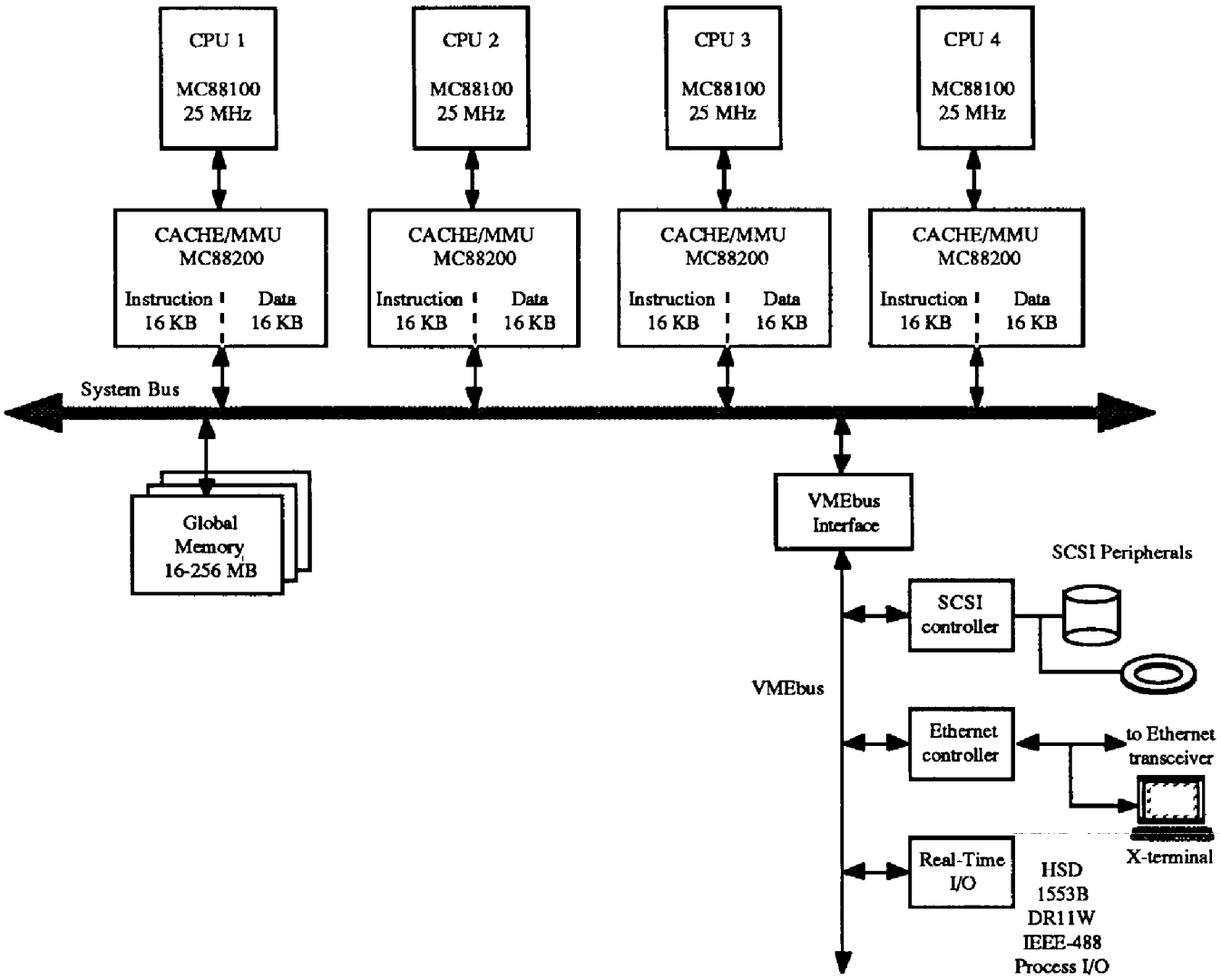

Figure 1 - The architecture of the quad processor REAL/STAR 2000 system

the copy back algorithm for maintaining the cache coherence. The memory board uses dynamic RAMs offering a capacity of from 16 MB to 64 MB. The system can be expanded up to six boards including three additional memory boards, which provides the maximum memory capacity of 256 MB.

The system controller board contains the VMEbus interface, system controller functions, and other facilities, including those commonly required for a computer operating in a VME bus environment. It also includes two RS-232C communication ports.

All local interrupts to the CPUs are controlled by logic on the system controller board. A multiprocessor interrupt controller enables any of 25 interrupt sources to be directed

to any of four processors. The availability of multiple processors allow the acceptance of interrupts and the scheduling processes in parallel.

The system is optimized to support I/O operations on the standard VMEbus and supports a number of I/O controllers and high-speed process I/O subsystems. The I/O controllers supported include the DR11W, the IEEE-388, the HSD, the external interrupt expander, and the 1553 Avionics bus. It also provides an interface to high-speed process I/O subsystems, such as Computer Products' IOBC and G2, and Tustin high-speed data acquisition subsystem as well as an interface to Modicon's Programmable Logic Controllers via MODBUS+. The VME interfaces are implemented via a fully preemptible kernel for maximum performance.

The scalability of the REAL/STAR 2000 system is provided by the HYPERmodule, which contains one, two, or four CPU clusters, as shown in Figure 2. Each cluster has a single CPU and from 32 KB to 128 KB of cache memory. The HYPERmodule connects to the main logic board via a multiplexed Mbus interface.

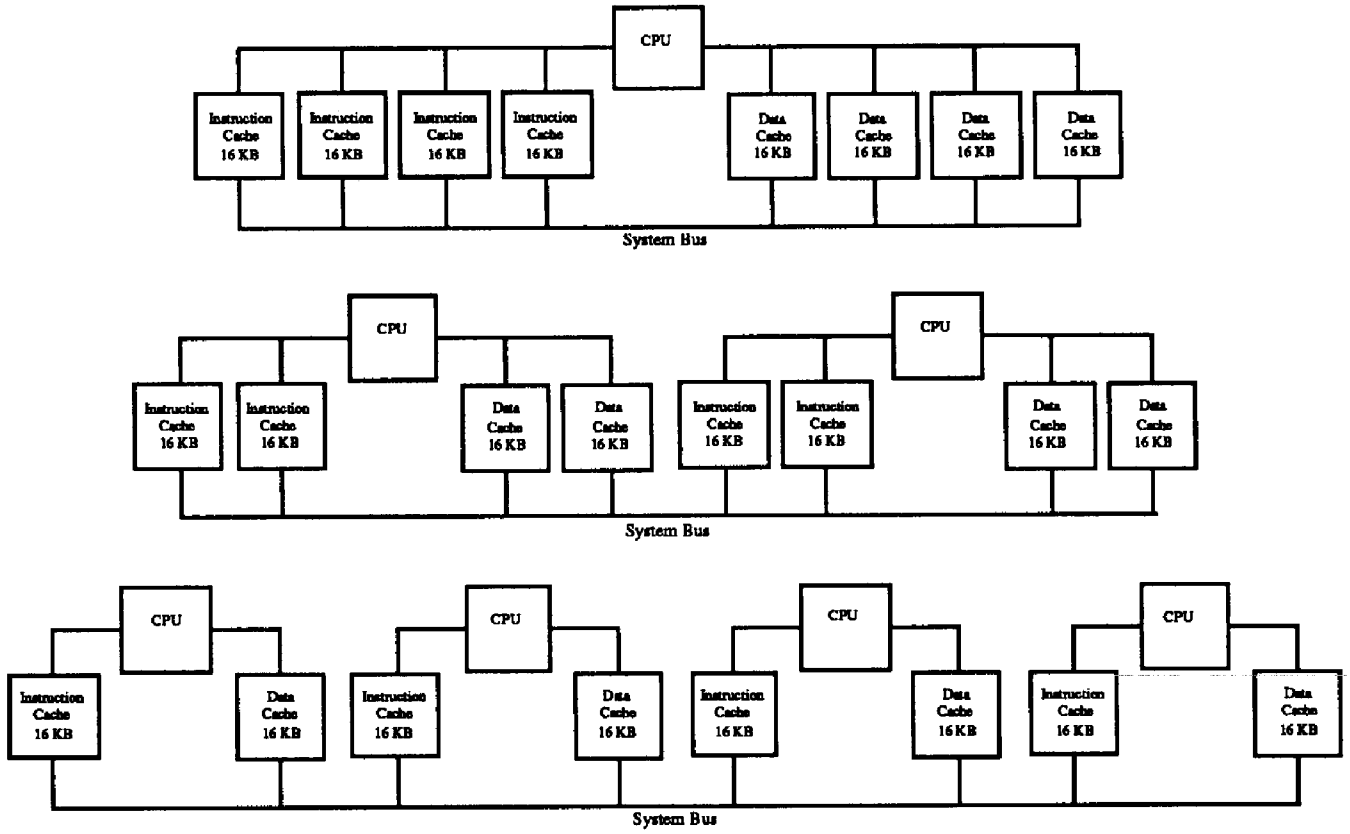

Figure 2 - The scalability of the REAL/STAR 2000: single, dual, and quad processor configurations

MULTIPROCESSOR REAL/IX OPERATING SYSTEM

The UNIX System V operating system has become a standard operating system gaining rapid acceptance because of its superior flexibility, portability, and large number of support tools. However, the UNIX operating system was originally designed for multitasking and time-sharing, and therefore the standard UNIX operating system does not have an adequate response time and the data throughput needed to support most real-time applications.

Many attempts have been made to adapt the UNIX kernel to provide a real-time environment [4]. These real-time UNIX systems have been considered for telemetry applications [5, 6, 7].

The REAL/STAR 2000 runs the multiprocessor REAL/IX operating system, which is MODCOMP's real-time enhancement of the AT&T UNIX System V. The REAL/IX operating system incorporates all the benefits inherent in the UNIX System V operating system while providing real-time performance. The REAL/IX operating system provides full kernel preemption, enhanced task scheduling, a variety of interprocess communication facilities, a fast file system, and enhanced I/O subsystem capabilities. It delivers the predictable and deterministic response required by real-time applications. A single copy of the multiprocessing REAL/IX operating system resides in global memory and provides total operational control over all processing within the system. The multiprocessing REAL/IX operating system includes key features such as tightly-coupled, symmetric multiprocessing with load balancing, and a multiprocess-threaded kernel.

A standard single process-threaded UNIX operating system does not make full use of a multiprocessor because UNIX allows only one thread of control at a time. Because standard UNIX is single threaded, most often UNIX -based multiprocessor systems are set up in master/slave configuration.

The multiprocessing REAL/IX operating system, designed to comply with BCS and OCS standards, meets the POSIX 1003.1 standard, and has the current functionality of the emerging POSIX 1003.4 real-time standard. This allows the portability of applications with real-time requirements.

Other features of the REAL/IX operating system include support for priority-based process scheduling and disk I/O scheduling, asynchronous disk I/O operations, buffer cache bypass and write-through for data integrity, enhanced memory management facilities which enable a process to be locked into memory, directly connected interrupts and common event notification capabilities. In addition to the standard

interprocess communication facilities, such as signals, messages, semaphores, and shared memory, the REAL/IX operating system supports a fast binary semaphore mechanism. The binary semaphores reduce system call overhead, allowing several processes to communicate without restricting real-time performance.

SOFTWARE TOOLS

The REAL/STAR 2000 system supports a full range of software tools as well as a specialized application generator. The full complement of programming languages for development of real-time applications is provided with General Language System (GLS). GLS features the ANSI C, FORTRAN 77, and Pascal programming languages. In addition, GLS provides a symbolic debugger for program testing and debugging. The REAL/VU Graphical Environment, a real-time graphical user interface, is also supported by all REAL/STAR 2000 systems. The REAL/VU Graphical Environment software consists of the X Window System, version 11.4 and the OSF/Motif User Environment, version 1.1.

Additional software tools available for the REAL/STAR 2000 system are the Ada programming environment, industry standard relational database management systems such as Informix and Oracle, and an interface to local area networks using either TCP/IP or DECNET protocols. The REAL/STAR 2000 system also supports the PACE/IX Process Automation and Control Executive. PACE/IX is a powerful application generator tool and man/machine interface used for development of data acquisition and process control applications.

PERFORMANCE EVALUATION

A number of benchmarks were run on the REAL/STAR 2000 system in order to assure that the system provides very high overall system performance, which balances three key features needed for time-critical applications: (1) computational speed, (2) interrupt handling, and (3) I/O throughput. A summary of results is given here, while detailed benchmark results and their description are presented in [8].

Standard Computational Benchmarks

The results of the standard computational benchmarks (Whetstone, Dhrystone and Linpack) for the REAL/STAR 2000 systems are presented in Table 1.

Note that in the case of the Whetstone and Dhrystone, the aggregate performance increase is practically linear with the addition of two or four processors. However, in the case of the Linpack, the performance increase is not linear. For a dual-processor

system, the speed-up is 1.85, while for the quad processor system, the speedup is 2.76. The reason for this is that both the Whetstone and Dhrystone fit into the cache memory, while the Linpack uses the large data arrays which do not fit into the cache memory.

Table 1
Standard Computational Benchmarks

	Single-system 1 x 88100 25 MHz	Dual-system 2 x 88100 25 MHz	Quad system 4 x 88100 25 MHz
WHETSTONE [MWhet]			
Single precision	21.3	42.4	85.7
Double precision	11.2	22.0	44.0
DHRYSTONE [Dhry/sec]			
With registers	49,586	99,140	198,590
LINPACK [MFlops]			
Single precision	4.85	9.02	13.40
Double precision	2.45	4.69	6.48

SPEC Benchmark

The SPEC Benchmark Suite provides a more objective speed rating (SPECmark) than the "old" MIPS rating. The SPEC also introduced the SPECthruput metric, which is an enhanced SPECmark, prorated according to the number of CPUs in the system. The SPEC result for the single processor REAL/STAR 2000 system is shown in Figure 3. The obtained SPECthruput for the quad processor REAL/STAR system is 4 @ 9.2, which gives 36.8 aggregate thruput [1].

Single-Parameter Real-Time Metrics

Single-parameter real-time metrics are typically concerned with priority interrupts and scheduling, which significantly impact real-time system responsiveness. The following seven matrices are used: task switching time, preemption time, interrupt latency time, semaphore shuffling time, deadlock breaking time, intertask message latency time, and process dispatch latency time.

Benchmark	SPEC Reference Time VAX 11/780 [seconds]	REAL/STAR 2000	
		Time [seconds]	SPEC ratio
gcc	1,482	88.8	16.7
expresso	2,266	143.3	15.8
spice 2g6	23,951	1934.9	12.4
doduc	1,863	190.4	9.8
nasa 7	20,093	1344.8	14.9
li	6,206	321.1	19.3
eqntott	1,101	66.2	16.5
matrix300	4,525	263.0	17.2
fpppp	3,038	209.8	14.5
tomcatv	2,649	237.7	11.1
SPECmark (Geometric Mean)			14.5

MODCOMP
REAL/STAR 2000
Single Processor System

HARDWARE

CPU:	MC88100, 25 MHz
Number of CPUs:	1
Cache size per CPU:	64 KB data/64 KB instructions
Memory:	16 MB
Disk Subsystem:	SCSI, 2 x 300 MB
Network Interface:	Ethernet

SOFTWARE

O/S type:	REAL/IX C.0
Compilers:	GLS C, GLS FORTRAN
Other software:	None

SYSTEM

Tuning parameters:	None
Background load:	None
System state:	Multi-User

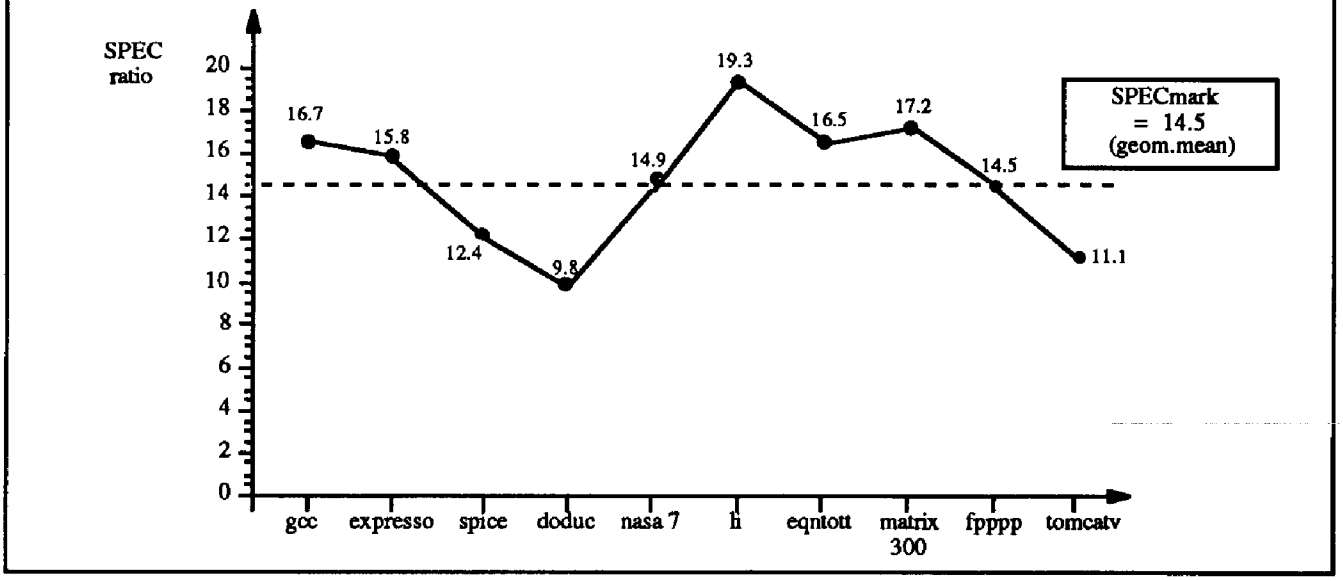

Figure 3 - SPECresults for the single processor REAL/STAR 2000 system

The definition of these metrics are given in [4, 9]. The results are shown in Table 2 and Figure 4.

Table 2
Single-Parameter Real-Time Metrics

Metrics	Task Switch Time [μs]	Preemption Time [μs]	Interrupt Latency Time [μs]	Semaphore Shuffle Time [μs]	Deadlock Break Time [μs]	Intertask Message Latency Time [μs]
REAL/STAR 2000	16	80	20-55	22	325	306

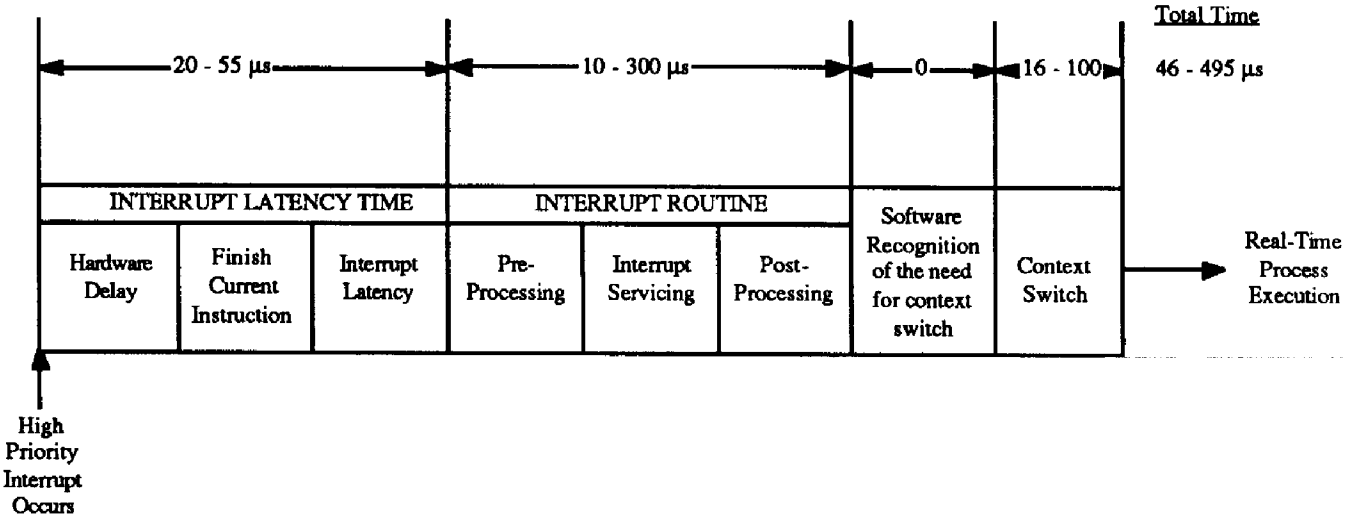

Figure 4 - Process dispatch latency time for the REAL/STAR 2000 system

Process dispatch latency time, which is often referred to as wall clock time is defined as the time it takes to transfer control from a lower priority to a higher priority process as a consequence of an external event. Figure 4 presents the range (the best and worst case) for the process dispatch latency time for the REAL/STAR 2000 system.

The worst case time is about 10 times higher than the best case time. The main reason for this is the existence of the cache memory. When an interrupt occurs and the corresponding interrupt response is not in the cache, additional time is required to update the cache and bring the interrupt routine into the cache. In the REAL/STAR 2000 systems with two and four 88100 processors, a processor can be assigned to handle interrupts, and consequently, interrupt routines can often be found in the cache memory. This will significantly reduce the process dispatch latency time.

The REAL/STAR 2000 system provides efficient and fast interrupt handling capabilities. The maximum number of interrupts that a single processor system can handle is 10,000 interrupts per second. The interrupt handling capability increases linearly with the addition of two and four processors.

The REAL/STAR 2000 system provides extremely fast intertask communication and synchronization facilities. The lock/unlock semaphore operations take only 2.7 microseconds using the Turbo™ (binary) semaphores, and 60.7 microseconds using AT&T System V semaphores. The average number of messages/sec transferred using pipes, FIFOs, and messages ranges from 1000 to 7500 messages/sec.

The REAL/STAR 2000 system supports asynchronous I/O operations, wherein a process can initiate an I/o operation, and then continue execution while the I/O operation is performed concurrently.

APPLICATION IN TELEMETRY

The REAL/STAR 2000 system has the flexibility and the power to handle various requirements within the range site. Figure 5 illustrates a typical telemetry processing application within an aerospace test range. The REAL/STAR 2000 system is receiving high-speed composite data streams from the front-end gear, and is displaying and archiving this data in real-time.

This open system solution provides a combined development and run-time environment which fully adheres to open systems standards, thereby reducing development complexity and costs. Often other solutions are “open” in the development environment, but offer reduced standards – conformance in the run-time portions of their systems.

The REAL/STAR 2000 computational power allows room for application growth even in today’s demanding telemetry and range applications.

The REAL/STAR 2000 also meets or exceeds the stringent requirements for interrupt handling and process dispatch latency times. I/O performance is a key requirement for telemetry and range applications and the REAL/STAR 2000 system meets this requirement through the high-performance I/O subsystem within the REAL/IX operating system.

The REAL/STAR 2000 provides the major connectivity interfaces and the real-time device drivers, incorporated into the REAL/IX operating system, for those interfaces.

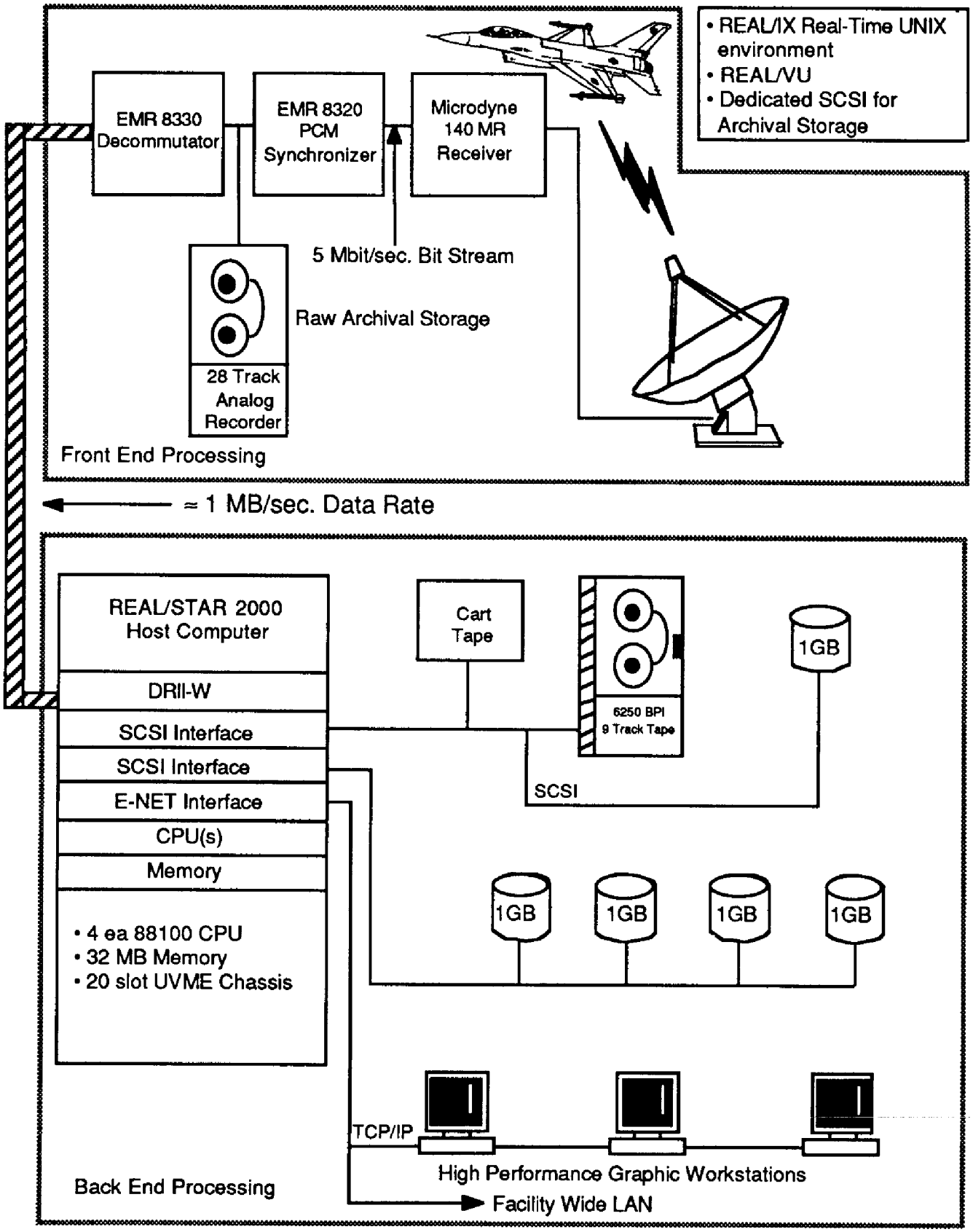

Figure 5 - Telemetry processing application using the REAL/STAR 2000 system

CONCLUSIONS

The REAL/STAR 2000 multiprocessor system is well suited for a number of time-critical and I/O intensive applications. It provides very high overall system performance, which balances three key real-time features: computational speed, interrupt handling, and I/O throughput. The REAL/STAR 2000 is based upon an open systems computer concept which uses off-the-shelf standard microprocessors (a standard multiprocessor real-time UNIX operating system, the REAL/IX operating system), standard communication protocols, and standard interface buses.

ACKNOWLEDGEMENTS

Many individuals were involved in designing the REAL/STAR 2000 system. Those who contributed significantly include: Dan Grostick, Jim Houston, Hagai Ohel, Joel Wagner, and Bob Sanford. We would like to thank those individuals who were actively involved in evaluating and benchmarking the REAL/STAR 2000 system: Abdulazeez Boujarwah, Damodar Kamath, Michael McCarty, and Ramadass Sureswaran. The authors also wish to thank Ms. Terri Stettner for her contribution to the production of this manuscript.

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