THE USE OF HIGH-SPEED DIGITAL TAPE RECORDERS AS COMPUTER PERIPHERALS

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ABSTRACT

While the scientific press brims with descriptions of state-of-the-art projects using the latest technology to produce huge amounts of data, little attention is given to the system requirements that result when Terabytes of data are generated. This paper examines the affect on telemetry, and replay/analysis systems and the necessary integration of high-speed digital tape recorders in such systems. Specifically, it considers how the tape recorder interfaces to the computer system, how the interface is integrated into the computer's I/O architecture, and how much the user can expect in performance.

THE DATA DELUGE

Users wage daily battle against the data deluge. Consider the problems NASA faces. The space agency estimates that the recently launched Hubble Space Telescope can produce a continuous 1 Mbit/sec flow of data (86 Gbit/day or 30 Tbit/year). When one considers that this is the product of only one project, it is easy to understand why NASA now has more than 48 Tbits (6 TBytes) of data in storage and why it expects the amount of new data to double every two years.

NASA is not alone. In high-end installations around the world, computer systems regularly confront greater quantities of data for processing and storage at higher data rates. Computer designs must provide a way to record continuous high-speed data streams. They must provide fast access to stored data for analysis. Computer designs must also provide compact and robust long-term storage. With this perspective, the role of high-performance digital tape recorders and their use in integrated systems will be examined.

CURRENT DIGITAL TAPE RECORDER CAPABILITIES

Digital tape recorder manufacturers have developed units to meet user requirements, however, the integration of high-performance recorders into computer systems has lagged behind.

Available digital tape recorders range from 9-track units to the latest 19mm devices. The low-end devices have a large installed base. While they offer low areal storage capacity at a low I/0 rate, they are still the most popular units on the market. At the mid-range are devices like the Metrum VLDS, a VHS-based tape recorder. The VLDS supports a sustained I/O rate of 4 MBytes/sec and has more storage capacity than a 9-track unit. A VHS cartridge for the VLDS holds more than 5 GBytes of data. Although the VLDS represents the mid-range in tape recorder performance, many computer system interfaces and I/O architectures cannot support the 4 MBytes/sec sustained I/O rate.

At the high-end, 19mm tape recorders can capture data at a faster I/O rate. These recorders also have a large storage capacity. Examples are the AMPEX DCRSi and the Sony DIR-1000 ID-1 recorder. These devices operate at sustained I/O rates of more than 10 MBytes/sec and store tens of GBytes on a single cartridge. At this leading edge of recorder technology, there are few computer interfaces that can support the sustained I/O rates.

Figure 1 compares some of the different digital tape recorders.

Example Digital Tape Recorders

	RECORDER	I/O RATE	CAPACITY
Low-end	9-Track	1 MB/sec	140 MB
	EXABYTE 8 mm	500 KB/sec	2 GB
Mid-range	IBM 3480	3.5 MB/sec	800MB
	METRUM VLDS	4 MB/sec	5 GB
High-end	AMPEX DCRSi	13.3 MB/sec	45 GB
	METRUM RSR-260	18.8 MB/sec	100 GB
	SONY DIR-1000	32 MB/sec	96 GB

Figure 1

APPLICATIONS

To illustrate how high-speed digital tape recorders can enhance a computer system solution and increase end-user productivity, two applications will be discussed; telemetry, and data replay and analysis.

Telemetry

Telemetry applications use digital tape recorders for saving data from one or more sources. In telemetry systems, one or more Analog/Digital (A/D) converters digitize

telemetry signals from receivers. The digitized data may be saved, and all or part of it must be processed. The processed data may be saved and/or displayed. Figure 2 shows a functional diagram of a digital telemetry system.

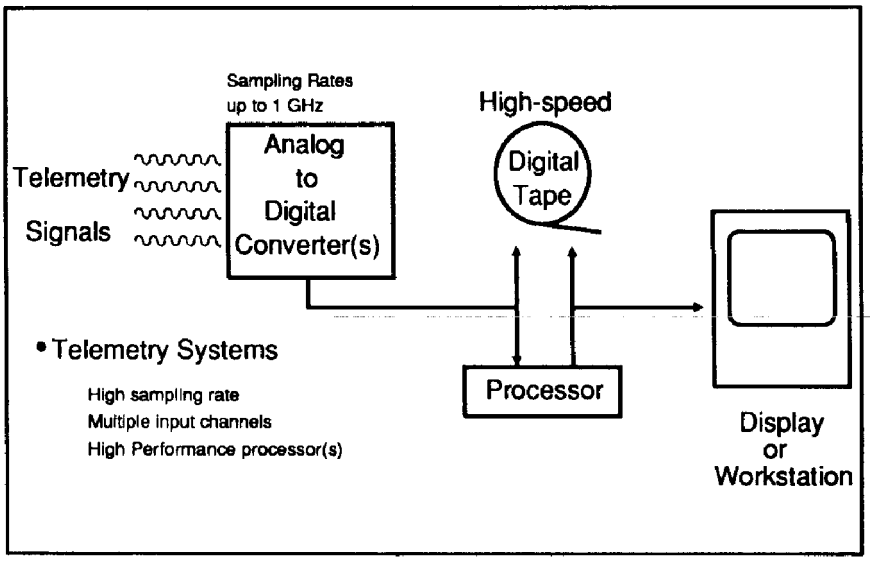

Figure 2

In such a system, the A/D converters digitize incoming telemetry signals. The latest converters operate at rates ranging from 100 MSamples/sec to 1 GSample/sec for a single channel. Sample sizes can vary from 1 to 16 bits, and the A/D can handle multiple channels. The newest models can capture more data channels at higher speeds and have the I/O bandwidth to send data to a computer system at high data rates. At these higher rates, corresponding high-performance processors and a high-speed digital tape recorder are needed.

Many telemetry applications operate in a continuous mode; data is digitized at high bandwidths for an indefinite period of time. Processing of the digitized data is most often required, and the processed data may be recorded. To accomplish this, the computer system must route data from the A/D converter to the processor(s) and then to the digital recorder.

In addition, the A/D converter is likely to input data at an I/O rate different than the sustained output rate required by the tape recorder. Because the tape recorder is a streaming device, the mechanics to start tape moving over the recording head takes a few seconds, making it undesirable to stop the data flow to the tape recorder once it has started. The computer system must buffer the incoming A/D converter data to provide a continuous flow to the tape recorder. This process is called speed matching.

In the overall system architecture, moving data between devices is most important. The computer system must speed-match data between input and output sources. Receiving digitized data, processing, displaying and recording data are asynchronous operations tied together in a pipeline. In rating a computer system and interface to a digital tape recorder, consider the I/O architecture of the complete system. The configuration in Figure 3 shows such a telemetry data acquisition system.

Data Replay / Analysis

Data replay/analysis applications have different requirements. Data has been collected on a high-speed digital tape recorder and the data tapes must be played back for processing and analysis. (See Figure 4.) In addition to data processing, the computer or recorder interface must demultiplex the single data stream into multiple smaller streams.

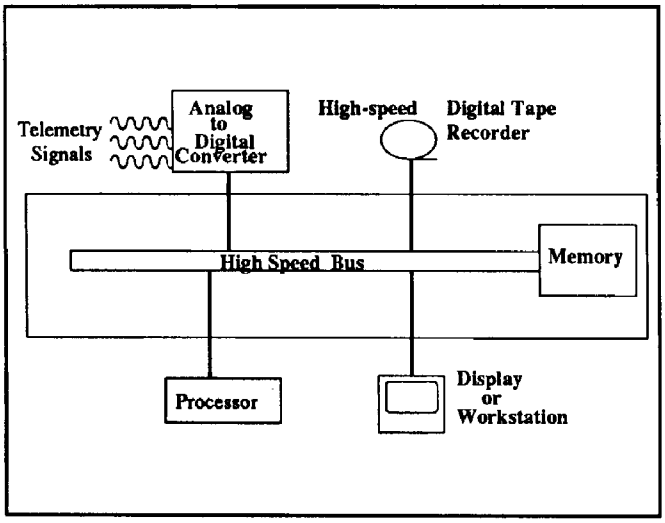

Figure 3

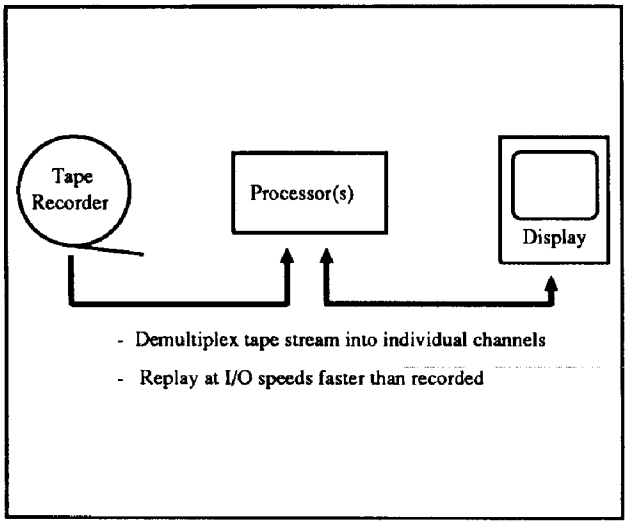

Figure 4

In these applications, each smaller data stream can represent information from receiving devices. Individual streams are processed separately and summed for analysis. Because it is advantageous to replay the data at I/O speeds greater than those at which the data was recorded, multiple-speed digital tape recorders are needed.

This replay/analysis application uses a high bandwidth point-to-point link between the tape recorder and computer. The link can run at different I/O speeds and demultiplex the continuous data stream. The smaller individual streams are loaded into different parts of the computer's memory. All of this functionality requires a high-performance interface with built-in intelligence. Figure 5 illustrates a system configuration solution.

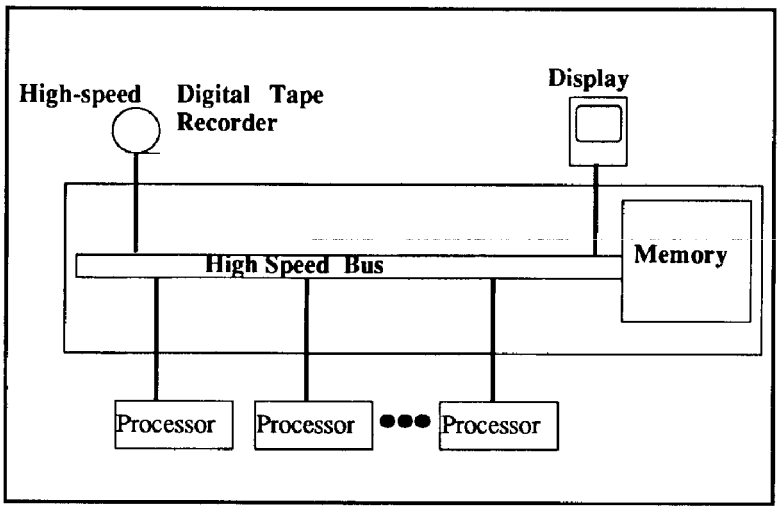

Figure 5

HIGH-SPEED INTERFACES

The integration of a high-speed digital tape recorder to a computer system requires a fast data link, one that will allow sustained high-speed data exchange. For high-end recorders this means a minimum of 10 MBytes/sec. And in the ideal system, the hardware link is under software control so data may be streamed to any resource on the computer system. Two interfaces that meet these requirements are Aptec Computer Systems High-Speed Interface-50 (HSI-50) and the American National Standard for Information systems (ANSI) standard High Performance Parallel Interface (HIPPI).

HSI-50

The HSI-50 connects high-speed peripheral systems and channels to Aptec Computer System's I/O Computer, performing data transfers at rates of up to 50 MBytes/sec. The data flows from the tape recorder to the HSI-50 device bus, through the HSI-50 to the I/O Computer system bus and to shared memory. (Figure 6 illustrates this data flow.) The HSI-50 provides a point-to-point transfer method from tape recorder to computer memory. In addition, it has the performance capacity to interface to high-speed commercially available tape recorders.

The HSI-50 hardware consists of four components: a Motorola 68030 CPU, 1 Mbyte local memory, an interface to the I/O Computer system bus and the HSI-50 device bus. (See Figure 7.) With the 1 MByte of memory, the Motorola 68030 CPU controls the HSI-50. The CPU is programmable using high-level programming languages, Fortran-77 (ANSI X3.9 1977 compatible with MIL-STD 1753 extensions) and C (UNIX 4.3 BSD f77 with extensions).

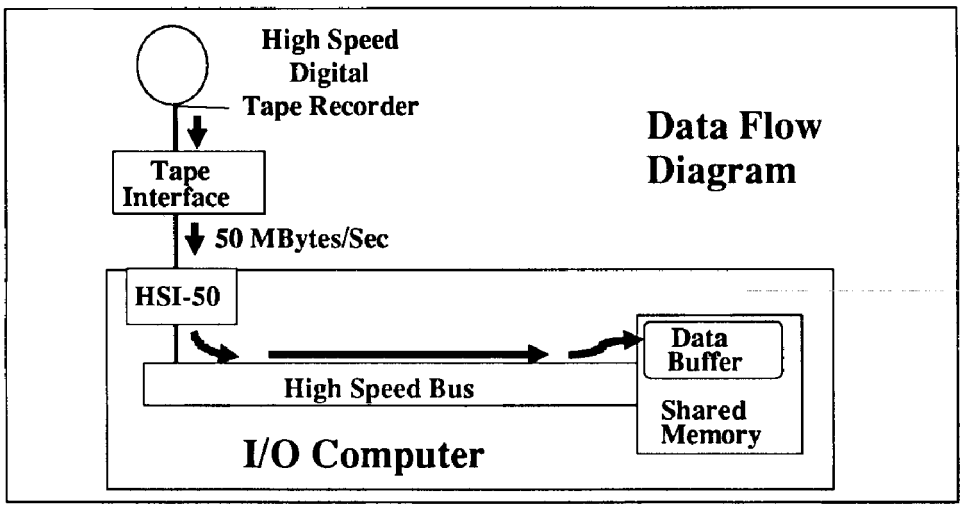

Figure 6

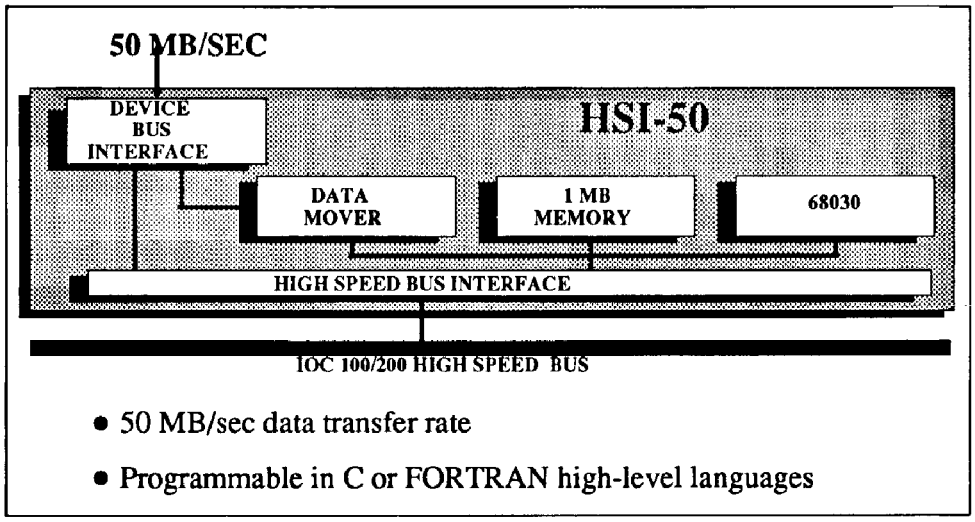

Figure 7

Local memory is used to store programs, local variables and data structures. This means data going to or from the device attached to the HSI-50 is not routed to local memory. Data goes directly between the I/O Computer system bus and the external device.

The HSI-50 device bus is the hardware communication link between the external device and the HSI-50. Aptec Computer Systems has made the device bus an open design. Detailed hardware and timing documentation for the device bus is available, and Aptec offers technical support to help complete an HSI-50 interface to a device. Designed for high-speed, 32-bit data transfers the HSI-50 device bus is bi-directional and synchronous. The 12.5 MHZ clock rate and 32-bit data path allow peak performance data transfers of 50 MBytes/sec.

The performance of the HSI-50 makes it especially suited for interfacing to high-speed digital tape recorders. Active as a data pipe, the HSI-50 blasts large blocks of data to memory. Additionally, because the HSI-50 device bus is an open architecture, integration efforts by recorder manufacturers, computer manufacturers or end users are reduced.

HIPPI

HIPPI is an ANSI standard defining a high-performance point-to-point interface. The ANSI X3T9.3 working group defined the standard and has been working on it since 1987. The HIPPI standard describes the mechanical, electrical and protocol specifications of a high-speed interface. (Note that HIPPI was formerly known as HSC.)

HIPPI standardizes the high-speed interconnection of computer equipment. This standard defines a point-to-point connection running at data rates of 100 or 200 MBytes/sec. The connection is a simplex channel. Along with the hardware interface, HIPPI also defines a data-framing protocol. The protocol specifies how to connect and exchange packets of data between devices. The HIPPI interface is optimized for large block transfers, matching the high-speed digital tape recorders needs.

Because HIPPI is a new standard, few HIPPI interfaces are available. Some computer manufacturers have announced HIPPI support while Aptec Computer Systems has offered a HIPPI interface since the beginning of 1991. The Aptec HIPPI interface uses an adapter attached to an HSI-50. The adapter performs the HIPPI protocol and conforms to the HIPPI physical interface specifications. Figure 8 illustrates HIPPI performance on the Aptec Computer HIPPI Adapter.

No high-speed digital tape recorder manufacturer currently offers a HIPPI interface. There are third-party HIPPI interfaces to recorders, such as the SONY DIR-1000, which will be available in the fall of 1991. Recorder manufacturers should embrace the HIPPI standard, and the end-user community should pressure the market to conform to this standard.

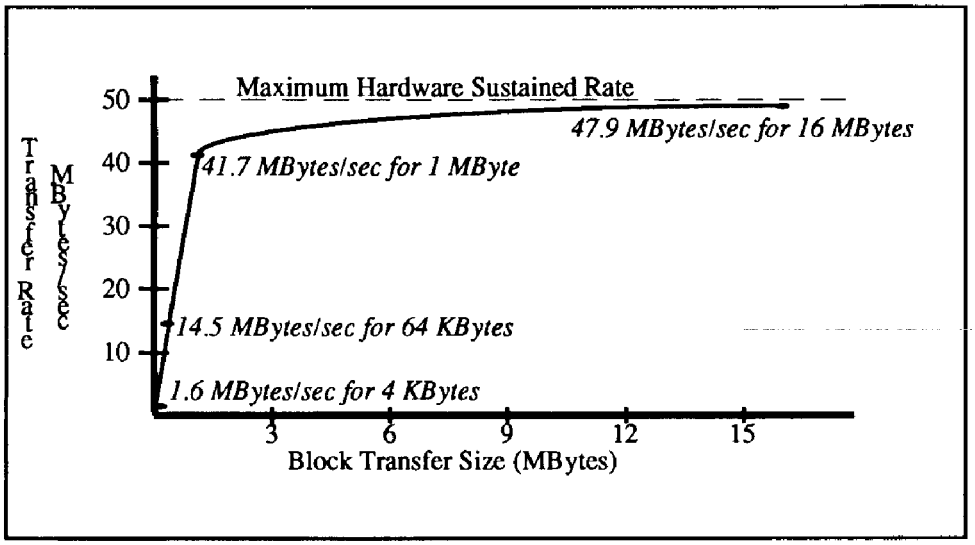

Figure 8

SUMMARY

Digital tape recorders operating at I/O speeds of more than 10 MBytes/sec are needed as computer peripherals in a wide variety of applications, but to increase high-speed recorder integration into more systems, the industry must adopt a broader systems perspective.

For their part, digital tape recorder manufacturers must provide computer interfaces to support the full range of product capabilities. The computer interface, like Aptec Computer System's HSI-50 and HIPPI, ought to support the recorder's high bandwidth and its design should be compatible with industry standards.

On the other hand, computer designers also must consider how high-speed digital tape recorders will coexist in the system with memory, disks, processors and other peripherals. This will require computer makers to look beyond processor performance to concentrate on I/O performance as well. The system bus and interfaces must be structured to support all peripherals involved in an applications data flow.

For computer designers and digital tape recorder manufacturers alike, the ANSI HIPPI standard for high-speed, point-to-point connections should be adopted. Already, Aptec Computer Systems, using an HSI-50 interface to HIPPI, and other manufacturers have demonstrated HIPPI's capability.

End users also figure in this calculation. They must set high expectations for system bandwidth performance. Digital tape recorder manufacturers ought to be told that users will not tolerate devices with no supported computer interface. They must be

told that high-speed recorders with I/O pipes that do not support the full recorder bandwidth are incomplete products. Also, end users must demand that computer manufacturers pay as much attention to I/O architecture as CPU performance. The computer system should not limit the I/O performance of the recorder. In the end, customers have the right to expect manufacturers to provide complete systems solutions.

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