SHOCK-HARDENED, HIGH FREQUENCY, PCM SYSTEM WITH MEMORY FOR EARTH PENETRATOR STUDY APPLICATIONS

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ABSTRACT

Increasing data requirements for earth penetrating vehicles have necessitated the design of a new digital telemetry system with greater signal frequency response, higher resolution, and more memory capacity than used previously. The new system encodes data into 8 bit digital words at a rate of 3.2 megabits per second and stores the data into a 640 Kbit CMOS memory for readout after the recovery of the penetrating vehicle. This paper describes the penetrator program and the new telemetry system developed for it.

INTRODUCTION

For the past two decades, Sandia National Laboratories has been involved in the study of earth and water penetrating vehicles. During this period of time, there has been a continuous evolution of telemetry systems that could survive the very severe mechanical environments experienced by these penetrators and that would provide meaningful data to meet the needs of the development programs. Early programs involved penetrators that impacted at velocities of only a few hundred feet per second. For these tests, the data was transmitted through an R.F. link as the penetrator traveled through the earth. When the impact velocities began approaching 1000 fps, it became impossible to get the trailing wire antenna of the R.F. system to survive the environment. At that time, two new system components were developed. One was a unit to digitize the data during penetration and to store it into a memory. The second was a low frequency transmission system to transmit the stored data through the earth at a low rate (1 Kbits/second) after the vehicle came to rest. This combination was used together until the impact velocities reached 1600 fps where the transmitting antenna could no longer withstand the stress of impact. Since that time all of the systems used for penetrators at Sandia have digitized the data and stored it in memory until the penetrator was recovered. Most of the data collected during these tests have been rigid body data and the frequency content of the data has been less than 1 Khz. The system used for these tests operated at 250 Kbits/second and the data was stored into

a 48 Kbit memory. Now, vehicles are impacting at velocities approaching 2500 fps which creates a need for data at a higher frequency response and resolution. To meet the needs of these new programs, an advanced shock-hardened pulse code modulation (PCM) system has been developed that encodes the input data into 8-bit digital words at a bit rate of 3.2 megabits/second and stores the data into a 640 Kbit CMOS memory array.

TEST DESCRIPTION

The Advanced Penetrator Studies Program for which this system was designed uses a gun-launched penetrator fired into various soils and rock structures. The gun is a 12-inch diameter recoiless tube that uses a reaction mass to generate the pushing forces for the vehicle (Fig. 1). In the operational position, the gun is near vertical and 5 ft. from the ground. When the powder is ignited, the reaction mass is propelled upward and out of the rear of the tube and the projectile is propelled downward into the ground. Velocities to 2400 fps have been achieved with this test method. During the acceleration in the barrel, the electronics package tends to be compressed toward the rear of the vehicle. At impact, the loading on the package changes direction and the forces push the package forward in the vehicle.

At impact, the loading on the package changes direction and the forces push the package forward in the vehicle. During the first body length of penetration, there are severe lateral loadings on the package as well as the longitudinal loadings. To prevent any movement of the instrumentation package during these changing loads, it is compressed into the vehicle during assembly by a hydraulic press with as much as 20,000 psi and then secured into place with locking rings.

DESIGN CONSIDERATIONS

Through the years of testing and the analysis of failures, certain guidelines have been established to aid in the design of a shock hardened system that will survive these environments. Although we have successfully fired systems having tantalum capacitors and ferrite components, their rate of failure has been significant. Tantalum capacitors and ferrite beads are very useful as decoupling components to remove noise from the system. If those components are not used in the system, switching noise, the primary source of noise in a digital system, is going to affect the data conversion unless the conversion is made at a time when the noise is minimal. This is accomplished by delaying the convert pulse to the A/D converter by a few hundred nanoseconds to allow the switching noise caused by the system clock to subside. Also, the elimination of the ferrites means that no transformer type DC-DC converter is available for a power source. Because of this, the systems are designed to operate from a single ended voltage which limits the type of active components that can be utilized. Past systems were designed entirely with CMOS

components that required no negative supplies and the systems worked directly from a battery source through discrete voltage regulators. This new system is also entirely CMOS except for one precision bipolar amplifier that requires a negative supply. The bipolar amplifier was used because the signal bandwidth of the single power supply operational amplifiers was too low to allow system operation at a 400 Ksample per second rate. To provide the negative supply for that one amplifier, we are using a solid state voltage inverter that will supply sufficient power to the amplifier for proper operation. Before an integrated circuit is designed into a system, the lid is removed from a sample and the chip's wire bonding is examined for wire placement and length. If the wire lengths are greater than 80 mils or if the wires are close together where they might short if moved slightly by the shock, the integrated circuit is considered marginal and an alternate source is considered. If there is no alternate, then a sampling of the devices is shock tested before they are used to see if they can survive the environments.

In the new system, the one device that caused the most concern was the memory device. It is a 2K by 8 C-MOS RAM manufactured by Hitachi. At the time the system was designed, there was no alternate source for the RAM and our volume was such that we could not go with a lower density device. We tested the device extensively and had no failure so it was incorporated into the system.

SYSTEM DESCRIPTION

The system block diagram (Fig. 2) shows that there are only eight data input lines to the system. More data channels could have been incorporated into the system when it was designed, but there are a limited number of meaningful monitor points on a penetrator and the minimization of components improves the reliability of the system. Most test vehicles require fewer than eight channels of data so the control of the system is designed around a programmable read only memory (PROM) that can be configured for the program requirements to maximize the available frequency response per data channel. Operating the system at 3.2 megabits per second and encoding into 8 bit words provides a system sampling rate of 400 Ksamples per second (Ksps). That sampling rate can be divided up among the selected data channels in almost any manner depending on the way the PROM is programmed. For example, the system could be dedicated to a single channel sampled at 400 Ksps or to eight channels divided equally at 50 Ksps. The channels can also be subcommutated within the frame to provide formats such as one channel sampled at 200 Ksps, one channel at 100 Ksps, one channel at 50 Ksps, one channel at 25 Ksps, one at 12.5 Ksps, one at 6.25 Ksps, and two at 3.125 Ksps. The PROM is addressed sequentially from an eight stage counter that is incremented by the system clock. The eight stage counter allows 256 states to be addressed within the PROM which can be used for one frame format or for multiple frame formats. There is no provision for reseting the counter during its operation so the frame length must be either 256 words long or some integer

factor of 256. The PROM has four output lines, three of which are used to address the desired input channel and one line to control the insertion of the synchronization words.

The pulse amplitude modulated output of the multiplexer is buffered by the precision bipolar amplifier to provide the necessary drive for the capacitive loading of the signal by the analog to digital (A-D) converter. The signal is digitized into an 8-bit word by a CMOS flash A-D converter circuit (Fig. 3) which does an instantaneous conversion on the input sample. The circuit consists of four 6-bit flash A-D converters manufactured by RCA and two logic gate packages. The first converter has a positive reference voltage of 1.280 volts and a negative reference voltage of analog ground. The second converter is referenced between 2.560 volts and 1.280 volts; the third is referenced between 3.840 volts and 2.560 volts; and the fourth is referenced between 5.120 volts and 3.840 volts. When the input sample is between o volts and 1.280 volts, the first converter is operational and the other three are disabled. If the voltage exceeds 1.280 volts, the first converter indicates an overflow and disables itself and enables the second converter. If the voltage is greater than 2.560 volts, the second converter exhibits an overflow condition which disables itself and enables the third converter. So the overflow indicators of each converter control whether the converters are enabled or disabled, and only one converter can be enabled at a time. The overflow indicators are decoded to determine which voltage quadrant in which the input sample lies, and the two bits indicative of that quadrant are used for the two most significant bits of the data word and the six bits encoded by the selected converter become the six least significant bits of the data word. This circuit approach was chosen over one of the more conventional A-D converters because it can convert in less than 100 nanoseconds and eliminates the need for a sample and hold amplifier. The sample and hold amplifier is very susceptable to switching noise which is present in the system because of the difficulty of filtering the noise with the available components. The flash A-D converter can be clocked between switching times which minimizes the effect of the switching noise. After the conversion, the data is placed onto the eight bit data bus through a tri-state buffer. A synchronization word generator is also tri-stated onto the data bus so that three 8-bit sync words can be placed on the data bus when the PROM commands a sync word insert. Also on the eight-bit data bus is the CMOS memory array which can receive the digitized data and sync words for storage, or, if commanded to do so, send its contents out through the data bus to a parallel to serial converter for transmission out of the system. The memory is comprised of 8 modules, each having 80 Kbits of storage and the necessary control for protecting the stored data and for getting the data out of memory if the rest of the system is not operational.

Since the function of the system is to take a two hundred millisecond snapshot of the data and store that piece of data for several weeks, the control of the memory is very important. There are four external control lines required for proper operation of the system. They are: a reset line, an arm line, a trigger line, and an output command line. The reset command

brings the system from the data hold state, where all write functions are inhibited to the memory protecting the data that is stored in it, to a state that is a low power standby for writing new data. To reset the system, an external signal of at least 22 volts is required. This prevents accidental reset during the penetration event since no voltage is present in the system greater than 18 volts. In the low power standby state, the write functions for the memory are unlocked, but they are not activated until the next control signal, the arm signal, is received. Again, the arm signal must be greater than 22 volts to prevent accidental arming of the system by an internal function. When the arm signal is received, the write functions are activated and all encoded data is sequentially loaded into the memory. Until the vehicle is fired, the data is continually written into the memory, overwriting old data as the memory capacity is exceeded. When the vehicle is fired, the acceleration initiates the timing circuits that count the data words as they are loaded into memory so that the write operation can be stopped short of overwriting the first acceleration data. This captures the data from just prior to firing through the time the vehicle comes to rest. The timing circuits can also be initiated by an external digital trigger signal to facilitate checkout of the system before the unit is fired. When the timing circuits have completed their countdown, all write functions to the memory are inhibited so that the data contained within cannot be accidentally altered. Also, all unnecessary control lines for the memory are turned off by tri-state switches so that the memory and its associated readout circuits are isolated from the main system power provided by Ni-Cad batteries which discharge within a few hours of the test. The memory and readout circuitry is then powered from a 5 volt mercury battery that provides keep alive power for up to 3 months to allow ample time for the recovery of the unit. When the vehicle is recovered, a back plate is removed allowing access to a 9 pin Canon MDM connector. A control box is connected to the connector and the o output command line is brought high by connecting the system keep alive power to it through the control box. The data is shifted out of the system serially and stored onto magnetic tape for shipment back to the data reduction facility for reconstruction.

MECHANICAL ASSEMBLY

The telemetry package is a cylindrical assembly 3.750 inches is diameter and approximately 14 inches long including the battery pack. The electronics assembly is comprised of a stack of round printed circuit boards, each assembled as an independent module, placed into a steel sleeve that is mounted to the battery (Fig. 1). Each printed circuit board is 3.6 inches in diameter and has the interface connections to other boards brought out to a ring of small sockets around the perimeter of the board. A potting ring is placed on both sides of the printed circuit just inside the ring of sockets and then filled with a micro balloon potting. After the potting is cured, both sides are machined so that the thickness of the module is exact and the two faces are parallel. All of the modules are stacked up and berrilium wire is run the full length of the system through a socket on each

board which interconnects the boards in a wire cage configuration. The stack of modules is compressively loaded into the steel cylinder and the voids are filled with polystyrene beads and heated until the package is solid. That system is then placed into the back of the vehicle and again compressively loaded so that nothing can move during the test event.

CONCLUSION

In the past, the telemetry systems for penetrators were capable of measuring only the rigid body penetration event. That data was sufficient for the initial development of the penetrator study program because so little was known about the penetrator response during the event. Now, rigid body response is understood and information is needed on the high frequency longitudinal and bending vibratory modes of the penetrator to completely define the structural dynamics problem. This new system is capable of supplying that data and will be useful to penetrator programs in the future.

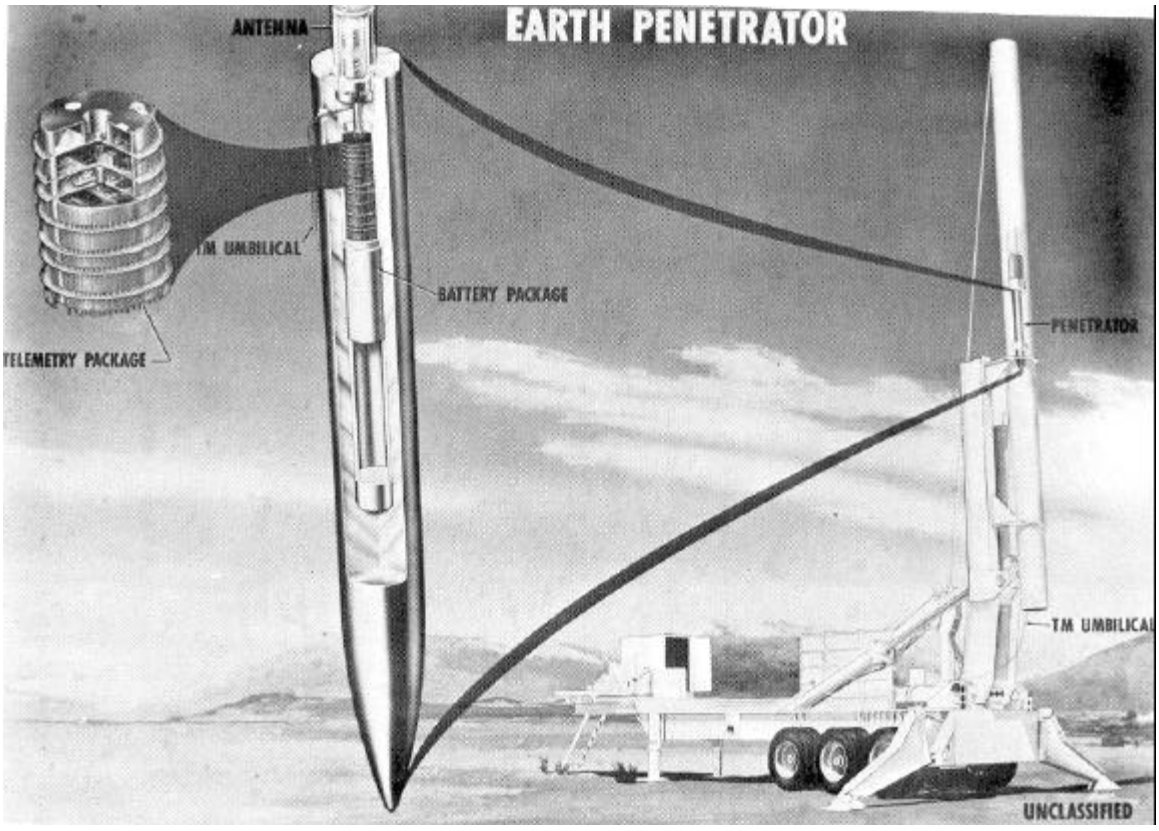

FIGURE 1. GUN LAUNCHED PENETRATOR

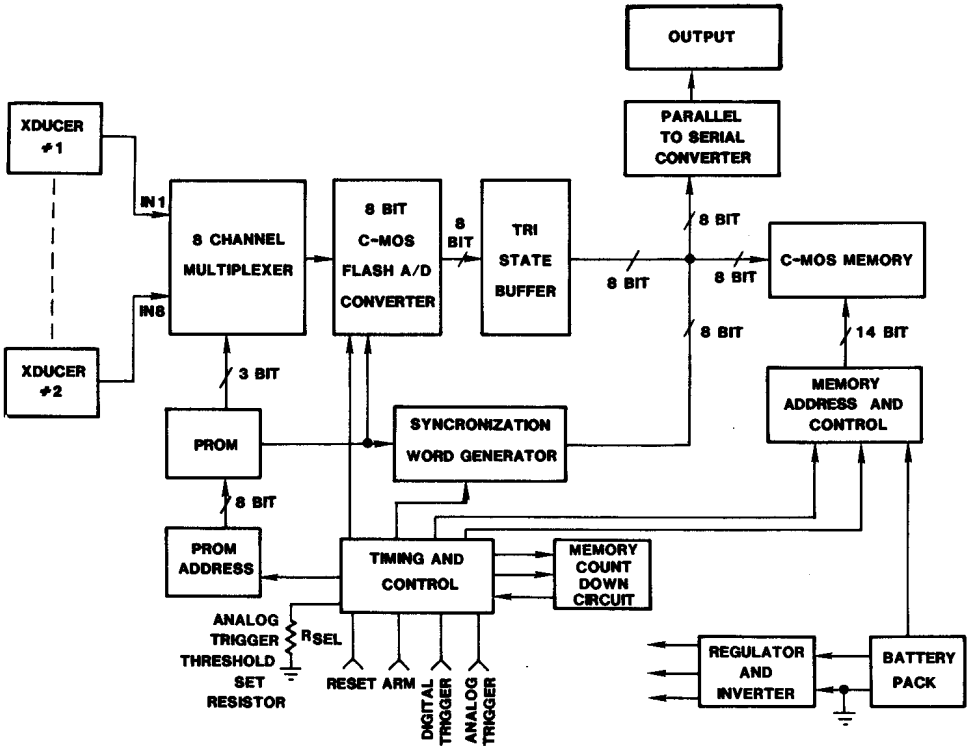

FIGURE 2. SYSTEM BLOCK DIAGRAM

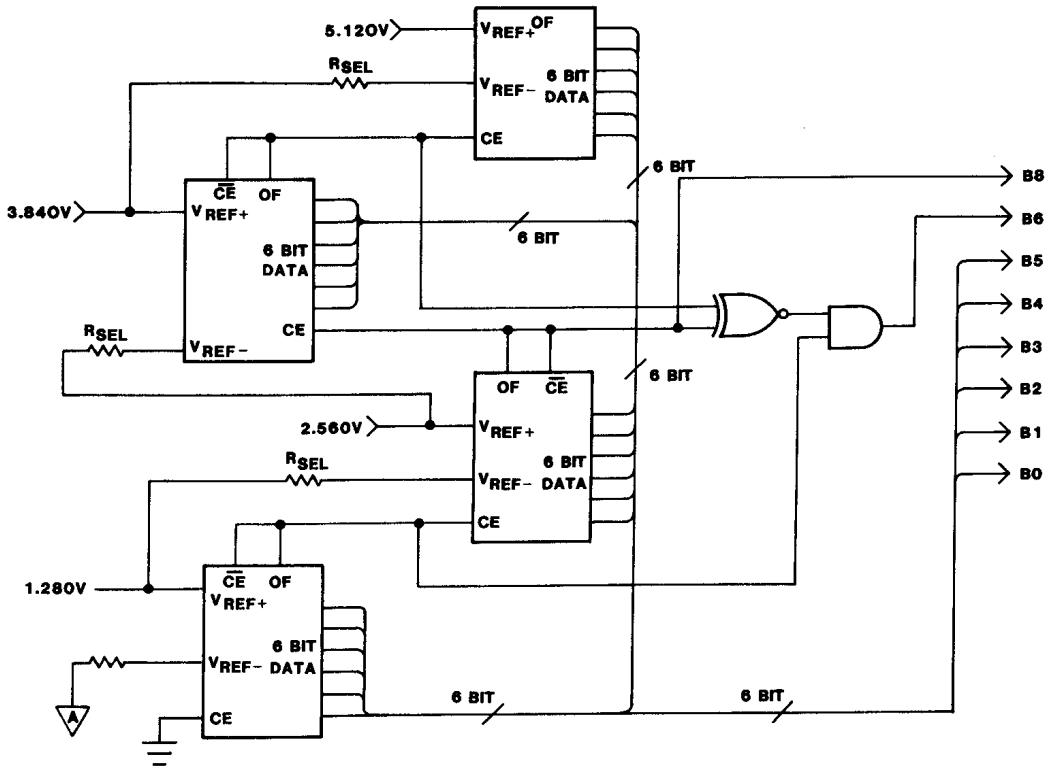

FIGURE 3. C-MOS 8 BIT FLASH CONVERTER CIRCUIT